2.4 GHz CyFi™ Transceiver

Features

- 2.4 GHz Direct Sequence Spread Spectrum (DSSS) radio transceiver
- Operates in the unlicensed worldwide Industrial, Scientific, and Medical (ISM) band (2.400 GHz – 2.483 GHz)
- 21 mA operating current (Transmit at –5 dBm)
- Transmit power up to +4 dBm
- Receive sensitivity up to –97 dBm
- Sleep Current <1 µA
- DSSS data rates up to 250 kbps, GFSK data rate of 1 Mbps
- Low external component count
- Auto Transaction Sequencer (ATS) - no MCU intervention
- Framing, Length, CRC16, and Auto ACK
- Power Management Unit (PMU) for MCU
- Fast Startup and Fast Channel Changes
- Separate 16-byte Transmit and Receive FIFOs
- Dynamic data rate reception
- Receive Signal Strength Indication (RSSI)
- Serial Peripheral Interface (SPI) control while in sleep mode
- 4 MHz SPI microcontroller interface
- Battery Voltage Monitoring Circuitry
- Supports coin-cell operated applications
- Operating voltage from 1.8V to 3.6V
- Operating temperature from 0 to 70°C
- Space saving 40-pin QFN 6x6 mm package

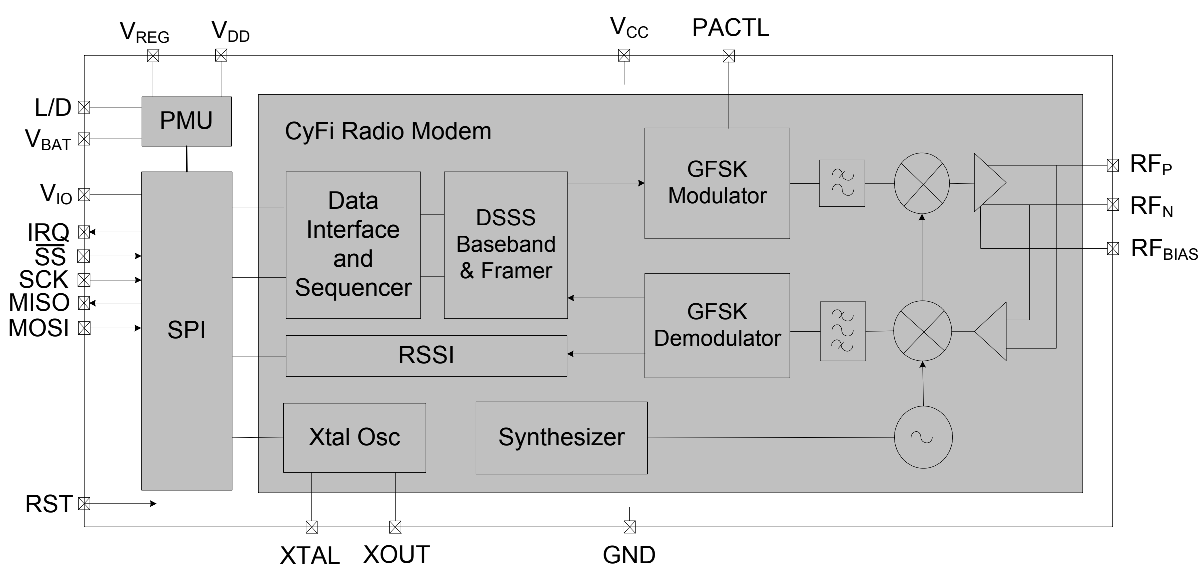
Applications

- Wireless Sensor Networks
- Wireless Actuator Control
- Home Automation
- White Goods
- Commercial Building Automation
- Automatic Meter Readers
- Precision Agriculture
- Remote Controls
- Consumer Electronics
- Personal Health and Fitness
- Toys

Applications Support

See www.cypress.com for development tools, reference designs, and application notes.

Logic Block Diagram



Functional Description

The CYRF7936 CyFi™ Transceiver is a Radio IC designed for low-power embedded wireless applications. Combined with Cypress's PSoC programmable system-on-chip and a CyFi network protocol stack, CYRF7936 can be used to implement a complete CyFi wireless system.

Figure 1. Pin Diagram - CYRF7936 40-Pin QFN

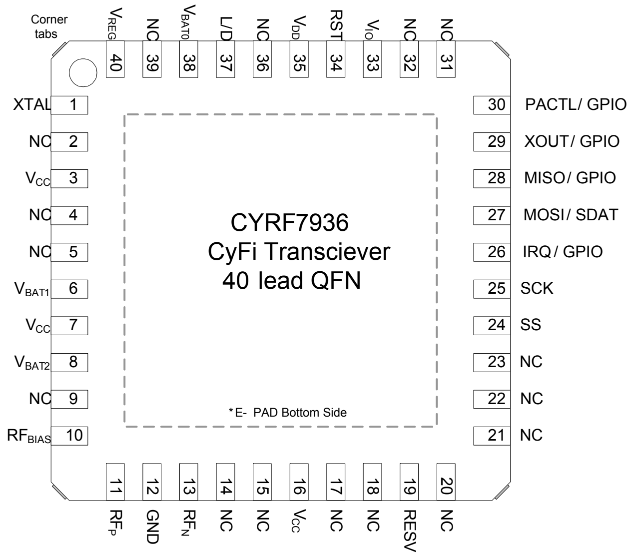


Table 1. Pin Description - CYRF7936 40-Pin QFN

Pin Number	Name	Type	Default	Description
13	RF_N	IO	I	Differential RF signal to and from antenna.
11	RF_P	IO	I	Differential RF signal to and from antenna.
10	RF_{BIAS}	O	O	RF IO 1.8V reference voltage.
30	PACTL	IO	O	Control signal for external PA, T/R switch, or GPIO.
1	XTAL	I	I	12 MHz crystal.
29	XOUT	IO	O	Buffered 0.75, 1.5, 3, 6, or 12 MHz clock, $\overline{\text{PACTL}}$, or GPIO. Tri-states in sleep mode (configure as GPIO drive LOW).
25	SCK	I	I	SPI clock.
28	MISO	IO	Z	SPI data output pin (Master In Slave Out), or GPIO (in SPI 3-pin mode). Tri-states when SPI 3PIN = 0 and SS# is deasserted.
27	MOSI	IO	I	SPI data input pin (Master Out Slave In), or SDAT.
24	SS#	I	I	SPI enable, active LOW assertion. Enables and frames transfers.
26	IRQ	IO	O	Interrupt output (configurable active HIGH or LOW), or GPIO.
34	RST	I	I	Device reset. Internal 10 kohm pull down resistor. Active HIGH, typically connect through a 0.47 µF capacitor to V_{BAT}. Must have RST = 1 event the first time power is applied to the radio. Otherwise the state of the radio control registers is unknown.
37	LVD	O		PMU inductor/diode connection, when used. If not used, connect to GND.
40	V_{REG}	Pwr		PMU boosted output voltage feedback.
35	V_{DD}	Pwr		Decoupling pin for 1.8V logic regulator, connect through a 0.47 µF capacitor to GND.
6, 8, 38	$V_{BAT(0-2)}$	Pwr		V_{BAT} = 1.8V to 3.6V. Main supply.
3, 7, 16	V_{CC}	Pwr		V_{CC} = 2.4V to 3.6V. Typically connected to V_{REG}.

Table 1. Pin Description - CYRF7936 40-Pin QFN (continued)

Pin Number	Name	Type	Default	Description
33	V_{IO}	Pwr		IO interface voltage, 1.8–3.6V.
19	RESV	I		Must be connected to GND.
2, 4, 5, 9, 14, 15, 18, 17, 20, 21, 22, 23, 32, 36, 39, 31	NC	NC		Connect to GND.
12	GND	GND		Ground.
E-PAD	GND	GND		Must be soldered to Ground.
Corner Tabs	NC	NC		Do Not solder the tabs and keep other signal traces clear. All tabs are common to the lead frame or paddle which is grounded after the pad is grounded. While they are visible to the user, they do not extend to the bottom.

Functional Overview

The CYRF7936 IC is designed to implement wireless device links operating in the worldwide 2.4 GHz ISM frequency band. It is intended for systems compliant with worldwide regulations covered by ETSI EN 301 489-1 V1.41, ETSI EN 300 328-1 V1.3.1 (Europe), FCC CFR 47 Part 15 (USA and Industry Canada), and TELEC ARIB_T66_March, 2003 (Japan).

The CYRF7936 contains a 2.4 GHz CyFi radio modem which features a 1 Mbps GFSK radio front-end, packet data buffering, packet framer, DSSS baseband controller, and Received Signal Strength Indication (RSSI). CYRF7936 features a SPI interface for data transfer and device configuration.

The CyFi radio modem supports 98 discrete 1 MHz channels (regulations may limit the use of some of these channels in certain jurisdictions).

The baseband performs DSSS spreading/despreading, Start of Packet (SOP), End of Packet (EOP) detection, and CRC16 generation and checking. The baseband may also be configured to automatically transmit Acknowledge (ACK) handshake packets whenever a valid packet is received.

When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates. This enables the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems that use high data rates at shorter distances or in a low-moderate interference environment or both. It changes to lower data rates at longer distances or in high interference environments or both.

In addition, the CYRF7936 IC has a Power Management Unit (PMU), which allows direct connection of the device to any battery voltage in the range 1.8V to 3.6V. The PMU conditions the battery voltage to provide the supply voltages required by the device, and may supply external devices.

Data Transmission Modes

The CyFi radio transceiver supports two different data transmission modes:

- In GFSK mode, data is transmitted at 1 Mbps, without any DSSS.
- In 8DR mode, DSSS is enabled and eight bits are encoded in each derived code symbol transmitted.

Both 64 chip and 32 chip Pseudo Noise (PN) codes are supported in 8DR mode. In general, lower data rates reduce packet error rate in any given environment.

Packet Framing

The CYRF7936 IC device supports the following data packet framing features:

SOP

Packets begin with a two-symbol Start-of-Packet (SoP) marker. The SOP_CODE_ADR PN code used for the SOP is different from that used for the “body” of the packet, and if desired may be a different length. SOP must be configured to be the same length on both sides of the link.

Length

This is the first eight bits after the SOP symbol, and is transmitted at the payload data rate. An EoP condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16.

CRC16

The device may be configured to append a 16 bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver verifies the calculated CRC16 for the payload data against the received value in the CRC16 field. The seed value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 is checked against both the configured and zero CRC16 seeds.

CRC16 detects the following errors:

- Any one bit in error.
- Any two bits in error (irrespective of how far apart, which column, and so on).
- Any odd number of bits in error (irrespective of the location).
- An error burst as wide as the checksum itself.

Figure 2 shows an example packet with SOP, CRC16, and lengths fields enabled, and Figure 3 shows a standard ACK packet.

Figure 2. Example Packet Format

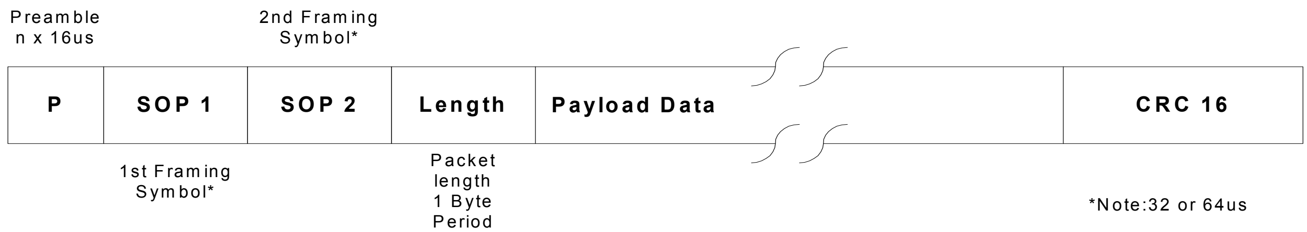
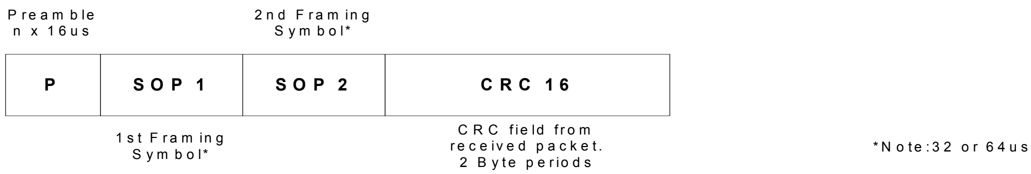


Figure 3. Example ACK Packet Format



Packet Buffers

All data transmission and reception use the 16 byte packet buffers - one for transmission and one for reception.

The transmit buffer allows loading a complete packet of up to 16 bytes of payload data in one burst SPI transaction. This is then transmitted with no further MCU intervention. Similarly, the receive buffer allows receiving an entire packet of payload data up to 16 bytes with no firmware intervention required until the packet reception is complete.

The CYRF7936 IC supports packets up to 255 bytes. However, the actual maximum packet length depends on the accuracy of the clock on each end of the link and the data mode. Interrupts are provided to allow an MCU to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the MCU can load 16 bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the MCU must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

Auto Transaction Sequencer (ATS)

The CYRF7936 IC provides automated support for transmission and reception of acknowledged data packets.

When transmitting in transaction mode, the device automatically:

- starts the crystal and synthesizer
- enters transmit mode
- transmits the packet in the transmit buffer
- transitions to receive mode and waits for an ACK packet
- transitions to the transaction end state when an ACK packet is received or a timeout period expires

Similarly, when receiving in transaction mode, the device automatically:

- waits in receive mode for a valid packet to be received
- transitions to transmit mode, transmits an ACK packet
- transitions to the transaction end state (receive mode to await the next packet, and so on.)

The contents of the packet buffers are not affected by the transmission or reception of ACK packets.

In each case, the entire packet transaction takes place without any need for MCU firmware action (as long as packets of 16 bytes or less are used). To transmit data, the MCU must load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware must retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

Data Rates

The CYRF7936 IC supports the following data rates by combining the PN code lengths and data transmission modes described in the previous sections:

- 1000 kbps (GFSK)
- 250 kbps (32 chip 8DR)
- 125 kbps (64 chip 8DR)

Functional Block Overview

2.4 GHz CyFi Radio Modem

The CyFi radio Modem is a dual conversion low IF architecture optimized for power, range, and robustness. The CyFi radio modem employs channel-matched filters to achieve high performance in the presence of interference. An integrated Power Amplifier (PA) provides up to +4 dBm transmit power, with an output power control range of 34 dB in seven steps. The supply current of the device is reduced as the RF output power is reduced.

Table 2. Internal PA Output Power Step Table

PA Setting	Typical Output Power (dBm)
7	+4
6	0
5	–5
4	–13
3	–18
2	–24
1	–30
0	–35

Frequency Synthesizer

Before transmission or reception may begin, the frequency synthesizer must settle. The settling time varies depending on channel; 25 fast channels are provided with a maximum settling time of 100 μs.

The 'fast channels' (less than 100 μs settling time) are every third channel, starting at 0 up to and including 72 (for example, 0, 3, 6, 9 …. 69, 72).

Baseband and Framer

The baseband and framer blocks provide the DSSS encoding and decoding, SOP generation and reception, CRC16 generation and checking, and EOP detection and length field.

Packet Buffers and Radio Configuration Registers

Packet data and configuration registers are accessed through the SPI interface. All configuration registers are directly addressed through the address field in the SPI packet. Configuration registers allow configuration of DSSS PN codes, data rate, operating mode, interrupt masks, interrupt status, and so on.

SPI Interface

The CYRF7936 IC has an SPI interface supporting communication between an application MCU and one or more slave devices (including the CYRF7936). The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of Slave Select (SS#), Serial Clock (SCK), Master Out-Slave In (MOSI), Master In-Slave Out (MISO), or Serial Data (SDAT).

SPI communication may be described as the following:

- Command Direction (bit 7) = '1' enables SPI write transaction. When it equals a '0', it enables SPI read transactions.
- Command Increment (bit 6) = '1' enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access. Otherwise the same address is accessed.
- Six bits of address
- Eight bits of data

The device receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active LOW Slave Select (SS#) pin must be asserted to initiate an SPI transfer.

The application MCU can initiate SPI data transfers using a multi-byte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes shown in Figure 4 through Figure 7 on page 6.

The SPI communications interface has a burst mechanism, where the first byte can be followed by as many data bytes as required. A burst transaction is terminated by deasserting the slave select (SS# = 1).

The SPI communications interface single read and burst read sequences are shown in Figure 5 and Figure 6 on page 6, respectively.

The SPI communications interface single write and burst write sequences are shown in Figure 7 and Figure 8 on page 6, respectively.

This interface may be optionally operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT). When using 3-pin mode, user firmware must ensure that the MOSI pin on the MCU is in a high impedance state except when MOSI is actively transmitting data.

The device registers may be written to or read from one byte at a time, or several sequential register locations may be written or read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files. Register files are FIFOs written to and read from using nonincrementing burst SPI transactions.

The IRQ pin function may be optionally multiplexed onto the MOSI pin. When this option is enabled, the IRQ function is not available while the SS# pin is LOW. When using this configuration, user firmware must ensure that the MOSI pin on the MCU is in a high impedance state whenever the SS# pin is HIGH.

The SPI interface is not dependent on the internal 12 MHz clock. Registers may therefore be read from or written to when the device is in sleep mode, and the 12 MHz oscillator disabled.

The SPI interface and the IRQ and RST pins have a separate voltage reference pin (V_{IO}). This enables the device to interface directly to MCUs operating at voltages below the CYRF7936 IC supply voltage.

Figure 4. SPI Transaction Format

	Byte 1			Byte 1+N
Bit #	7	6	[5:0]	[7:0]
Bit Name	DIR	INC	Address	Data

Figure 5. SPI Single Read Sequence

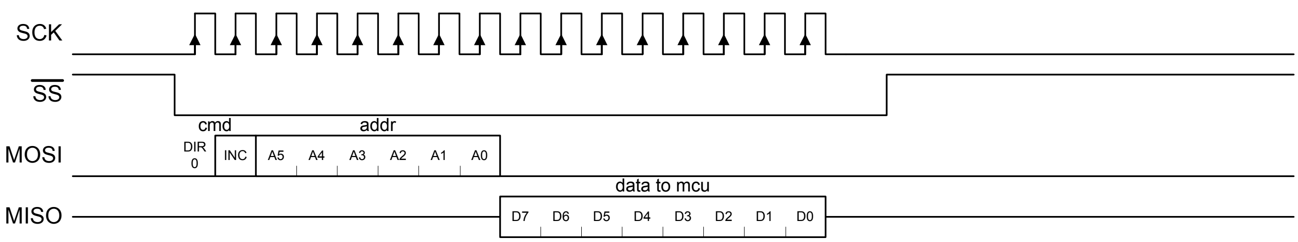


Figure 6. SPI Incrementing Burst Read Sequence

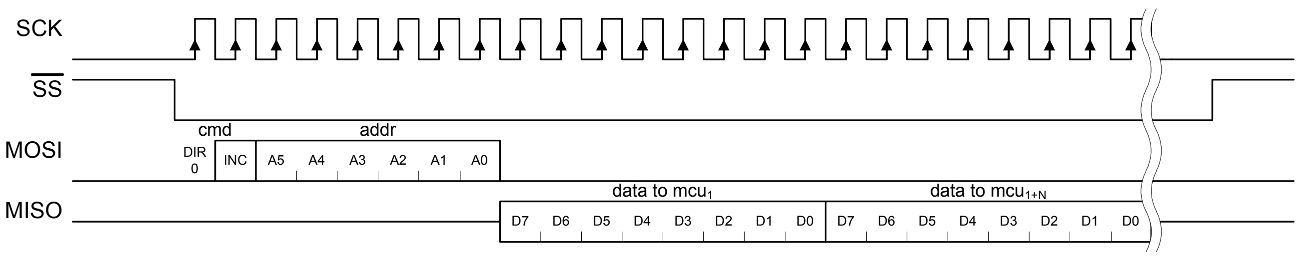


Figure 7. SPI Single Write Sequence

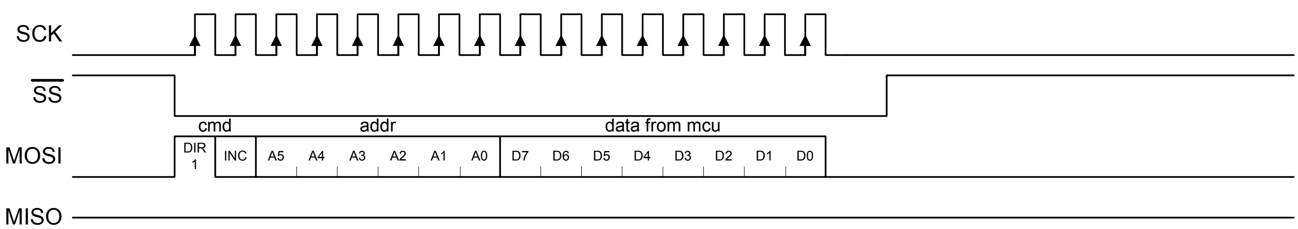
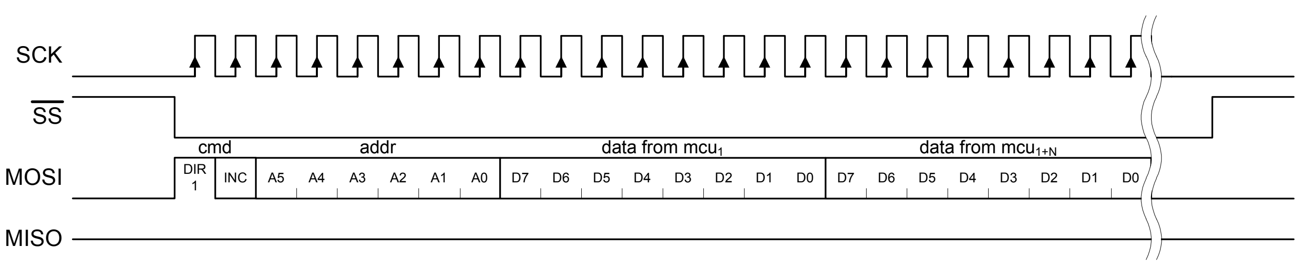


Figure 8. SPI Incrementing Burst Write Sequence



Interrupts

The device provides an interrupt (IRQ) output, which is configurable to indicate the occurrence of various different events. The IRQ pin may be programmed to be either active HIGH or active LOW, and be either a CMOS or open drain output. The available interrupts are described in the section Register Descriptions on page 12.

The CYRF7936 IC features three sets of interrupts: transmit, receive, and system interrupts. These interrupts all share a single pin (IRQ), but can be independently enabled or disabled. The contents of the enable registers are preserved when switching between transmit and receive modes.

If more than one interrupt is enabled at any time, it is necessary to read the relevant status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that would otherwise cause an interrupt can be determined by reading the appropriate status register. It is therefore possible to use the devices without the IRQ pin, by polling the status registers to wait for an event, rather than using the IRQ pin.

Clocks

A 12 MHz crystal (30 ppm or better) is directly connected between XTAL and GND without the need for external capacitors. A digital clock out function is provided, with selectable output frequencies of 0.75, 1.5, 3, 6, or 12 MHz. This output may be used to clock an external microcontroller (MCU) or ASIC. This output is enabled by default, but may be disabled.

The requirements to directly connect the crystal to the XTAL pin and GND are:

- Nominal Frequency: 12 MHz
- Operating Mode: Fundamental Mode
- Resonance Mode: Parallel Resonant
- Frequency Initial Stability: ±30 ppm
- Series Resistance: $\leq$60 ohms
- Load Capacitance: 10 pF
- Drive Level: 100 µW

Power Management

The operating voltage of the device is 1.8V to 3.6V DC, which is applied to the V_{BAT} pin. The device can be shut down to a fully static sleep mode by writing to the FRC END = 1 and END STATE = 000 bits in the XACT_CFG_ADR register over the SPI interface. The device enters sleep mode within 35 µs after the last SCK positive edge at the end of this SPI transaction. Alternatively, the device may be configured to automatically enter sleep mode after completing the packet transmission or reception. When in sleep mode, the on-chip oscillator is stopped, but the SPI interface remains functional. The device wakes from sleep mode automatically when the device is commanded to enter transmit or receive mode. When resuming from sleep mode, there is a short delay while the oscillator restarts. The device can be configured to assert the IRQ pin when the oscillator has stabilized.

The output voltage (V_{REG}) of the Power Management Unit (PMU) is configurable to several minimum values between 2.4V and 2.7V. V_{REG} may be used to provide up to 15 mA (average load) to external devices. It is possible to disable the PMU and provide an externally regulated DC supply voltage to the device's main supply in the range 2.4V to 3.6V. The PMU also provides a regulated 1.8V supply to the logic.

The PMU is designed to provide high boost efficiency (74–85% depending on input voltage, output voltage, and load) when using a Schottky diode and power inductor, eliminating the need for an external boost converter in many systems where other components require a boosted voltage. However, reasonable efficiencies (69–82% depending on input voltage, output voltage, and load) may be achieved when using low cost components such as SOT23 diodes and 0805 inductors.

The PMU also provides a configurable low battery detection function, which may be read over the SPI interface. One of seven thresholds between 1.8V and 2.7V may be selected. The interrupt pin may be configured to assert when the voltage on the V_{BAT} pin falls below the configured threshold. LV IRQ is not a latched event. Battery monitoring is disabled when the device is in sleep mode.

Low Noise Amplifier and Received Signal Strength Indication

The gain of the receiver can be controlled directly by clearing the AGC EN bit and writing to the Low Noise Amplifier (LNA) bit of the RX_CFG_ADR register. Clearing the LNA bit reduces the receiver gain approximately 20 dB, allowing accurate reception of very strong received signals (for example, when operating a receiver very close to the transmitter). Approximately 30 dB of receiver attenuation can be added by setting the Attenuation (ATT) bit. This limits data reception to devices at very short ranges. Disabling AGC and enabling LNA is recommended, unless receiving from a device using external PA.

When the device is in receive mode the RSSI_ADR register returns the relative signal strength of the on-channel signal power.

When receiving, the device automatically measures and stores the relative strength of the signal being received as a five bit value. An RSSI reading is taken automatically when the SoP is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI_ADR register, allowing the background RF energy level on any given channel to be easily measured when RSSI is read while no signal is being received. A new reading can occur as fast as once every 12 µs.

Application Examples

Figure 9. Recommended Circuit for Systems where VBAT ≤ 2.4V

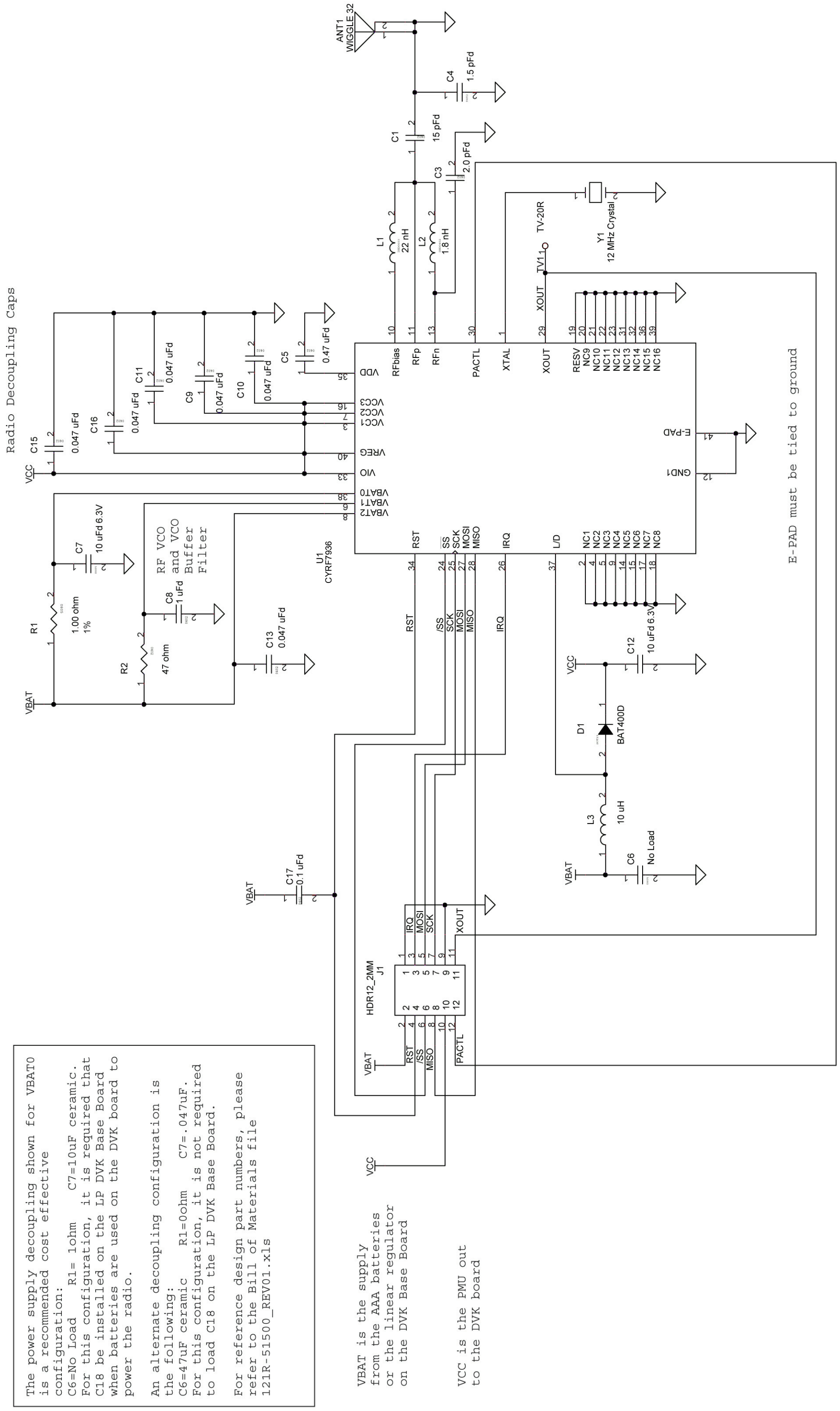


Table 3. Recommended BoM for Systems where VBAT ≤ 2.4V

Item	Qty	CY Part Number	Reference	Description	Manufacturer	Mfr Part Number
1	1	NA	ANT1	2.5GHZ H-STUB WIGGLE ANTENNA FOR 32MIL PCB	NA	NA
2	1	730-10012	C1	CAP 15PF 50V CERAMIC NPO 0402	Panasonic	ECJ-0EC1H150J
3	1	730-11955	C3	CAP 2.0 PF 50V CERAMIC NPO 0402	Kemet	C0402C209C5GAC TU
4	1	730-11398	C4	CAP 1.5PF 50V CERAMIC NPO 0402 SMD	PANASONIC	ECJ-0EC1H1R5C
5	1	730R-13322	C5	CAP CER .47UF 6.3V X5R 0402	Murata	GRM155R60J474K E19D
6	2	730-13037	C12,C7	CAP CERAMIC 10UF 6.3V X5R 0805	Kemet	C0805C106K9PAC TU
7	1	730-13400	C8	CAP 1 uF 6.3V CERAMIC X5R 0402	Panasonic	ECJ-0EB0J105M
8	6	730-13404	C9,C10,C11, C13,C15,C16	CAP 0.047 uF 50V CERAMIC X5R 0402	AVX	0402YD473KAT2A
9	1	730R-11952	C17	CAP .10UF 10V CERAMIC X5R 0402	Kemet	C0402C104K8PAC TU
10	1	800-13317	D1	DIODE SCHOTTKY 0.5A 40V SOT23	DIODES INC	BAT400D-7-F
11	1	420-11976	J1	CONN HEADER 12 PIN 2MM GOLD	Hirose Electric Co. LTD.	DF11-12DP-2DSA(01)
12	1	800-13401	L1	INDUCTOR 22NH 2% FIXED 0603 SMD	Panasonic - ECG	ELJ-RE22NGF2
13	1	800-11651	L2	INDUCTOR 1.8NH +-.3NH FIXED 0402 SMD	Panasonic - ECG	ELJ-RF1N8DF
14	1	800-10594	L3	COIL 10UH 1100MA CHOKE 0805	Newark	30K5421
15	1	630-11356	R1	RES 1.00 OHM 1/8W 1% 0805 SMD	Yageo	9C08052A1R00FK HFT
16	1	610-13402	R2	RES 47 OHM 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ470X
17	1	CYRF7936-40LFXC	U1	IC, LP 2.4 GHz RADIO SoC QFN-40	Cypress Semiconductor	CYRF7936-40LFXC
18	1	800-13259	Y1	CRYSTAL 12.00MHZ HC49 SMD	eCERA	GF-1200008
19	1	PDCR-9515 REV01	PCB	PRINTED CIRCUIT BOARD	Cypress Semiconductor	PDCR-9515 REV01
20	1	920-11206	LABEL1	Serial Number		
21	1	920-51500 REV01	LABEL2	PCA #		121R-51500 REV01

Figure 10. Recommended Circuit for Systems where V_{BAT} is 2.4V - 3.6V (PMU Disabled)

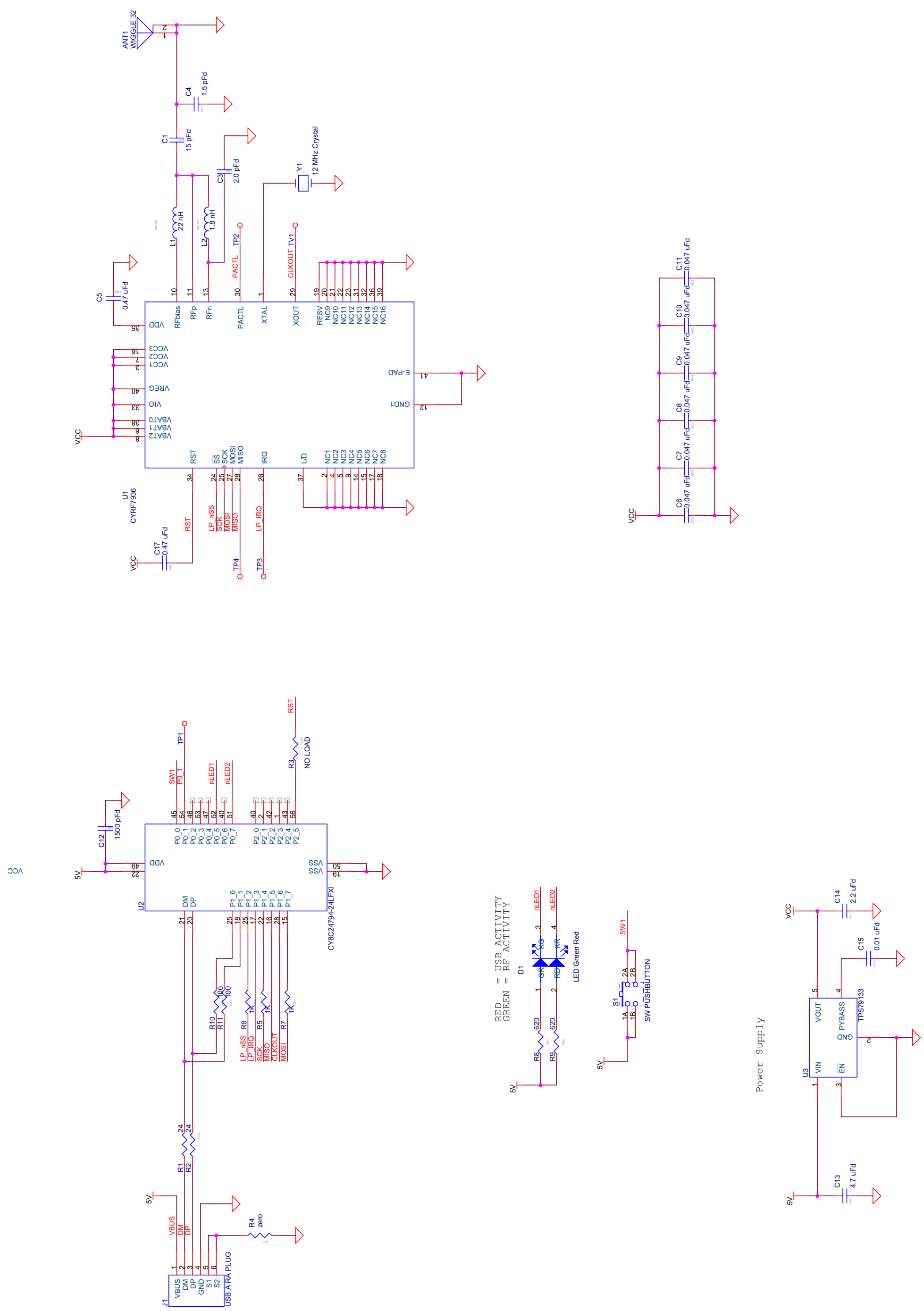


Table 4. Recommended BoM for Systems where V_{BAT} is 2.4V - 3.6V (PMU disabled)

Item	Qty	CY Part Number	Reference	Description	Manufacturer	Mfr Part Number
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2	1	730-10012	C1	CAP 15PF 50V CERAMIC NPO 0402	Panasonic	ECJ-0EC1H150J
3	1	730-11955	C3	CAP 2.0 PF 50V CERAMIC NPO 0402	Kemet	C0402C209C5GACTU
4	1	730-11398	C4	CAP 1.5PF 50V CERAMIC NPO 0402 SMD	PANASONIC	ECJ-0EC1H1R5C
5	1	730-13322	C5	CAP 0.47 uF 6.3V CERAMIC X5R 0402	Murata	GRM155R60J474KE19D
6	6	730-13404	C6,C7,C8, C9,C10, C11	CAP 0.047 uF 16V CERAMIC X5R 0402	AVX	0402YD473KAT2A
7	1	730-11953	C12	CAP 1500PF 50V CERAMIC X7R 0402	Kemet	C0402C152K5RACTU
8	1	730-13040	C13	CAP CERAMIC 4.7UF 6.3V XR5 0805	Kemet	C0805C475K9PACTU
9	1	730-12003	C14	CAP CER 2.2UF 10V 10% X7R 0805	Murata Electronics North America	GRM21BR71A225KA01L
10	1	800-13333	D1	LED GREEN/RED BICOLOR 1210 SMD	LITEON	LTST-C155KGJRKT
11	1	420-13046	J1	CONN USB PLUG TYPE A PCB SMT	ACON	UAR72-4N5J10
12	1	800-13401	L1	INDUCTOR 22NH 2% FIXED 0603 SMD	Panasonic - ECG	ELJ-RE22NGF2
13	1	800-11651	L2	INDUCTOR 1.8NH +-.3NH FIXED 0402 SMD	Panasonic - ECG	ELJ-RF1N8DF
14	2	610-10037	R1, R2	RES 24 OHM 1/16W 5% 0603 SMD	Panasonic - ECG	ERJ-3GEYJ240V
15	1	610-10343	R4	RES ZERO OHM 1/16W 0402 SMD	Panasonic - ECG	ERJ-2GE0R00X
16	3	610-10016	R5, R6, R7	RES CHIP 1K OHM 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ102X
17	2	610-13472	R9,R8	RES CHIP 620 OHM 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ621X
18	2	610-10684	R10, R11	RES CHIP 100 OHM 1/16W 5% 0402 SMD	Phycomp USA Inc	9C1A04021000FLHF3
19	1	200-13471	S1	SWITCH LT 3.5MMX2.9MM 160GF SMD	Panasonic - ECG	EVQ-P7J01K
20	1	CYRF7936-40LFC	U1	IC, 2.4 GHz CyFi Transceiver QFN-40	Cypress Semiconductor	CYRF7936 Rev A5
21	1	CY8C24794-24LF XI	U2	PSoC Mixed Signal Array	Cypress Semiconductor	CY8C24794-24LFXI
22	1	800-13259	Y1	CRYSTAL 12.00MHZ HC49 SMD	eCERA	GF-1200008
23	1		LABEL1	Serial Number	XXXXXX	

Register Descriptions

All registers are read and writable, except where noted. Registers may be written to or read from individually or in sequential groups.

Table 5. Register Map Summary

Address	Mnemonic	b7	b6	b5	b4	b3	b2	b1	b0	Default[1]	Access[1]
0x00	CHANNEL_ADR	Not Used	Channel							-1001000	-bbbbbbb
0x01	TX_LENGTH_ADR	TX Length								00000000	bbbbbbbb
0x02	TX_CTRL_ADR	TX GO	TX CLR	TXB15 IRQEN	TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN	00000011	bbbbbbbb
0x03	TX_CFG_ADR	Not Used	Not Used	DATA CODE LENGTH	DATA MODE		PA SETTING			--000101	--bbbbbb
0x04	TX_IRQ_STATUS_ADR	OS IRQ	LV IRQ	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXBERR IRQ	TXC IRQ	TXE IRQ	--------	rrrrrrrr
0x05	RX_CTRL_ADR	RX GO	RSVD	RXB16 IRQEN	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN	00000111	bbbbbbbb
0x06	RX_CFG_ADR	AGC EN	LNA	ATT	HILO	FAST TURN EN	Not Used	RXOW EN	VLD EN	10010-10	bbbbb-bb
0x07	RX_IRQ_STATUS_ADR	RXOW IRQ	SOPDET IRQ	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERR IRQ	RXC IRQ	RXE IRQ	--------	brrrrrrr
0x08	RX_STATUS_ADR	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode		--------	rrrrrrrr
0x09	RX_COUNT_ADR	RX Count								00000000	rrrrrrrr
0x0A	RX_LENGTH_ADR	RX Length								00000000	rrrrrrrr
0x0B	PWR_CTRL_ADR	PMU EN	LVIRQ EN	PMU Mode Force	PFET disable	LVI TH		PMU OUTV		10100000	bbb-bbbb
0x0C	XTAL_CTRL_ADR	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ			000--100	bbb--bbb
0x0D	IO_CFG_ADR	IRQ OD	IRQ POL	MISO OD	XOUT OD	PACTL OD	PACTL GPIO	SPI 3PIN	IRQ GPIO	00000000	bbbbbbbb
0x0E	GPIO_CTRL_ADR	XOUT OP	MISO OP	PACTL OP	IRQ OP	XOUT IP	MISO IP	PACTL IP	IRQ IP	0000----	bbbbrrrr
0x0F	XACT_CFG_ADR	ACK EN	Not Used	FRC END	END STATE			ACK TO		1-000000	b-bbbbbb
0x10	FRAMING_CFG_ADR	SOP EN	SOP LEN	LEN EN	SOP TH					10100101	bbbbbbbb
0x11	DATA32_THOLD_ADR	Not Used	Not Used	Not Used	Not Used	TH32				----0100	----bbbb
0x12	DATA64_THOLD_ADR	Not Used	Not Used	Not Used	TH64					---01010	---bbbbb
0x13	RSSI_ADR	SOP	Not Used	LNA	RSSI					0-100000	r-rrrrrr
0x14	EOP_CTRL_ADR	HEN	HINT			EOP				10100100	bbbbbbbb
0x15	CRC_SEED_LSB_ADR	CRC SEED LSB								00000000	bbbbbbbb
0x16	CRC_SEED_MSB_ADR	CRC SEED MSB								00000000	bbbbbbbb
0x17	TX_CRC_LSB_ADR	CRC LSB								--------	rrrrrrrr
0x18	TX_CRC_MSB_ADR	CRC MSB								--------	rrrrrrrr
0x19	RX_CRC_LSB_ADR	CRC LSB								11111111	rrrrrrrr
0x1A	RX_CRC_MSB_ADR	CRC MSB								11111111	rrrrrrrr
0x1B	TX_OFFSET_LSB_ADR	STRIM LSB								00000000	bbbbbbbb
0x1C	TX_OFFSET_MSB_ADR	Not Used	Not Used	Not Used	Not Used	STRIM MSB				----0000	----bbbb
0x1D	MODE_OVERRIDE_ADR	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST	00000--0	wwwww--w
0x1E	RX_OVERRIDE_ADR	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used	0000000-	bbbbbbb-
0x1F	TX_OVERRIDE_ADR	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV	00000000	bbbbbbbb
0x26	XTAL_CFG_ADR	RSVD	RSVD	RSVD	RSVD	START DLY	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x27	CLK_OVERRIDE_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x28	CLK_EN_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x29	RX_ABORT_ADR	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x32	AUTO_CAL_TIME_ADR	AUTO_CAL_TIME								00000011	wwwwwwww
0x35	AUTO_CAL_OFFSET_ADR	AUTO_CAL_OFFSET								00000000	wwwwwwww
0x39	ANALOG_CTRL_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RX INV	ALL SLOW	00000000	wwwwwwww
Register Files											
0x20	TX_BUFFER_ADR	TX Buffer File								--------	wwwwwwww
0x21	RX_BUFFER_ADR	RX Buffer File								--------	rrrrrrrr
0x22	SOP_CODE_ADR	SOP Code File								Note 2	bbbbbbbb
0x23	DATA_CODE_ADR	Data Code File								Note 3	bbbbbbbb
0x24	PREAMBLE_ADR	Preamble File								Note 4	bbbbbbbb
0x25	MFG_ID_ADR	MFG ID File								NA	rrrrrrrr

Notes
1. b = read/write; r = read only; w = write only; '-' = not used, default value is undefined.
2. SOP_CODE_ADR default = 0x17FF9E213690C782.
3. DATA_CODE_ADR default = 0x02F9939702FA5CE3012BF1DB0132BE6F.
4. PREAMBLE_ADR default = 0x333302. The count value must be great than 4 for DDR and greater than 8 for SDR
5. Registers must be configured or accessed only when the radio is in IDLE or SLEEP mode. The PMU, GPIOs, and RSSI registers can be accessed in Active Tx and Rx mode.
6. EOP_CTRL_ADR[6:4] must never have the value of "000", that is, EOP Hint Symbol count must never be "0"
7. PFET Bit: Setting this bit to "1" disables the FET, therefore safely allowing Vbat to be connected to a separate reference from Vcc when the PMU is disabled to the radio.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied.. –55°C to +125°C

Supply Voltage on any power supply pin relative to V_{SS} ....–0.3V to +3.9V

DC Voltage to Logic Inputs[8] .... –0.3V to V_{IO} +0.3V

DC Voltage applied to Outputs in High-Z State .... –0.3V to V_{IO} +0.3V

Static Discharge Voltage (Digital)[9] .... >2000V

Static Discharge Voltage (RF)[9] 1100V

Latch-Up Current ....+200 mA, –200 mA

Operating Conditions

V_{CC} ....2.4V to 3.6V

V_{IO} ....1.8V to 3.6V

V_{BAT} ....1.8V to 3.6V

T_A (Ambient Temperature Under Bias) .... 0°C to +70°C

Ground Voltage.. 0V

F_{OSC} (Crystal Frequency)............................ 12MHz ±30 ppm

DC Characteristics

(T = 25°C, V_{BAT} = 2.4V, PMU disabled, f_{OSC} = 12.000000 MHz)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	0–70°C	1.8		3.6	V
V_{REG}[10]	PMU Output Voltage	2.4V mode	2.4	2.43		V
V_{REG}[10]	PMU Output Voltage	2.7V mode	2.7	2.73		V
V_{IO}[11]	V_{IO} Voltage		1.8		3.6	V
V_{CC}	V_{CC} Voltage	0–70°C	2.4[12]		3.6	V
V_{OH1}	Output High Voltage Condition 1	At I_{OH} = –100.0 µA	V_{IO} – 0.2	V_{IO}		V
V_{OH2}	Output High Voltage Condition 2	At I_{OH} = –2.0 mA	V_{IO} – 0.4	V_{IO}		V
V_{OL}	Output Low Voltage	At I_{OL} = 2.0 mA		0	0.45	V
V_{IH}	Input High Voltage		$0.7V_{IO}$		V_{IO}	V
V_{IL}	Input Low Voltage		0		$0.3V_{IO}$	V
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{IO}$	–1	0.26	+1	µA
C_{IN}	Pin Input Capacitance	except XTAL, RF_N, RF_P, RF_{BIAS}		3.5	10	pF
I_{CC} (GFSK)[13]	Average TX I_{CC}, 1 Mbps, slow channel	PA = 5, 2 way, 4 bytes/10 ms		0.87		mA
I_{CC} (32-8DR)[13]	Average TX I_{CC}, 250 kbps, fast channel	PA = 5, 2 way, 4 bytes/10 ms		1.2		mA
I_{SB}[14]	Sleep Mode I_{CC}			0.8	10	µA
I_{SB}[14]	Sleep Mode I_{CC}	PMU enabled		31.4		µA
IDLE I_{CC}	Radio off, XTAL Active	XOUT disabled		1.0		mA
I_{synth}	I_{CC} during Synth Start			8.4		mA
TX I_{CC}	I_{CC} during Transmit	PA = 5 (–5 dBm)		20.8		mA
TX I_{CC}	I_{CC} during Transmit	PA = 6 (0 dBm)		26.2		mA
TX I_{CC}	I_{CC} during Transmit	PA = 7 (+4 dBm)		34.1		mA
RX I_{CC}	I_{CC} during Receive	LNA off, ATT on		18.4		mA
RX I_{CC}	I_{CC} during Receive	LNA on, ATT off		21.2		mA
Boost Eff	PMU Boost Converter Efficiency	V_{BAT} = 2.5V, V_{REG} = 2.73V, I_{LOAD} = 20 mA		81		%
I_{LOAD_EXT}	Average PMU External Load current	V_{BAT} = 1.8V, V_{REG} = 2.73V, 0–50°C, RX Mode			15	mA
I_{LOAD_EXT}	Average PMU External Load current	V_{BAT} = 1.8V, V_{REG} = 2.73V, 50–70°C, RX Mode			10	mA

Notes

8. It is permissible to connect voltages above V_{IO} to inputs through a series resistor limiting input current to 1 mA. AC timing not guaranteed.
9. Human Body Model (HBM).
10. V_{REG} depends on battery input voltage.
11. In sleep mode, the IO interface voltage reference is V_{BAT}.
12. In sleep mode, V_{CC} min. can be as low as 1.8V.
13. Includes current drawn while starting crystal, starting synthesizer, transmitting packet (including SOP and CRC16), changing to receive mode, and receiving ACK handshake. Device is in sleep except during this transaction.
14. ISB is not guaranteed if any IO pin is connected to voltages higher than V_{IO}.

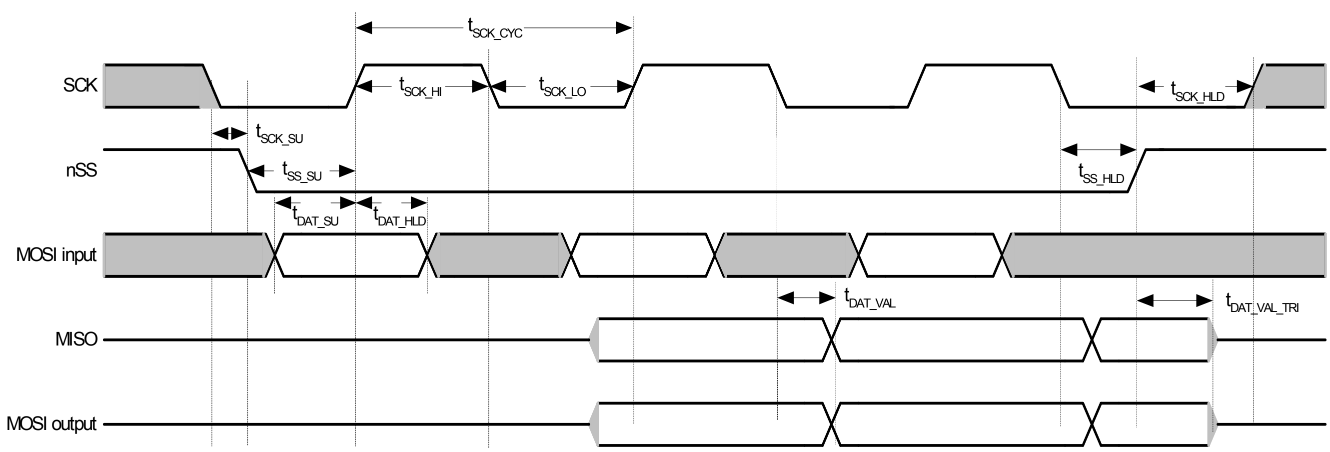
AC Characteristics

The AC Characteristics of CYRF7936 follow[12]

Table 6. SPI Interface[16]

Parameter	Description	Min	Typ	Max	Unit
t_{SCK_CYC}	SPI Clock Period	238.1			ns
t_{SCK_HI}	SPI Clock High Time	100			ns
t_{SCK_LO}	SPI Clock Low Time	100			ns
t_{DAT_SU}	SPI Input Data Setup Time	25			ns
t_{DAT_HLD}	SPI Input Data Hold Time	10			ns
t_{DAT_VAL}	SPI Output Data Valid Time	0		50	ns
$t_{DAT\_VAL\_TRI}$	SPI Output Data Tri-state (MOSI from Slave Select Deassert)			20	ns
t_{SS_SU}	SPI Slave Select Setup Time before first positive edge of SCK[17]	10			ns
t_{SS_HLD}	SPI Slave Select Hold Time after last negative edge of SCK	10			ns
t_{SS_PW}	SPI Slave Select Minimum Pulse Width	20			ns
t_{SCK_SU}	SPI Slave Select Setup Time	10			ns
t_{SCK_HLD}	SPI SCK Hold Time	10			ns
t_{RESET}	Minimum RST Pin Pulse Width	10			ns

Figure 11. SPI Timing



Notes

15. AC values are not guaranteed if voltage on any pin exceeding V_{IO}.
16. C_{LOAD} = 30 pF
17. SCK must start low at the time SS# goes LOW, otherwise the success of SPI transactions are not guaranteed.

RF Characteristics

Table 7. Radio Parameters

Parameter Description	Conditions	Min	Typ	Max	Unit
RF Frequency Range	Note 18	2.400		2.497	GHz
Receiver (T = 25°C, V_{CC} = 3.0V, f_{OSC} = 12.000000 MHz, BER < 1E-3)					
Sensitivity 125 kbps 64-8DR	BER 1E-3		–97		dBm
Sensitivity 250 kbps 32-8DR	BER 1E-3		–93		dBm
Sensitivity	CER 1E-3	–80	–87		dBm
Sensitivity GFSK	BER 1E-3, ALL SLOW = 1		–84		dBm
LNA Gain			22.8		dB
ATT Gain			–31.7		dB
Maximum Received Signal	LNA On	–15	–6		dBm
RSSI Value for PWR_{in} –60 dBm	LNA On		21		Count
RSSI Slope			1.9		dB/Count
Interference Performance (CER 1E-3)					
Co-channel Interference rejection Carrier-to-Interference (C/I)	C = –60 dBm		9		dB
Adjacent (±1 MHz) channel selectivity C/I 1 MHz	C = –60 dBm		3		dB
Adjacent (±2 MHz) channel selectivity C/I 2 MHz	C = –60 dBm		–30		dB
Adjacent (≥ 3 MHz) channel selectivity C/I ≥ 3 MHz	C = –67 dBm		–38		dB
Out-of-Band Blocking 30 MHz–12.75 MHz[19]	C = –67 dBm		–30		dBm
Intermodulation	C = –64 dBm, Δf = 5,10 MHz		–36		dBm
Receive Spurious Emission					
800 MHz	100 kHz ResBW		–79		dBm
1.6 GHz	100 kHz ResBW		–71		dBm
3.2 GHz	100 kHz ResBW		–65		dBm
Transmitter (T = 25°C, V_{CC} = 3.0V)					
Maximum RF Transmit Power	PA = 7	+2	4	+6	dBm
Maximum RF Transmit Power	PA = 6	–2	0	+2	dBm
Maximum RF Transmit Power	PA = 5	–7	–5	–3	dBm
Maximum RF Transmit Power	PA = 0		–35		dBm
RF Power Control Range			39		dB
RF Power Range Control Step Size	Seven steps, monotonic		5.6		dB
Frequency Deviation Min	PN Code Pattern 10101010		270		kHz
Frequency Deviation Max	PN Code Pattern 11110000		323		kHz
Error Vector Magnitude (FSK error)	>0 dBm		10		%rms
Occupied Bandwidth	–6 dBc, 100 kHz ResBW	500	876		kHz
Transmit Spurious Emission (PA = 7)					
In-band Spurious Second Channel Power (±2 MHz)			–38		dBm
In-band Spurious Third Channel Power (≥3 MHz)			–44		dBm

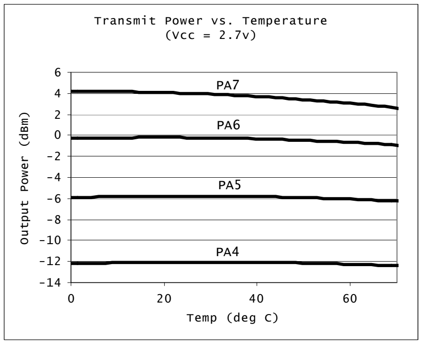
Notes
18. Subject to regulation.
19. Exceptions F/3 & 5C/3.

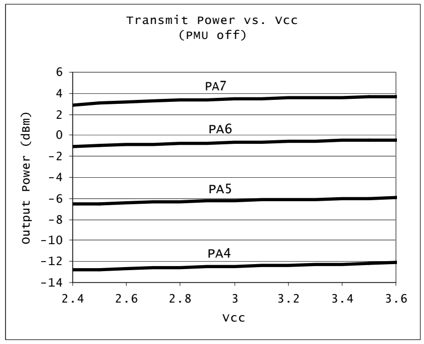
Table 7. Radio Parameters (continued)

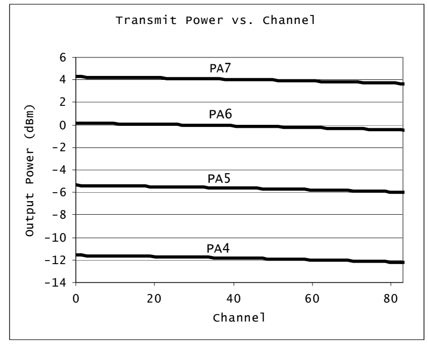
Parameter Description	Conditions	Min	Typ	Max	Unit
Non-Harmonically Related Spurs (800 MHz)			–38		dBm
Non-Harmonically Related Spurs (1.6 GHz)			–34		dBm
Non-Harmonically Related Spurs (3.2 GHz)			–47		dBm
Harmonic Spurs (Second Harmonic)			–43		dBm
Harmonic Spurs (Third Harmonic)			–48		dBm
Fourth and Greater Harmonics			–59		dBm
Power Management (Crystal PN# eCERA GF-1200008)					
Crystal Start to 10ppm			0.7	1.3	ms
Crystal Start to IRQ	XSIRQ EN = 1		0.6		ms
Synth Settle	Slow channels			270	µs
Synth Settle	Medium channels			180	µs
Synth Settle	Fast channels			100	µs
Link Turnaround Time	GFSK			30	µs
Link Turnaround Time	250 kbps			62	µs
Link Turnaround Time	125 kbps			94	µs
Link Turnaround Time	<125 kbps			31	µs
Max Packet Length	<60 ppm crystal-to-crystal			40	bytes

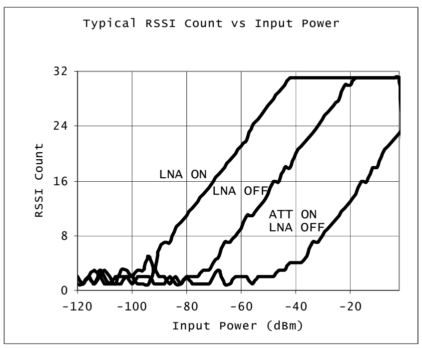
Typical Operating Characteristics

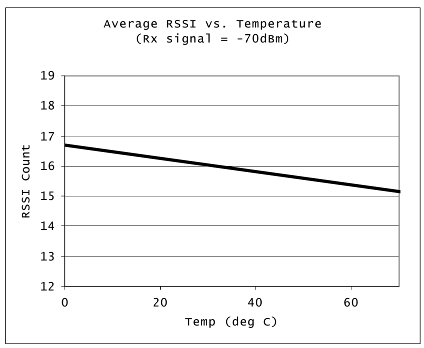
The typical operating characteristics of CYRF7936 follow[20]

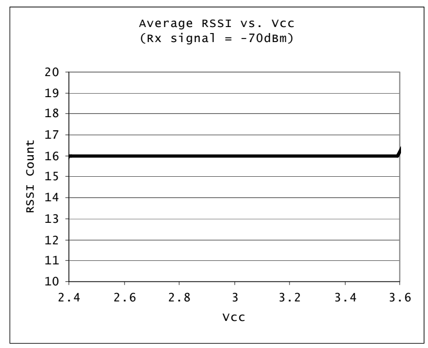


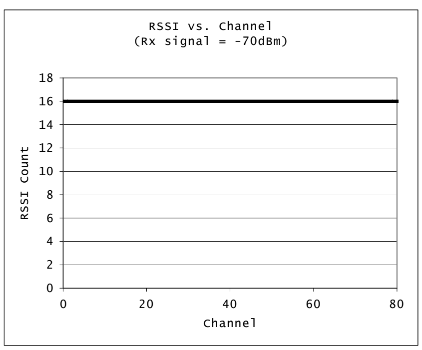


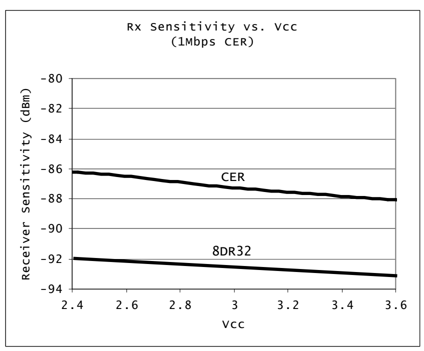


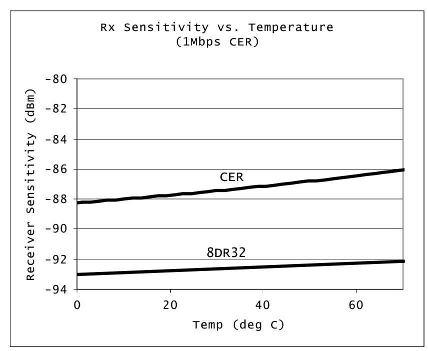


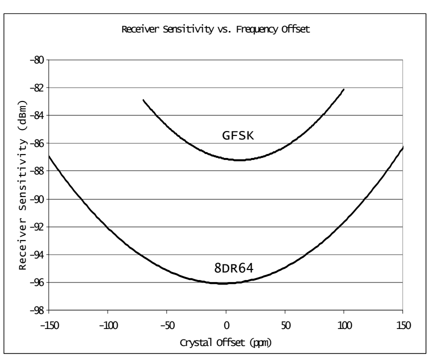


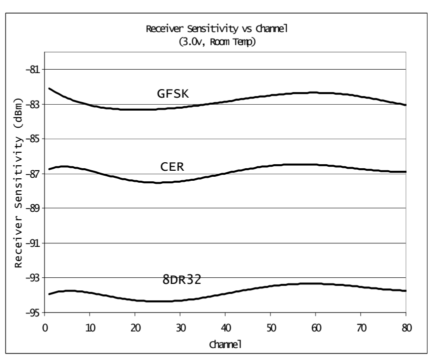


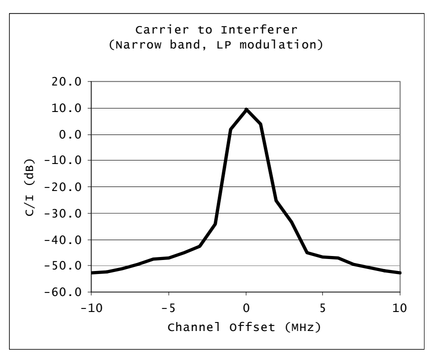








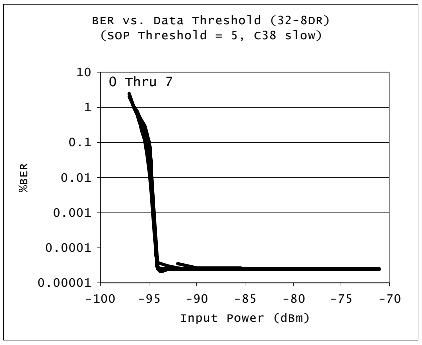


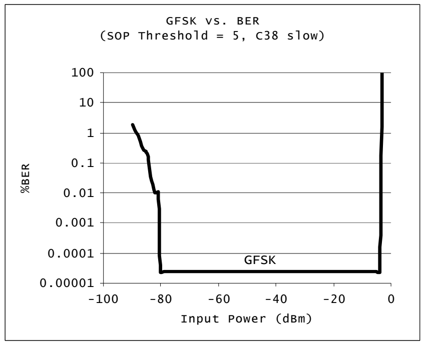


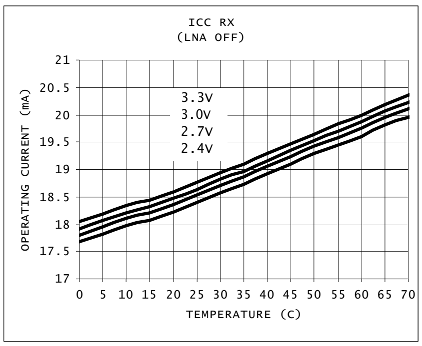
Note

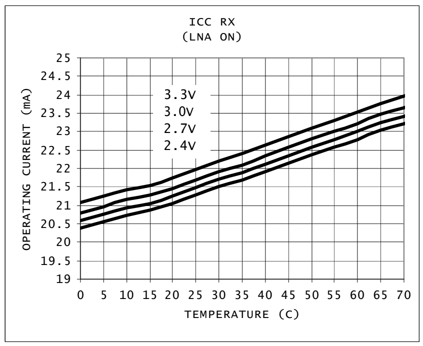
20. With LNA on, ATT off, above -2dBm erroneous RSSI values may be read. Cross-checking RSSI with LNA off/on is recommended for accurate readings.

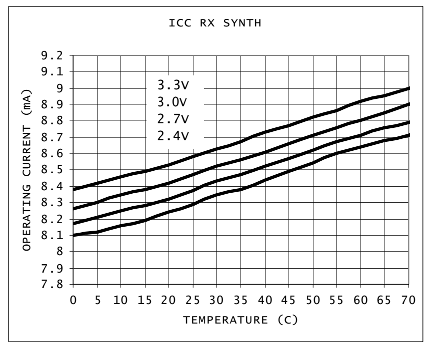
Typical Operating Characteristics (continued)

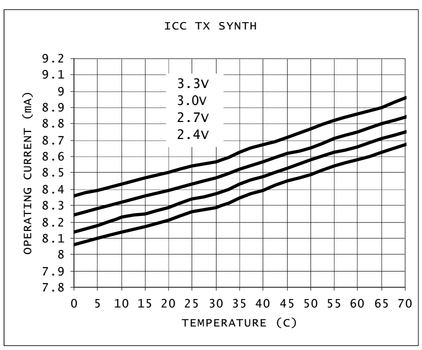


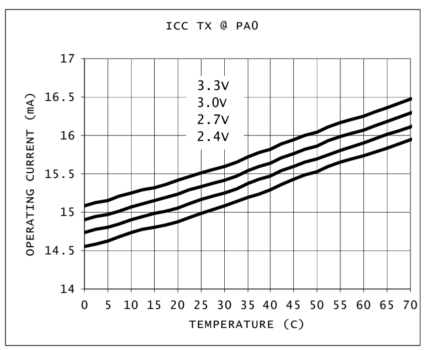


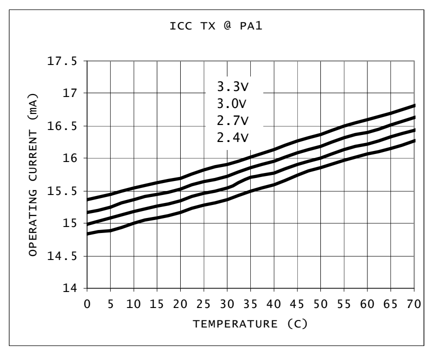


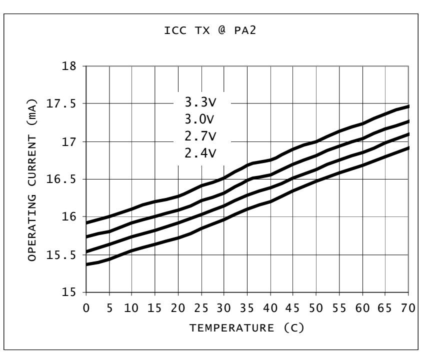


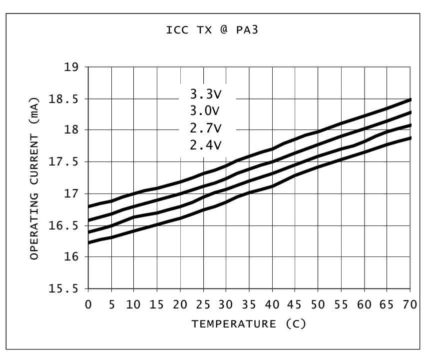


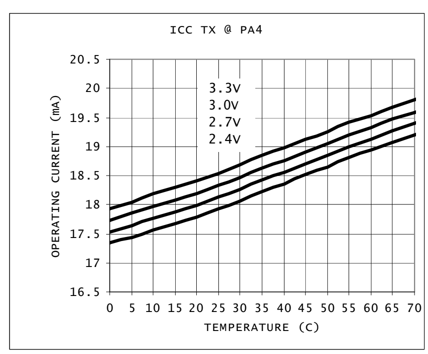




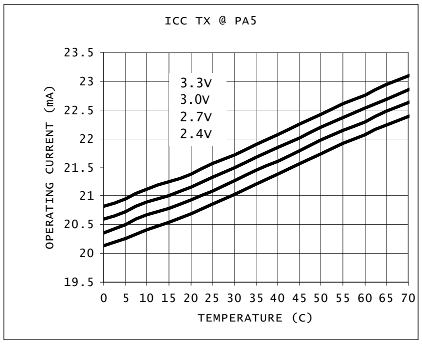


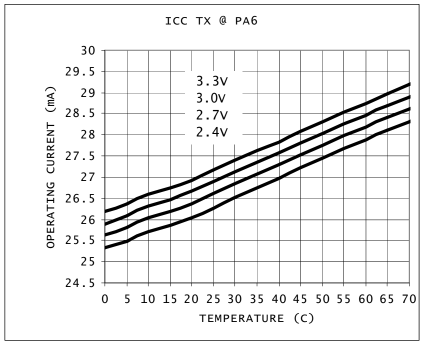


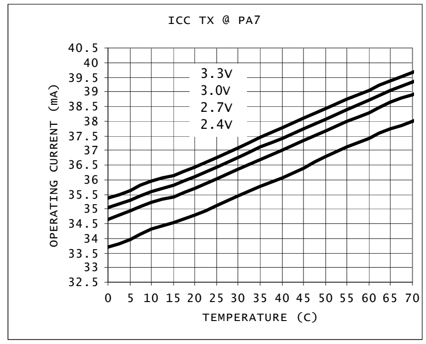




Typical Operating Characteristics (continued)

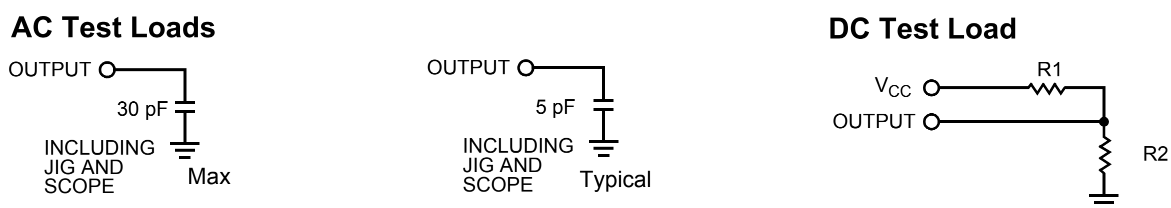




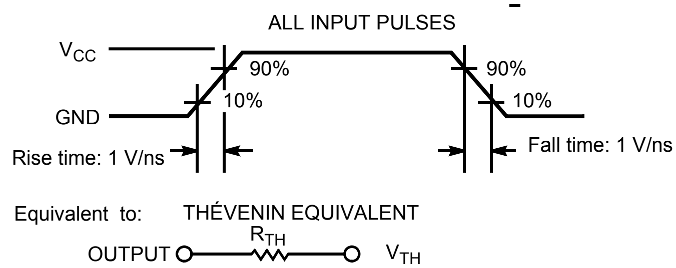


AC Test Loads and Waveforms for Digital Pins

Figure 12. AC Test Loads and Waveforms for Digital Pins



Parameter		Unit
R1	1071	Ω
R2	937	Ω
R_{TH}	500	Ω
V_{TH}	1.4	V
V_{CC}	3.00	V



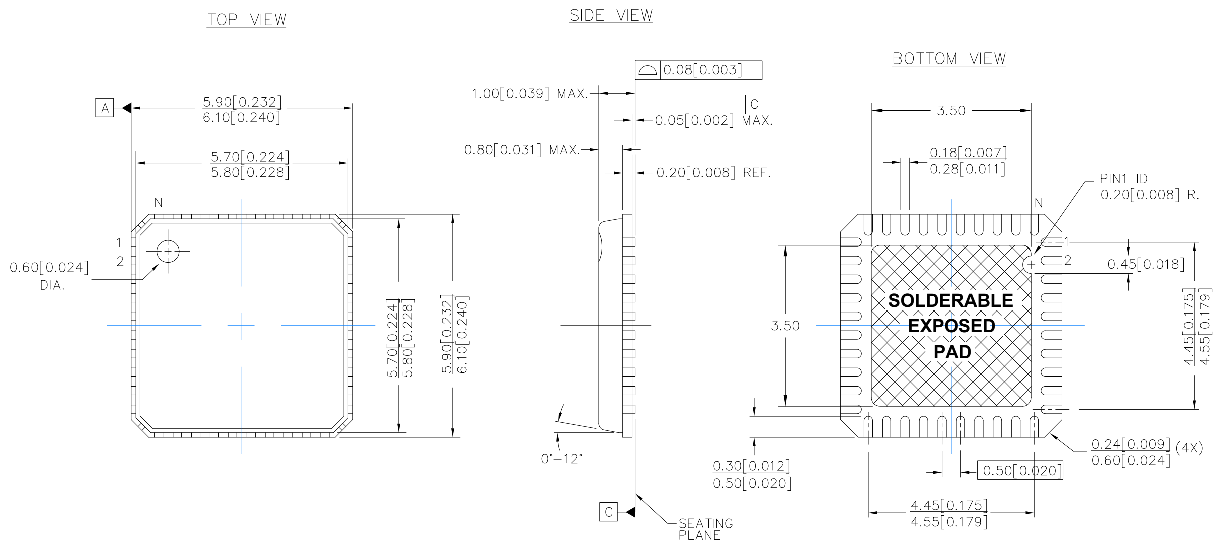
Ordering Information

Table 8. Ordering Information

Part Number	Radio	Package Name	Package Type	Operating Range
CYRF7936-40LFXC	Transceiver	40 QFN	40 Quad Flat Package No Leads Pb-Free CYRF7936	Commercial

Package Description

Figure 13. 40-Pin Pb-Free QFN 6 x 6 mm LY40



NOTES:

1. HATCH IS SOLDERABLE EXPOSED AREA
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.086g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

(SUBCON Punch Type PKG WITH 3.50X3.50 EPAD)

PART #	DESCRIPTION
LF40A	STANDARD
LY40A	PB-FREE

001-12917 *A

The recommended dimension of the PCB pad size for the E-PAD underneath the QFN is 3.5 mm × 3.5 mm (width x length).

Document History Page

Description Title: CYRF7936 2.4 GHz CyFi™ Transceiver Document #: 001-48013 Rev. **				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2557501	KKU/AESA	09/10/08	New Data Sheet

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