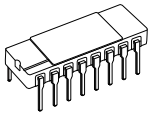
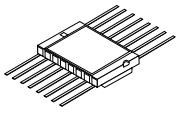
M54HC4053

RAD-HARD TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

- LOW POWER DISSIPATION:
  I_{CC} = 4μA(MAX.) at T_A=25°C
- LOGIC LEVEL TRANSLATION TO ENABLE 5V LOGIC SIGNAL TO COMMUNICATE WITH ±5V ANALOG SIGNAL
- LOW "ON" RESISTANCE:
  70Ω TYP. (V_{CC} - V_{EE} = 4.5V)
  50Ω TYP. (V_{CC} - V_{EE} = 9V)
- WIDE ANALOG INPUT VOLT. RANGE: ±6V
- FAST SWITCHING:
  t_{pd} = 15ns (TYP.) at T_A = 25 °C
- LOW CROSSTALK BETWEEN SWITCHES
- HIGH ON/OFF OUTPUT VOLTAGE RATIO
- WIDE OPERATING SUPPLY VOLTAGE RANGE (V_{CC} - V_{EE}) = 2V TO 12V
- LOW SINE WAVE DISTORTION:
  0.02% at V_{CC} - V_{EE} = 9V
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 4053
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9408-065



DILC-16



FPC-16

ORDER CODES

PACKAGE	FM	EM
DILC	M54HC4053D	M54HC4053D1
FPC	M54HC4053K	M54HC4053K1

DESCRIPTION

The M54HC4053 is a triple two-channel analog MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology and it is pin to pin compatible with the equivalent metal gate CMOS4000B series.

It contains 6 bidirectional and digitally controlled analog switches.

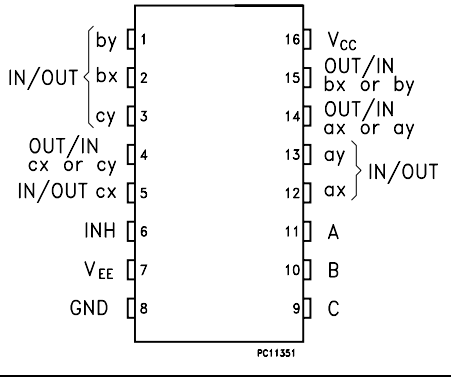
A built-in level shifting is included to allow an input range up to ±6V (peak) for an analog signal with digital control signal of 0 to 6V.

V_{EE} supply pin is provided for analog input signals. It has an inhibit (INH) input terminal to disable all the switches when high. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND.

A, B and C control inputs select one of a pair of channels.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION



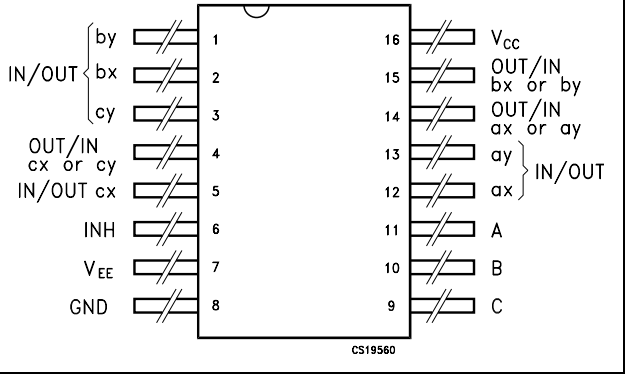


Figure 1: IEC Logic Symbols

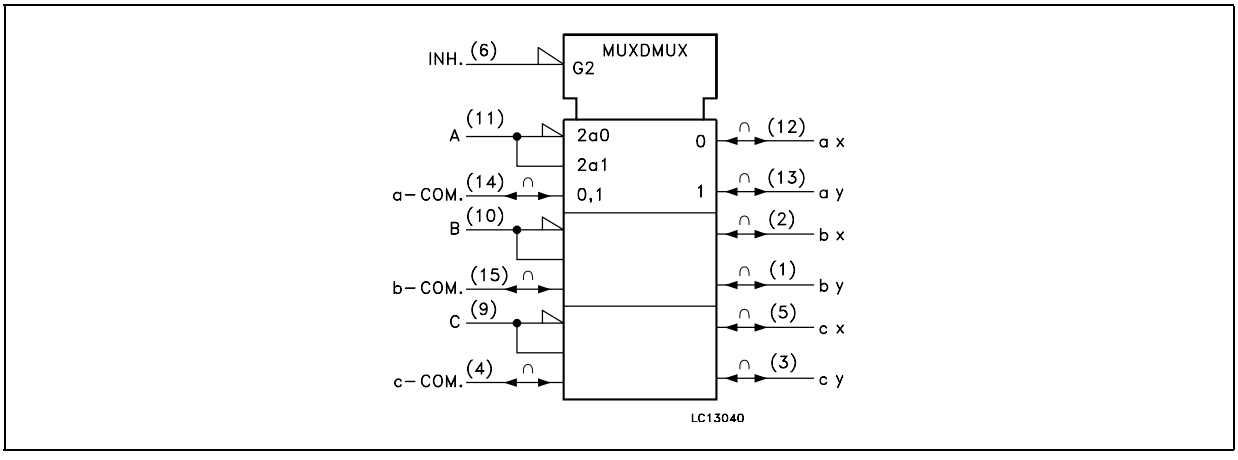


Figure 2: Control Input Equivalent Circuit

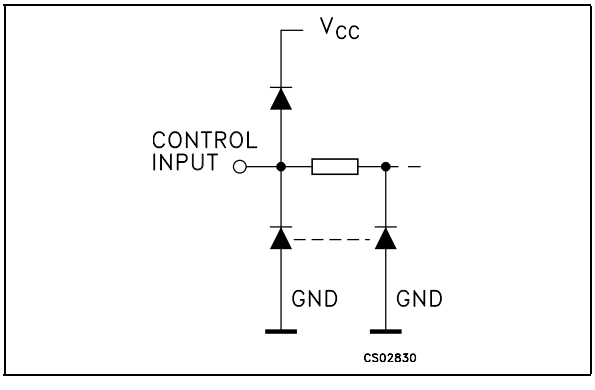


Figure 3: I/O Equivalent Circuit

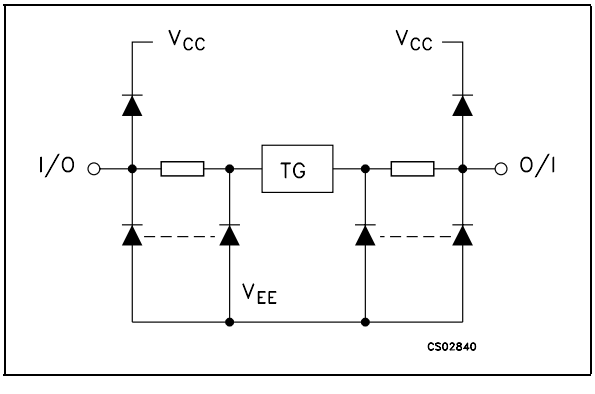


Table 1: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
2, 1	bx, by	Independent Input Outputs
5, 3	cx, cy	Independent Input Outputs
6	INH	INHIBIT Input
7	V_{EE}	Negative Supply Voltage
11, 10, 9	A, B, C	Select Inputs
12, 13	ax, ay	Independent Input Outputs
14, 15, 4	ax to cy	Common Output/Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUT STATE		ON CHANNEL
INH	A or B or C	
L	L	ax or bx or cx
L	H	ay or by or cy
H	X	NONE

X: Don't care

Figure 4: Functional Diagram

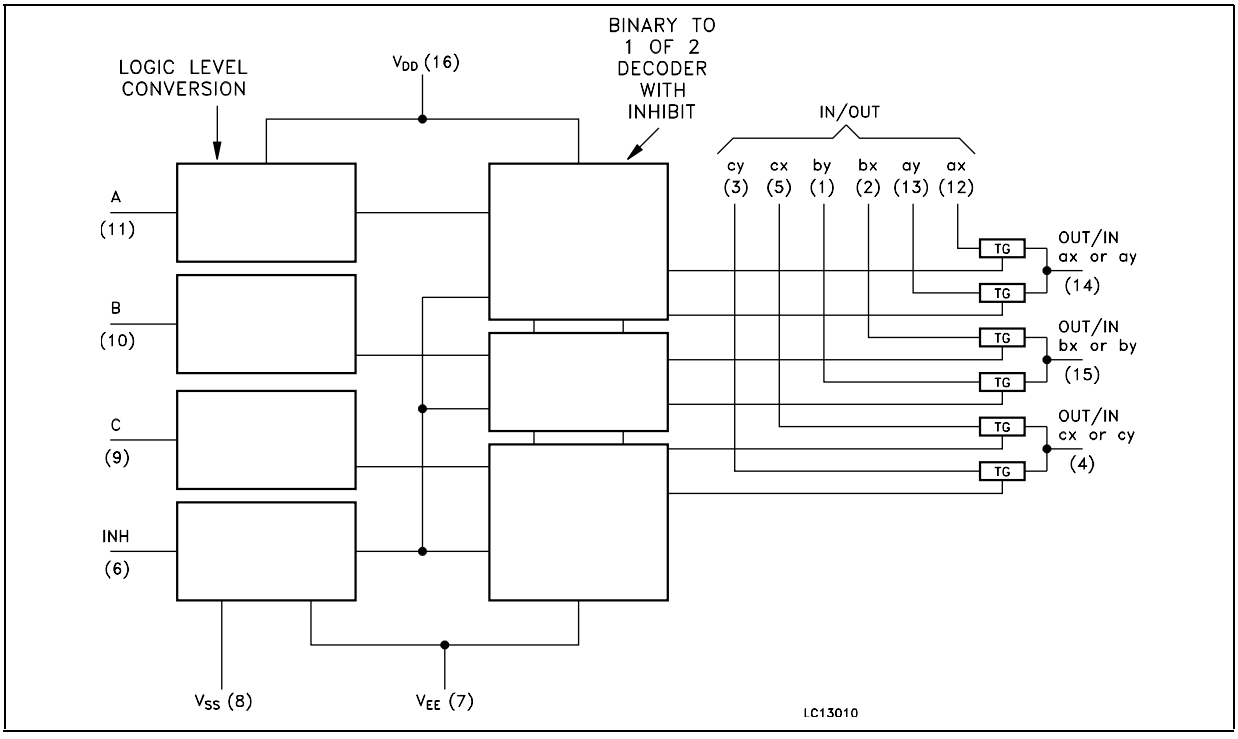


Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_{CC} - V_{EE}	Supply Voltage	-0.5 to +13	V
V_I	Control Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	Switch I/O Voltage	V_{EE} -0.5 to V_{CC} + 0.5	V
I_{CK}	Control Input Diode Current	± 20	mA
I_{IOK}	I/O Diode Current	± 20	mA
I_T	Switch Through Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_{EE}	Supply Voltage		-6 to 0	V
V_{CC} - V_{EE}	Supply Voltage		2 to 12	V
V_I	Input Voltage		0 to V_{CC}	V
$V_{I/O}$	I/O Voltage		V_{EE} to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	
		V_{CC} = 6.0V	0 to 400	

Table 5: DC Specifications

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{ILC}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
R_{ON}	ON Resistance	4.5	GND	V_I = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq$ 2mA		85	180		225		270	Ω
		4.5	-4.5			55	120		150		180	
		6.0	-6.0			50	100		125		150	
		2.0	GND	V_I = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq$ 2mA		150						
		4.5	GND			70	150		190		230	
		4.5	-4.5			50	100		125		150	
		6.0	-6.0			45	80		100		120	
ΔR_{ON}	Difference of ON Resistance between switches	4.5	GND	V_I = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq$ 2mA		10	30		35		45	Ω
		4.5	-4.5			5	12		15		18	
		6.0	-6.0			5	10		12		15	
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	6.0	GND	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_I = V_{ILC} or V_{IHC}			±0.06		± 0.6		± 1.2	µA
		6.0	-6.0				± 0.1		± 1		± 2	
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	6.0	GND	V_{OS} = V_{CC} or GND V_I = V_{IHC} or V_{ILC}			±0.06		± 0.6		± 1.2	µA
		6.0	-6.0				± 0.1		± 1		± 2	
I_I	Input Leakage Current	6.0	GND	V_I = V_{CC} or GND			± 0.1		± 0.1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	GND	V_I = V_{CC} or GND			4		40		80	µA
		6.0	-6.0				8		80		160	

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\Phi_{I/O}$	Phase Difference Between Input and Output	2.0	GND			25	60		75		90	ns
		4.5	GND			6	12		15		18	
		6.0	GND			5	10		13		15	
		4.5	-4.5			4						
t_{PZL} t_{PZH}	Output Enable Time	2.0	GND	R_L = 1KΩ		50	225		280		340	ns
		4.5	GND			14	45		56		68	
		6.0	GND			12	38		48		58	
		4.5	-4.5			14						
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	GND	R_L = 1KΩ		95	225		280		340	ns
		4.5	GND			30	45		56		68	
		6.0	GND			26	38		48		58	
		4.5	-4.5			26						

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0				5	10		10		10	pF
$C_{I/O}$	Common Terminal Capacitance	5.0	-5.0			11	20		20		20	pF
$C_{I/O}$	Switch Terminal Capacitance	5.0	-5.0			7	15		15		15	pF
C_{IOS}	Feed Through Capacitance	5.0	-5.0			0.75	2		2		2	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	GND			67						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

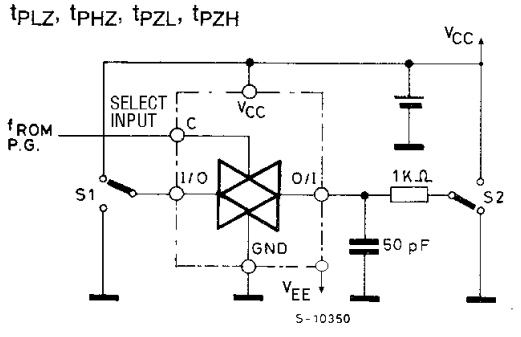
Table 8: Analog Switch Characteristics (GND = 0V;T_A = 25°C)

Symbol	Parameter	Test Condition				Value	Unit
		V_{CC} (V)	V_{EE} (V)	V_{IN} (V_{p-p})		Typ.	
	Sine Wave Distortion	2.25	-2.25	4	f_{IN} = 1 KHz R_L = 10 KΩ, C_L = 50 pF	0.025	%
		4.5	-4.5	8		0.020	
		6.0	-6.0	11		0.018	
f_{MAX}	Frequency Response (Switch ON) (*)	2.25	-2.25	Adjust f_{IN} voltage to obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB meter reads -3dB R_L = 50Ω, C_L = 10 pF, f_{IN} = 1KHz sine wave		120	MHz
		4.5	-4.5			190	
		6.0	-6.0			200	
f_{MAX}	Frequency Response (Switch ON) (**)	2.25	-2.25	Adjust f_{IN} voltage to obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB meter reads -3dB R_L = 50Ω, C_L = 10 pF, f_{IN} = 1KHz sine wave		95	MHz
		4.5	-4.5			150	
		6.0	-6.0			190	
	Feed through Attenuation (Switch OFF)	2.25	-2.25	V_{IN} is centered at (V_{CC} - V_{EE})/2 Adjust input for 0 dBm R_L = 600Ω, C_L = 50 pF, f_{IN} = 1KHz sine wave		-50	dB
		4.5	-4.5			-50	
		6.0	-6.0			-50	
	Crosstalk (Control Input to Signal Output)	2.25	-2.25	Adjust R_L at set up so that I_S = 0A. R_L = 600Ω, C_L = 50 pF, f_{IN} = 1KHz square wave		60	mV
		4.5	-4.5			140	
		6.0	-6.0			200	
	Crosstalk (between any two Switches)	2.25	-2.25	Adjust V_{IN} to obtain 0dBm at input R_L = 600Ω, C_L = 50 pF, f_{IN} = 1KHz sine wave		-50	dB
		4.5	-4.5			-50	
		6.0	-6.0			-50	

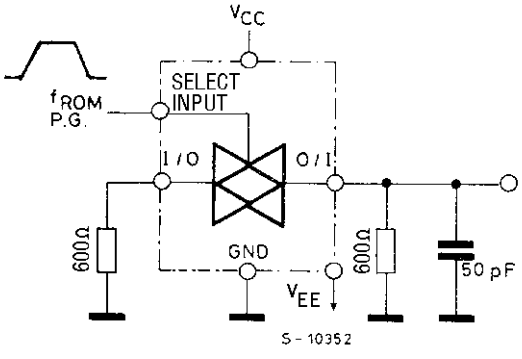
(*) Input COMMON Terminal, and measured at SWITCH Terminal
(**) Input SWITCH Terminal, and measured at common Terminal
NOTE: These characteristics are determined by the design of the device.

Figure 5: Switching Characteristics Test Circuit

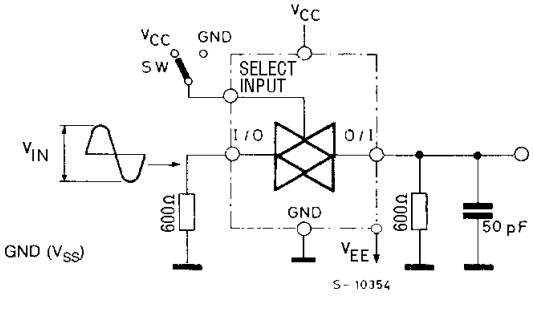
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}



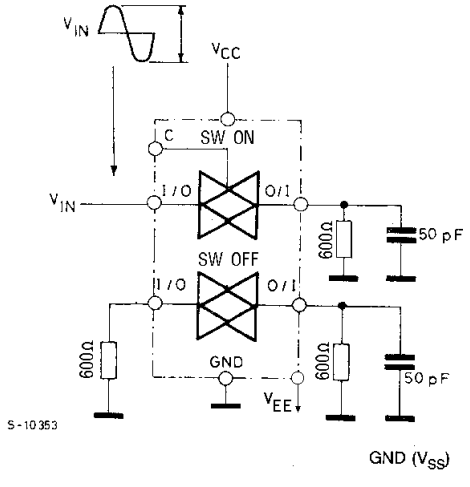
CROSSTALK (control to output)



BANDWIDTH AND FEEDTHROUGH ATTENUATION



CROSSTALK BETWEEN ANY TWO SWITCHES



C_{I-O}, $C_{I/O}$

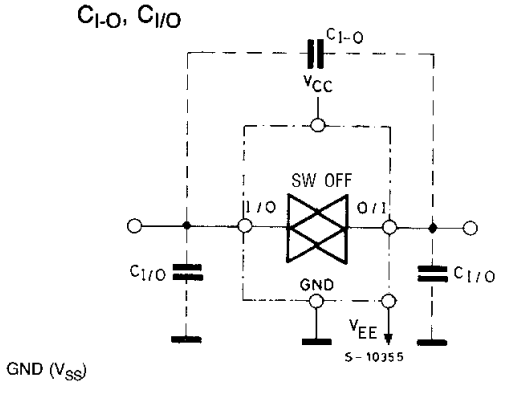


Figure 6: Switching Characteristics Waveform

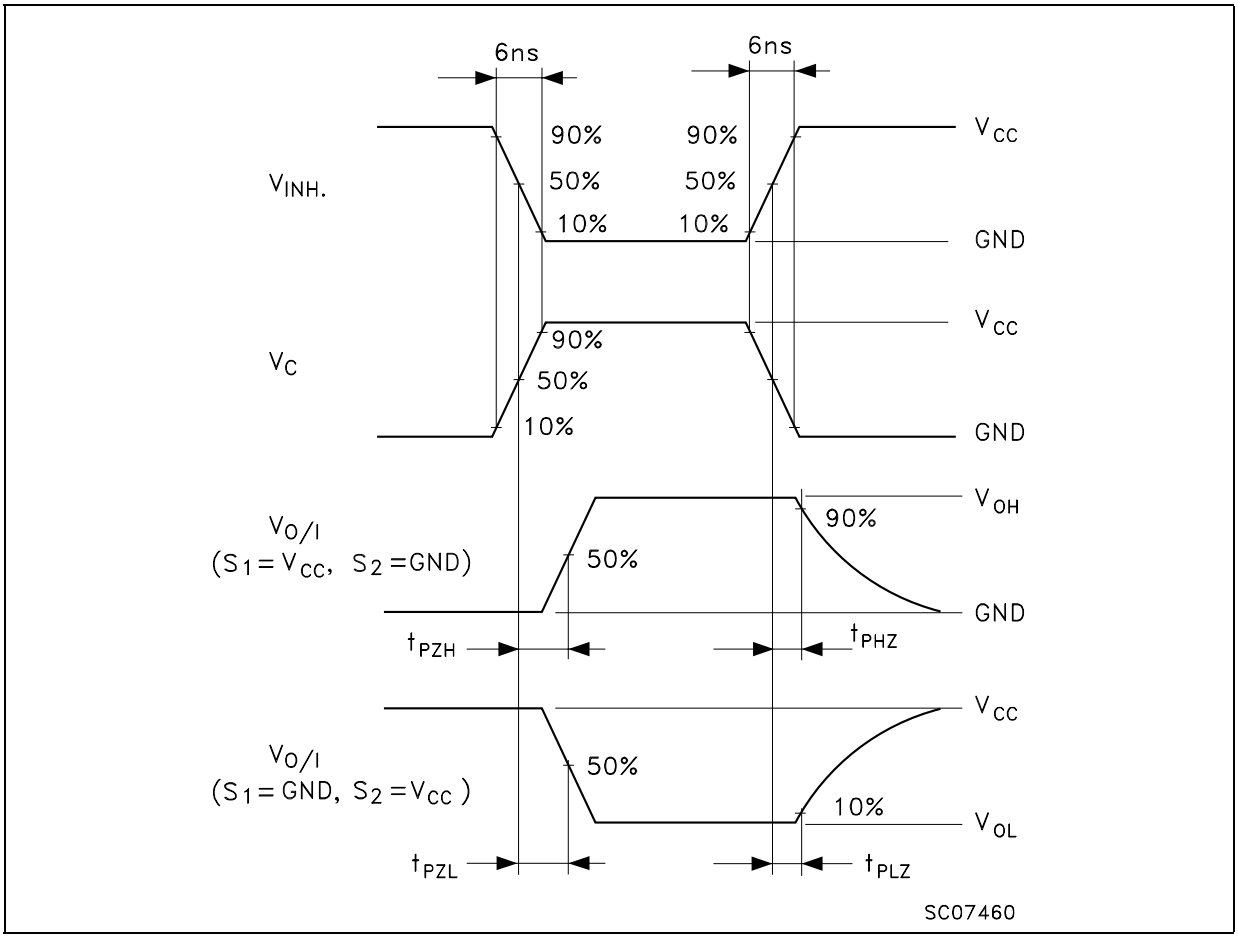


Figure 7: Channel Resistance (R_{ON})

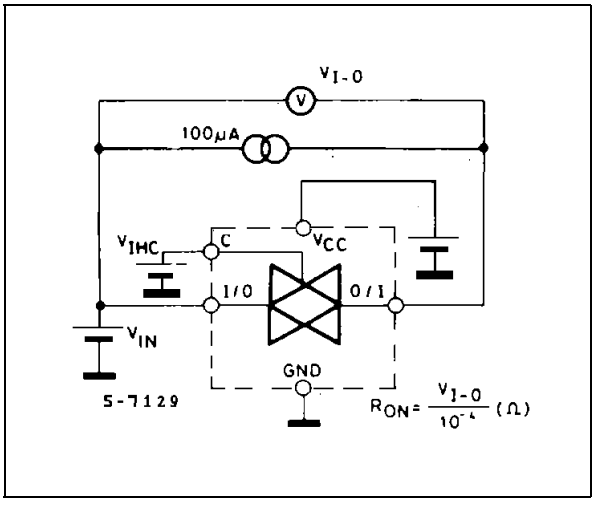
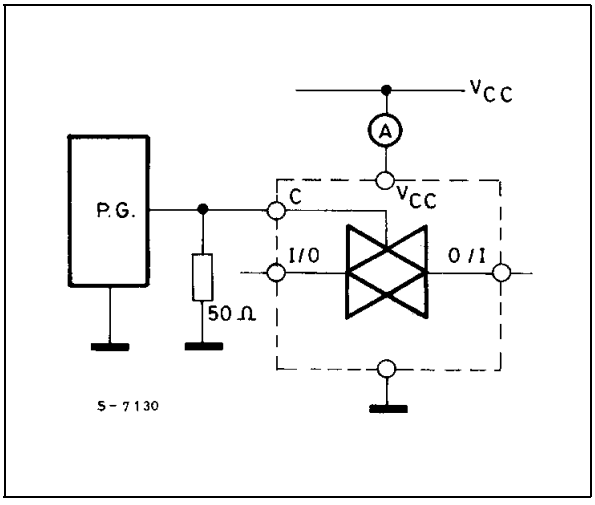
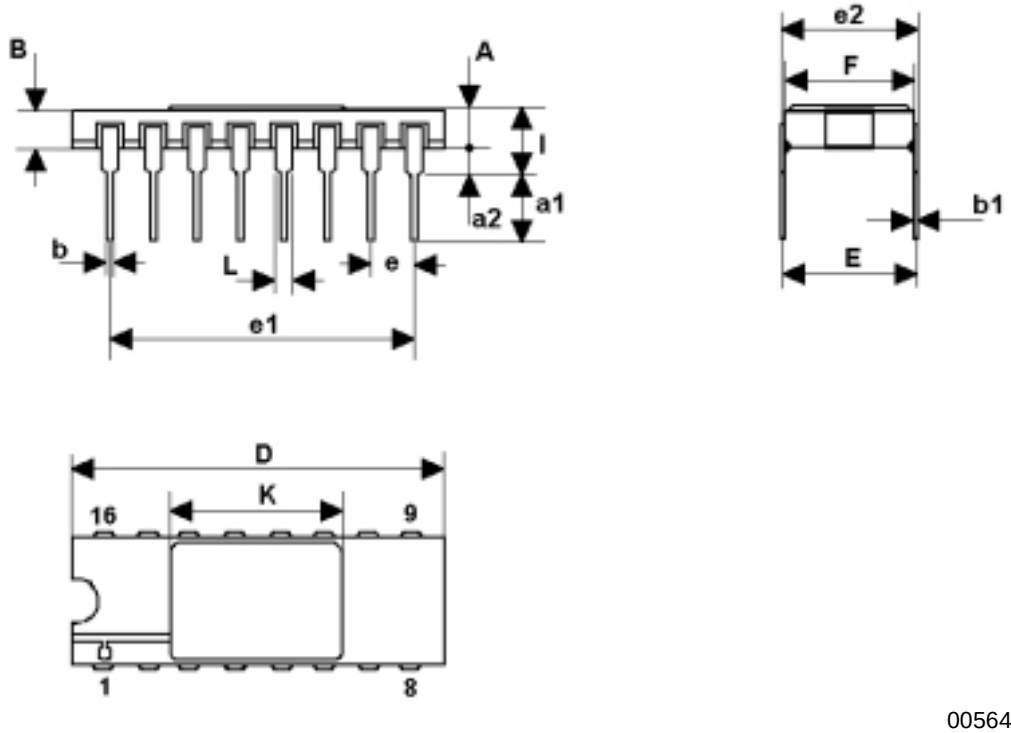


Figure 8: I_{CC} (Opr.)



DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	17.65	17.78	17.90	0.695	0.700	0.705
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	

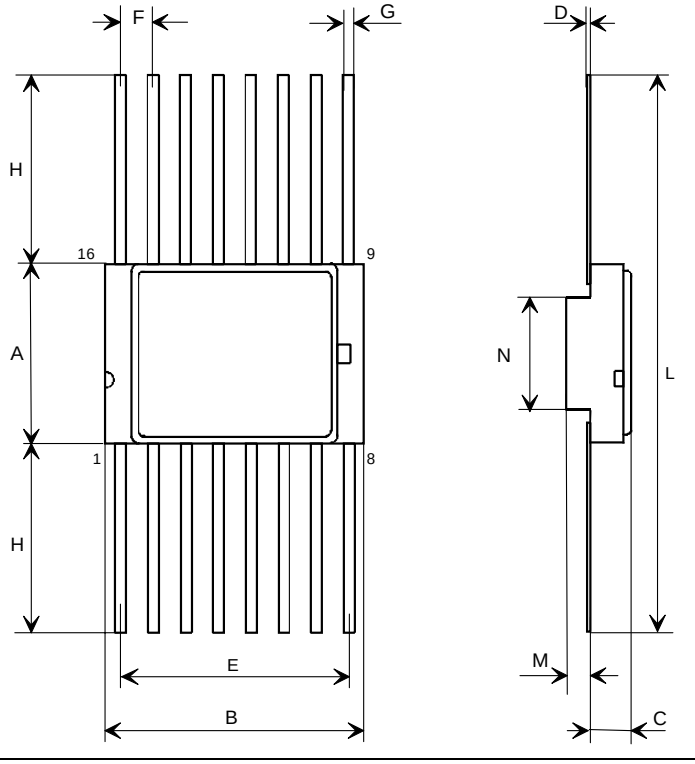

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Table 9: Revision History

Date	Revision	Description of Changes
15-May-2004	1	First Release