Thyristor/Diode and Thyristor/Thyristor, 135 A to 160 A (New INT-A-PAK™ Power Modules)

New INT-A-PAK™

FEATURES

- High voltage
- Electrically isolated by DBC ceramic (Al_2O_3)
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- High surge capability
- Glass passivated chips
- Modules uses high voltage power thyristor/diodes in three basic configurations
- Simple mounting
- UL E78996 approved
- Totally lead (Pb)-free
- Designed and qualified for multiple level

RoHS COMPLIANT

APPLICATIONS

- DC motor control and drives
- Battery charges
- Welders
- Power converters
- Lighting control
- Heat and temperature control

PRODUCT SUMMARY	
$I_{T(AV)}$	135 to 160 A

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VSK.136..	VSK.142..	VSK.162..	UNITS
$I_{T(AV)}$	85 °C	135	140	160	A
$I_{T(RMS)}$		300	310	355	A
I_{TSM}	50 Hz	3200	4500	4870	A
	60 Hz	3360	4712	5100	A
I^2t	50 Hz	51.5	102	119	kA^2s
	60 Hz	47	92.5	108	kA^2s
$I^2\sqrt{t}$		515.5	1013	1190	$kA^2\sqrt{s}$
V_{RRM}	Range	400 to 1600			V
T_J	Range	- 40 to 125			°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
VSK.136 VSK.142 VSK.162	04	400	500	50
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

FORWARD CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VSK.136	VSK.142	VSK.162	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			135	140	160	A
					85	85	85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch			300	310	355	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial T_J = T_J maximum	3200	4500	4870	
		t = 8.3 ms			3360	4712	5100	
		t = 10 ms	100 % V_{RRM} reapplied		2700	3785	4100	
		t = 8.3 ms			2800	3963	4300	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		51.5	102	119	kA^2s
		t = 8.3 ms			47	92.5	108	
		t = 10 ms	100 % V_{RRM} reapplied		36.5	71.6	84	
		t = 8.3 ms			33.3	65.4	76.7	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			515.5	1013	1190	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J maximum			0.86	0.83	0.8	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), T_J maximum			1.05	1	0.98	
Low level value on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J maximum			2.02	1.78	1.67	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), T_J maximum			1.65	1.43	1.38	
Maximum on-state voltage drop	V_{TM}	I_{TM} = π x $I_{T(AV)}$, T_J = 25 °C, 180° conduction			1.57	1.55	1.54	V
Maximum forward voltage drop	V_{FM}	I_{TM} = π x $I_{T(AV)}$, T_J = 25 °C, 180° conduction			1.57	1.55	1.54	V
Maximum holding current	I_H	Anode supply = 6 V initial I_T = 30 A, T_J = 25 °C			200			mA
Maximum latching current	I_L	Anode supply = 6 V resistive load = 1 Ω Gate pulse: 10 V, 100 µs, T_J = 25 °C			400			

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	t_{gd}	T_J = 25 °C	Gate current = 1 A, dI_g/dt = 1 A/µs V_d = 0.67 % V_{DRM}	1	µs
Typical rise time	t_{gr}			2	
Typical turn-off time	t_q	I_{TM} = 300 A, - dI/dt = 15 A/µs; T_J = T_J maximum V_R = 50 V; dV/dt = 20 V/µs; gate 0 V, 100 Ω		50 to 200	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	T_J = 125 °C	50	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted, t = 1 s	3500	V
Critical rate of rise of off-state voltage	dV/dt	T_J = T_J maximum, exponential to 67 % rated V_{DRM}	1000	V/µs

Thyristor/Diode and Thyristor/Thyristor, 135 A to 160 A
(New INT-A-PAK™ Power Modules)

TRIGGERING					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**VALUES**	**UNITS**
Maximum peak gate power	P_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		12	W
Maximum average gate power	$P_{G(AV)}$	f = 50 Hz, $T_J = T_J$ maximum		3	
Maximum peak gate current	I_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		3	A
Maximum peak negative gate voltage	$-V_{GT}$			10	V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = - 40 °C	Anode supply = 6 V, resistive load; R_a = 1 Ω	4	
		T_J = 25 °C		2.5	
		$T_J = T_J$ maximum		1.7	
Maximum required DC gate current to trigger	I_{GT}	T_J = - 40 °C		270	mA
		T_J = 25 °C		150	
		$T_J = T_J$ maximum		80	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied		0.3	V
Maximum gate current that will not trigger	I_{GD}			10	mA
Maximum rate of rise of turned-on current	dI/dt	$T_J = T_J$ maximum, I_{TM} = 400 A rated V_{DRM} applied		300	A/µs

THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**		**UNITS**
Maximum junction operating temperature range	T_J		- 40 to 125		°C
Maximum storage temperature range	T_{Stg}		- 40 to 150		
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.18	0.16	K/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface, smooth, flat and greased	0.05		
Mounting torque ± 10 % — IAP to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6		Nm
Mounting torque ± 10 % — busbar to IAP					
Approximate weight			200		g
			7.1		oz.
Case style			New INT-A-PAK		

ΔR CONDUCTION PER JUNCTION											
DEVICES	**SINUSOIDAL CONDUCTION AT T_J MAXIMUM**					**RECTANGULAR CONDUCTION AT T_J MAXIMUM**					**UNITS**
	180°	**120°**	**90°**	**60°**	**30°**	**180°**	**120°**	**90°**	**60°**	**30°**	
VSK.136	0.007	0.01	0.013	0.0155	0.017	0.009	0.012	0.014	0.015	0.017	K/W
VSK.142	0.0019	0.0019	0.0020	0.0020	0.0021	0.0018	0.0022	0.0023	0.0023	0.0020	
VSK.162	0.0030	0.0031	0.0032	0.0033	0.0034	0.0029	0.0036	0.0039	0.0041	0.0040	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

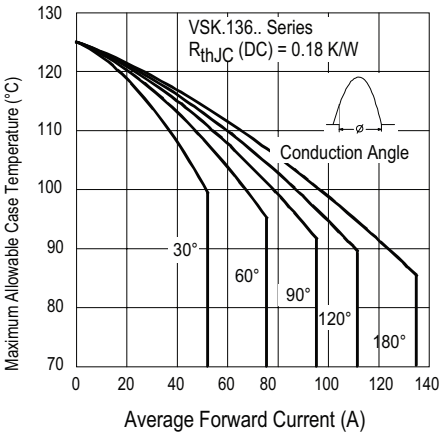


Fig. 1 - Current Ratings Characteristics

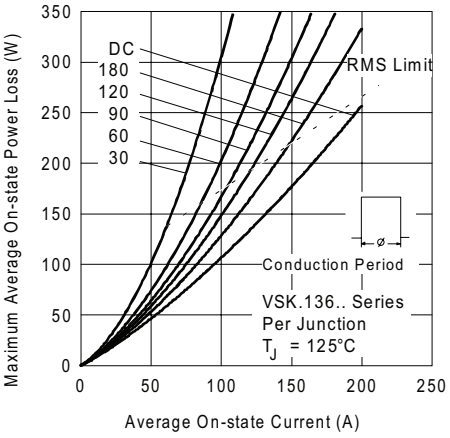


Fig. 4 - On-State Power Loss Characteristics

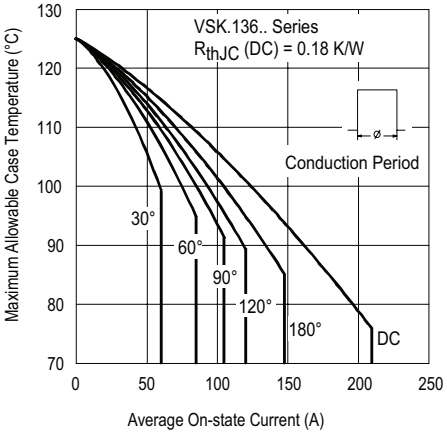


Fig. 2 - Current Ratings Characteristics

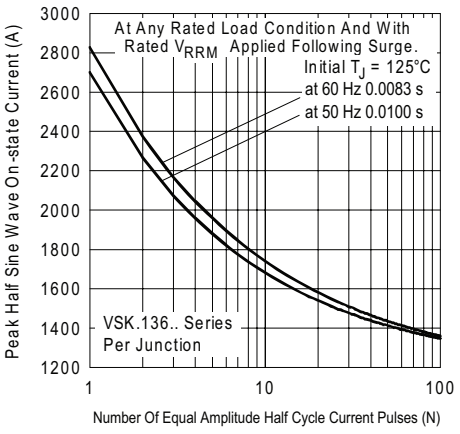


Fig. 5 - Maximum Non-Repetitive Surge Current

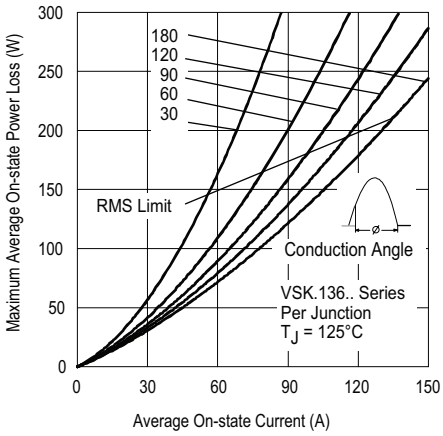


Fig. 3 - On-State Power Loss Characteristics

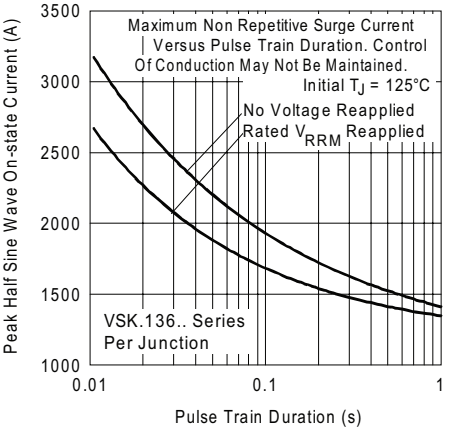


Fig. 6 - Maximum Non-Repetitive Surge Current

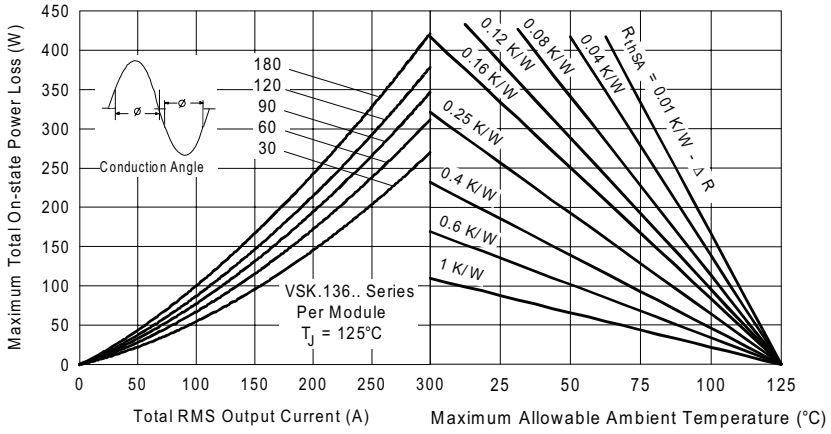


Fig. 7 - On-State Power Loss Characteristics

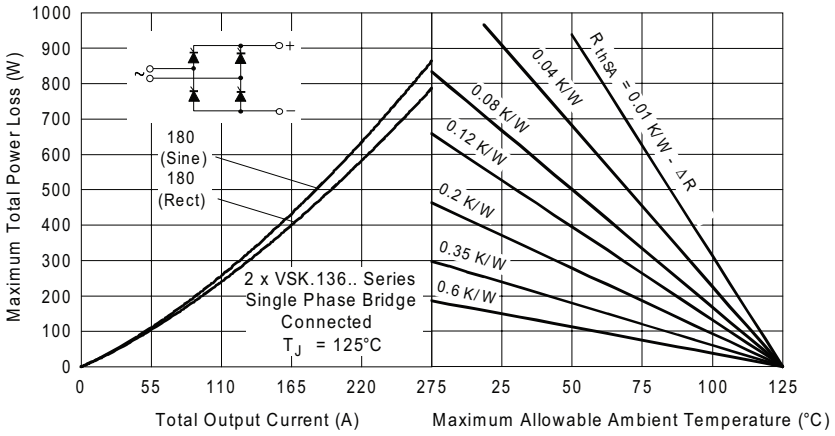


Fig. 8 - On-State Power Loss Characteristics

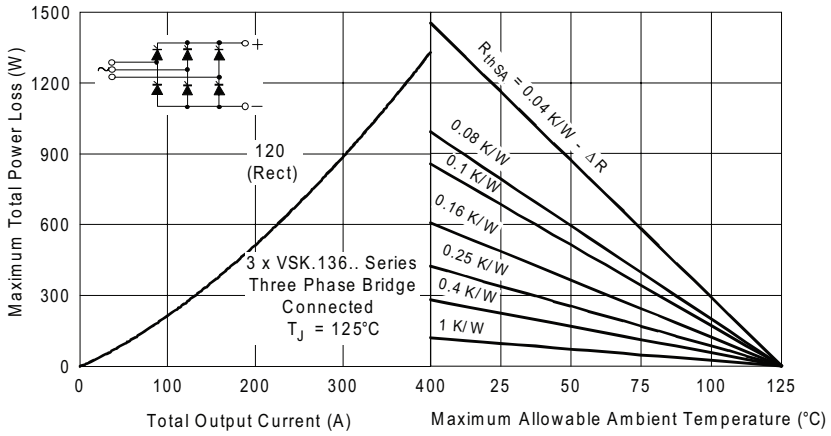


Fig. 9 - On-State Power Loss Characteristics

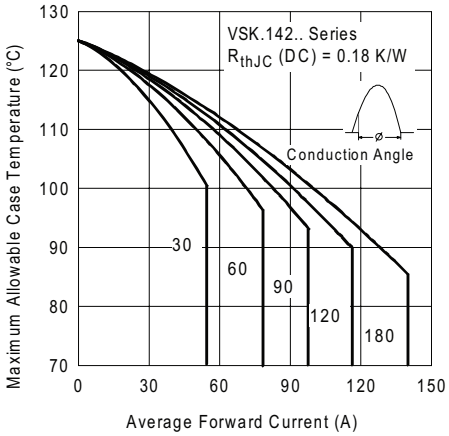


Fig. 10 - Current Ratings Characteristics

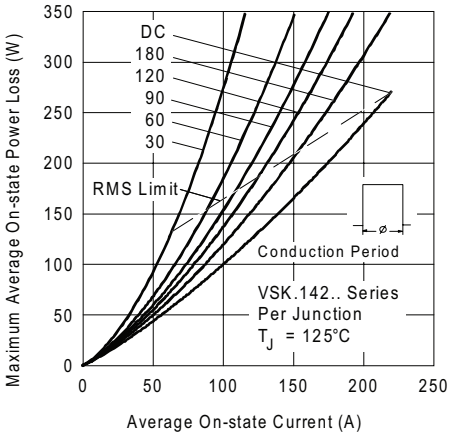


Fig. 13 - On-State Power Loss Characteristics

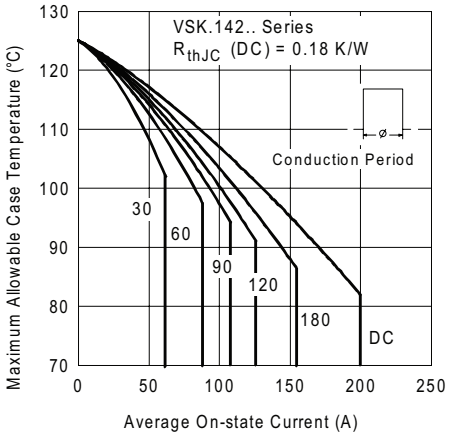


Fig. 11 - Current Ratings Characteristics

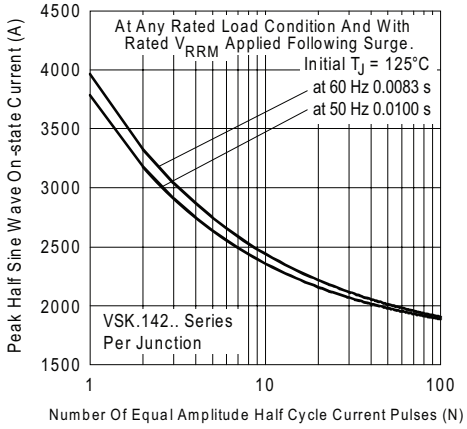


Fig. 14 - Maximum Non-Repetitive Surge Current

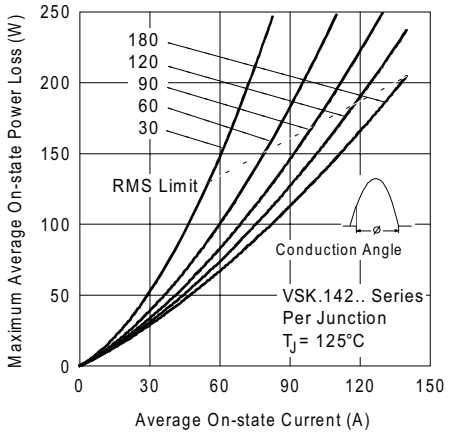


Fig. 12 - On-State Power Loss Characteristics

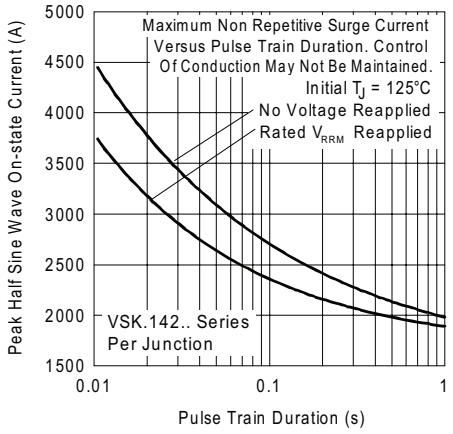


Fig. 15 - Maximum Non-Repetitive Surge Current

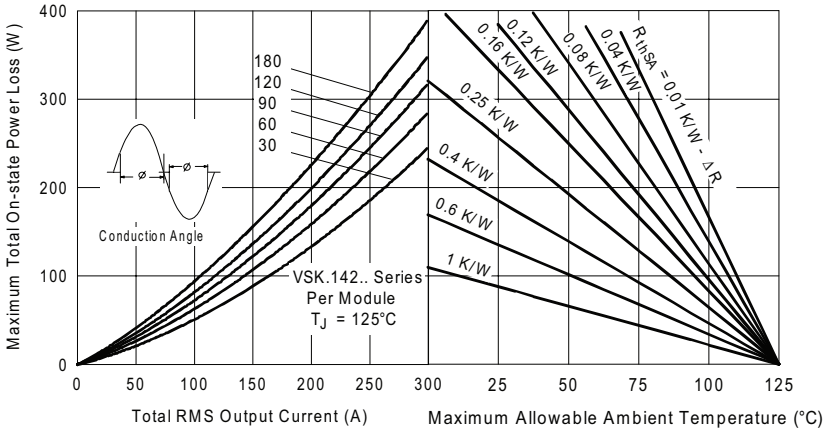


Fig. 16 - On-State Power Loss Characteristics

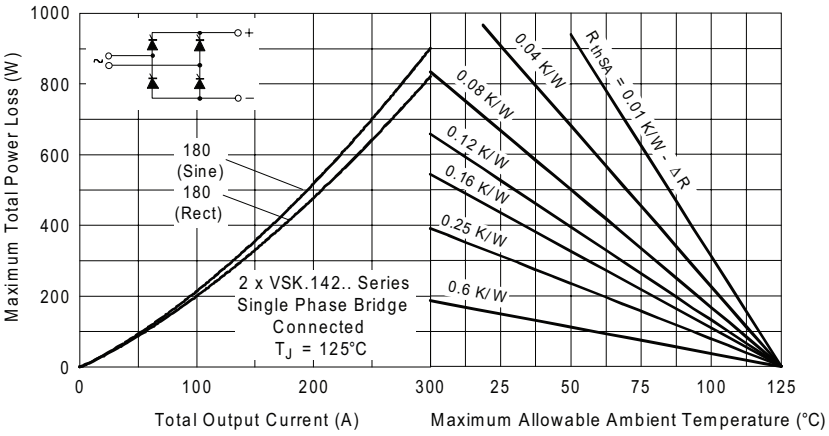


Fig. 17 - On-State Power Loss Characteristics

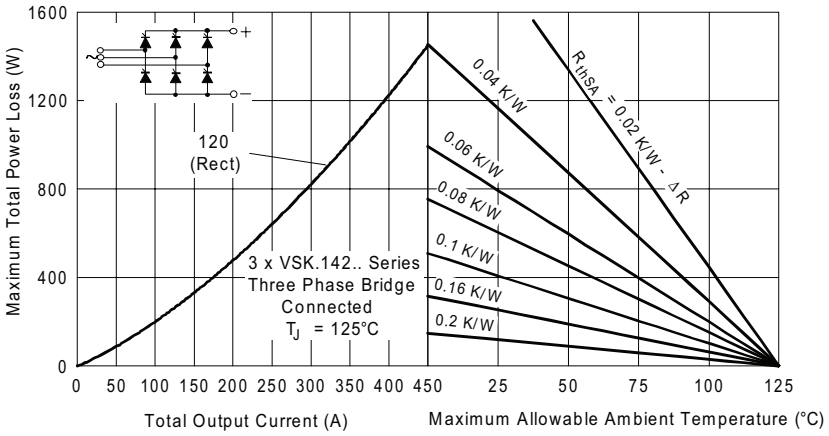


Fig. 18 - On-State Power Loss Characteristics

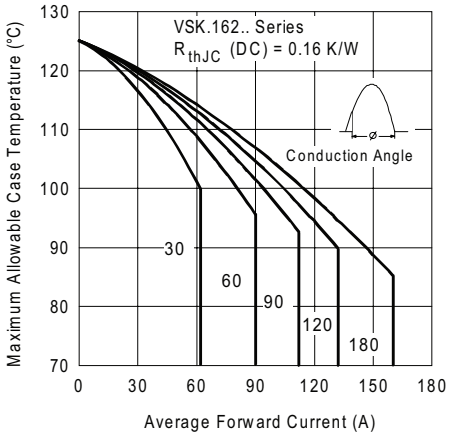


Fig. 19 - Current Ratings Characteristics

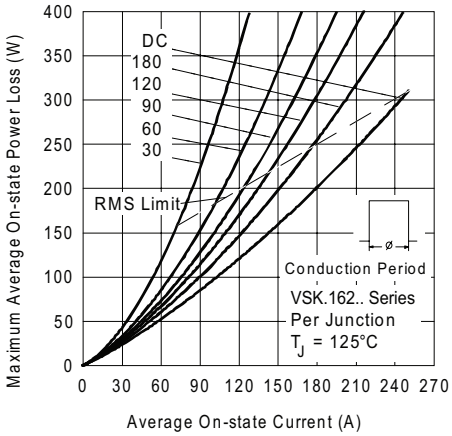


Fig. 22 - On-State Power Loss Characteristics

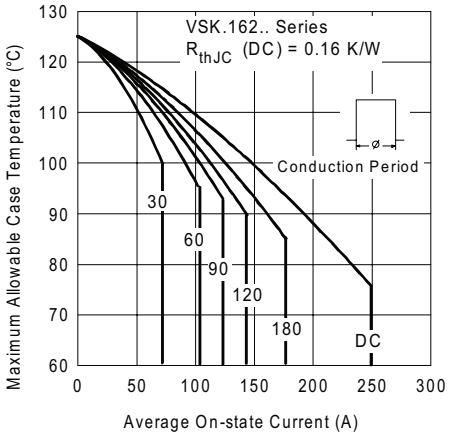


Fig. 20 - Current Ratings Characteristics

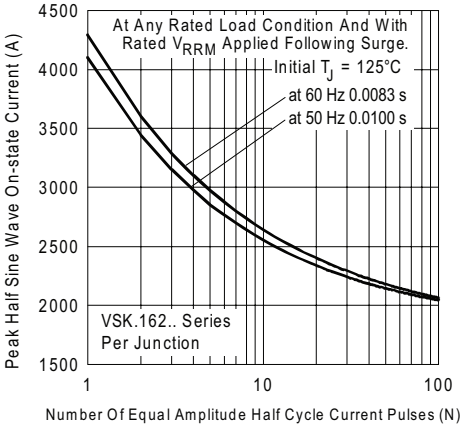


Fig. 23 - Maximum Non-Repetitive Surge Current

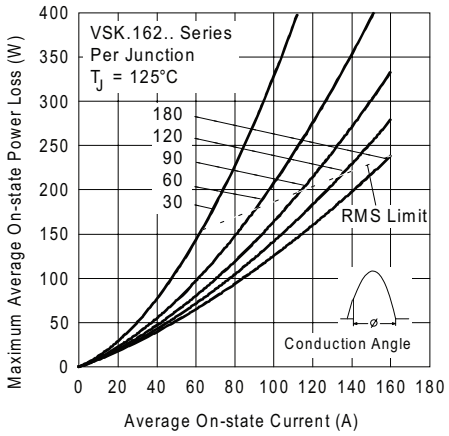


Fig. 21 - On-State Power Loss Characteristics

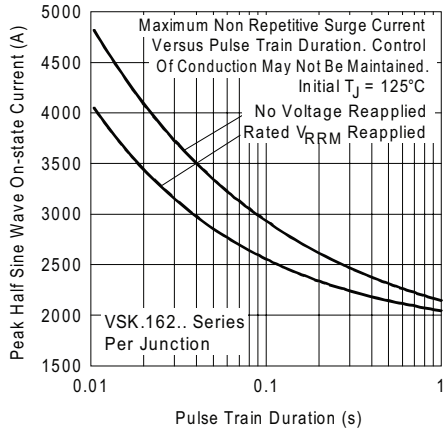


Fig. 24 - Maximum Non-Repetitive Surge Current

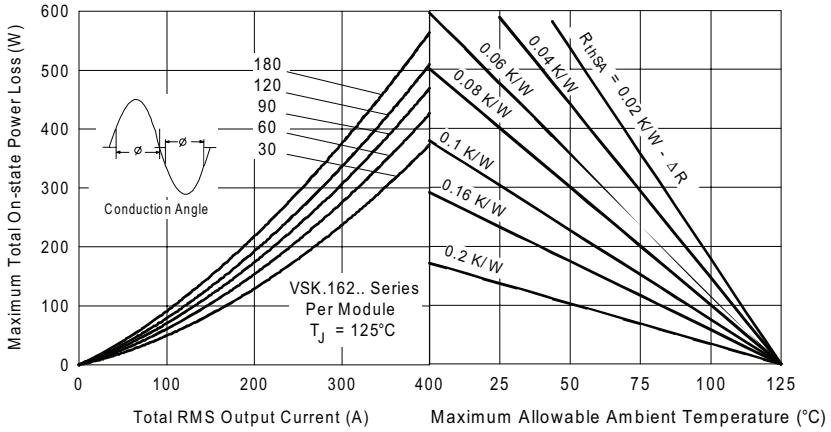


Fig. 25 - On-State Power Loss Characteristics

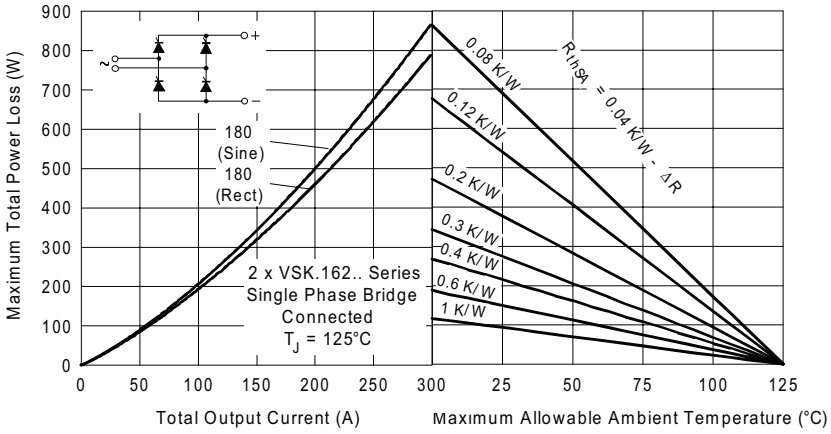


Fig. 26 - On-State Power Loss Characteristics

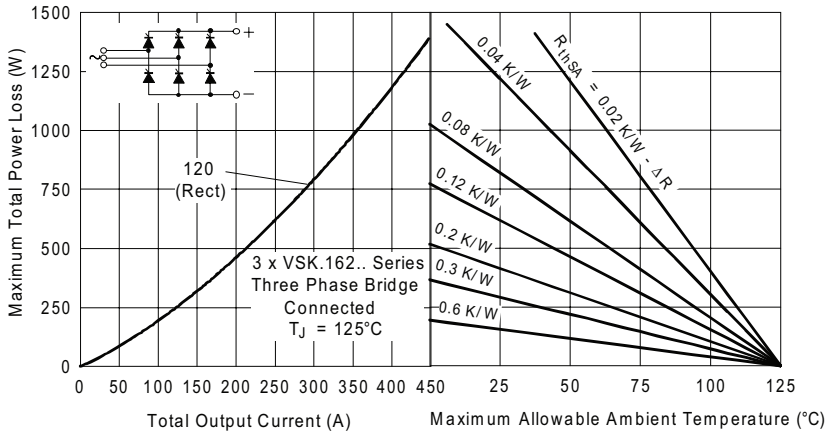


Fig. 27 - On-State Power Loss Characteristics

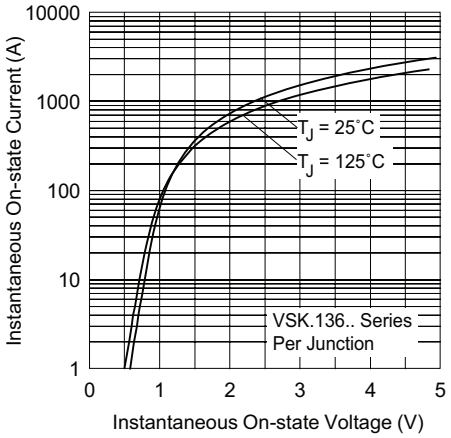


Fig. 28 - On-State Voltage Drop Characteristics

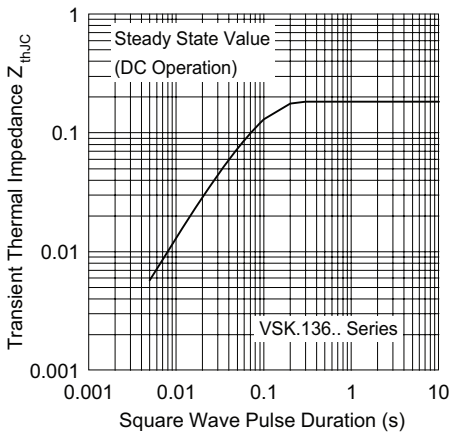


Fig. 31 - Thermal Impedance Z_{thJC} Characteristics

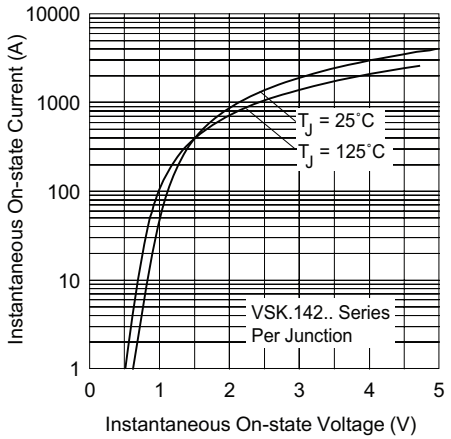


Fig. 29 - On-State Voltage Drop Characteristics

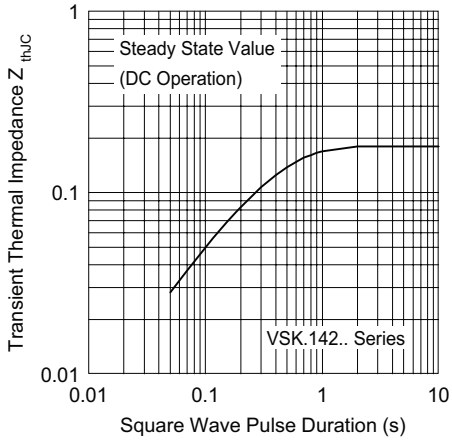


Fig. 32 - Thermal Impedance Z_{thJC} Characteristics

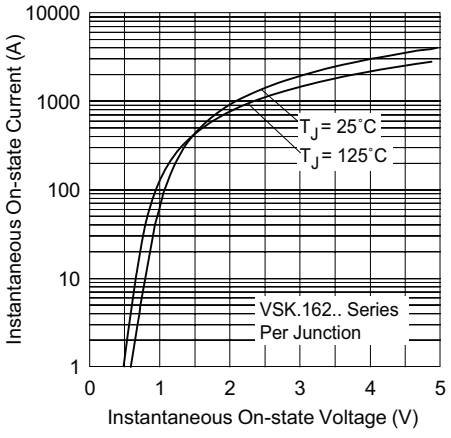


Fig. 30 - On-State Voltage Drop Characteristics

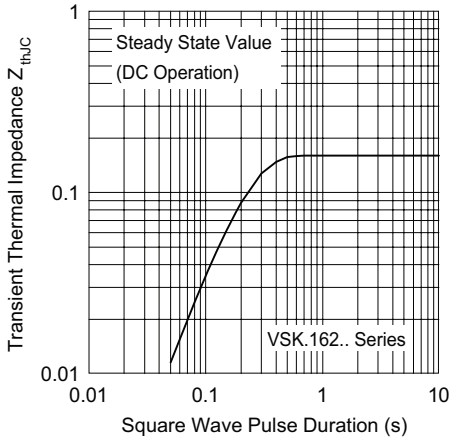


Fig. 33 - Thermal Impedance Z_{thJC} Characteristics

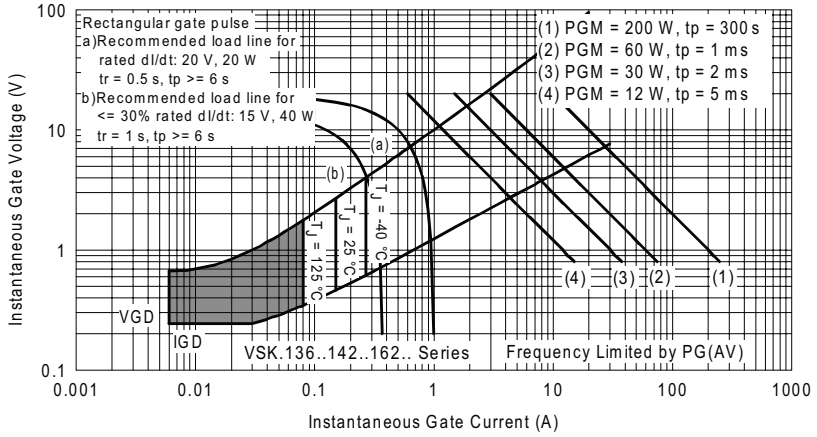


Fig. 34 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

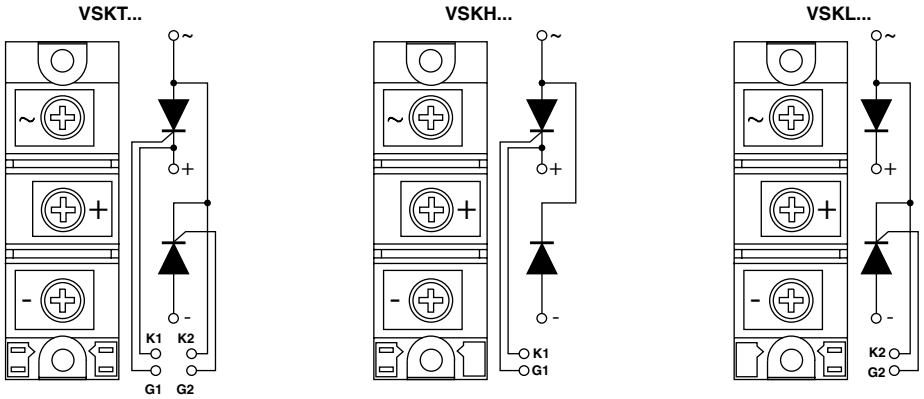
VSK	T	162	/	16	PbF
1	2	3		4	5

1 - Module type
2 - Circuit configuration
3 - Current rating: $I_{T(AV)}$
4 - Voltage code x 100 = V_{RRM}
5 - PbF = Lead (Pb)-free

Note

- To order the optional hardware go to www.vishay.com/doc?95172

CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95067

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.