Features

- Utilizes the ARM7TDMI™ ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-circuit Emulation)
- 8K Bytes Internal SRAM
- Fully-programmable External Bus Interface (EBI)
  - 128 M Bytes of Maximum External Address Space
  - 8 Chip Selects
  - Software Programmable 8-/16-bit External Databus
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 8 External Interrupts, Including a High-priority, Low-latency Interrupt Request
- 58 Programmable I/O Lines
- 6-channel 16-bit Timer/Counter
  - Six External Clock Inputs
  - Two Multi-purpose I/O Pins per Channel
- Three USARTs
- Master/Slave SPI Interface
  - 8-bit to 16-bit Programmable Data Length
  - Four External Slave Chip Selects
- Programmable Watchdog Timer
- 8-channel 10-bit ADC
- 2-channel 10-bit DAC
- Clock Generator with On-chip Main Oscillator and PLL for Multiplication
  - 3 MHz to 20 MHz Frequency Range Main Oscillator
- Real-time Clock with On-chip 32 kHz Oscillator
  - Battery Backup Operation and External Alarm
- 8-channel Peripheral Data Controller for USARTs and SPIs
- Advanced Power Management Controller (APMC)
  - Normal, Wait, Slow, Standby and Power-down Modes
- IEEE 1149.1 JTAG Boundary-scan on All Digital Pins
- Fully Static Operation: 0 Hz to 33 MHz Internal Frequency Range at V_{DDCORE} = 3.0 V, 85°C
- 2.7V to 3.6V Core Operating Range
- 2.7V to 5.5V I/O Operating Range
- 2.7V to 3.6V Analog Operating Range
- 1.8V to 3.6V Backup Battery Operating Range
- 2.7V to 3.6V Oscillator and PLL Operating Range
- -40°C to +85°C Temperature Range
- Available in a 176-lead TQFP or 176-ball BGA Package

Description

The AT91M55800A is a member of the Atmel AT91 16-/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

The fully-programmable External Bus Interface provides a direct connection to off-chip memory in as fast as one clock cycle for a read or write operation. An eight-level priority vectored interrupt controller in conjunction with the Peripheral Data Controller significantly improve the real-time performance of the device.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with an on-chip SRAM and a wide range of peripheral functions, analog interfaces and low-power oscillators on a monolithic chip,

AT91 ARM® Thumb® Microcontroller

AT91M55800A Electrical Characteristics

Rev. 1727E–ATARM–01/04

the Atmel AT91M55800A is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many ultra low-power applications.

Absolute Maximum Ratings*

Operating Temperature (Industrial).....-40°C to +85°C
Storage Temperature.....-60°C to + 150°C
Voltage on V_{DDBU} Powered Input Pins with Respect to Ground: .....-0.3V to +3.9V
Voltage on Any Other Input Pin with Respect to Ground..... ...-0.3V to +5.5V
Maximum Operating Voltage (V_{DDCORE}, V_{DDA}, V_{DDPLL} and V_{DDBU}) 3.6V
Maximum Operating Voltage (V_{DDIO}) 5.5V
DC Output Current (V_{DDIO})..... 4 mA
DC Output Current (V_{DDBU})..... 6 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The following characteristics are applicable to the Operating Temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a Junction Temperature up to T_J = 100°C.

Table 1. DC Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{DDBU}	DC Supply Backup Battery			1.8		3.6	V
V_{DDCORE}	DC Supply Core			2.7		3.6	V
V_{DDPLL}	DC Supply Oscillator and PLL			V_{DDCORE}		3.6	V
V_{DDA}	DC Supply Analog I/Os			V_{DDCORE}		3.6	V
V_{DDIO}	DC Supply Digital I/Os			V_{DDCORE}		V_{DDCORE} + 2.0 or 5.5	V
V_{IL}	Input Low-level Voltage	NRSTBU and WAKEUP pins		-0.3		0.3 x V_{DDBU}	V
		Other pins		-0.3		0.8	
V_{IH}	Input High-level Voltage	NRSTBU and WAKEUP pins		0.7 x V_{DDBU}		V_{DDBU} + 0.3	V
		Other pins		2		V_{DD} + 0.3(1)	
V_{OL}	Output Low-level Voltage	SHDN pin: V_{DDBU} = 3.0V I_{OL} = 0.3 mA(2)				GND_{BU} + 0.1	V
		Other pins: I_{OL} = 4 mA(2) I_{OL} = 0 mA(2)				0.4 0.2	
V_{OH}	Output High-level Voltage	SHDN pin: V_{DDBU} = 3.0V I_{OH} = 0.3 mA(2)		V_{DDBU} - 0.1			V
		Other pins: I_{OH} = 4 mA(2) I_{OH} = 0 mA(2		V_{DD} - 0.4(1) V_{DD} - 0.2(1)			
I_{LEAK}	Input Leakage Current					392	nA
I_{PULL}	Input Pull-up Current	Blocks powered by V_{DDBU}, V_{DDBU} = 3.6V, V_{IN} = 0				352	µA
		Blocks powered by V_{DDIO}, V_{DDA} and V_{DDPLL}, V_{DD} = 3.6V(1), V_{IN} = 0				280	
C_{IN}	Input Capacitance	176-TQFP Package				6	pF
I_{SC}	Static Current	V_{DD}(1) = V_{DDCORE} = 3.6V, MCK = 0 Hz	T_A = 25°C			25	µA
		All inputs driven TMS, TDI, TCK, NRST = 1	T_A = 85°C			500	

Notes: 1. V_{DD} is applicable to V_{DDIO}, V_{DDA} and V_{DDPLL}.
2. I_O = Output Current.

Power Consumption

The values in the following tables are measured values in the operating conditions indicated (i.e., V_{DDIO} = 3.3V, V_{DDCORE} = 3.3V, T_A = 25°C) on the AT91EB55 Evaluation Board. They represent the power consumption on the V_{DDCORE} power supply unless otherwise specified.

Table 2. Power Consumption

Mode	Conditions	Consumption	Unit
Normal	Fetch in ARM mode out of internal SRAM All peripheral clocks activated	6.55	mW/MHz
	Fetch in ARM mode out of internal SRAM All peripheral clocks deactivated	4.59	
Idle	All peripheral clocks activated	3.85	
	All peripheral clocks deactivated	1.78	

Table 3. Power Consumption per Peripheral

Peripheral	Consumption	Unit
PIO Controller	0.22	mW/MHz
Timer/Counter Channel	0.15	
Timer/Counter Block (3 Channels)	0.42	
USART	0.40	
SPI	0.40	
ADC	0.23	
DAC	0.29	
PLL (1) (2)	2.6	mW

Notes: 1. Power consumption on the V_{DDPLL} power supply.
2. With a reference frequency equal to 16 MHz, output frequency of 32 MHz and R = 287Ω, C_1 = 680 pF, C_2 = 68 pF as loop filter.

Table 4. Battery Supply Voltage Consumption

Condition	Consumption	Unit
V_{DDBU} = 3.0 V Power consumption on the V_{DDBU} Power Supply. Without any capacitor connected to the RTC oscillator pins (XIN32, XOUT32)	0.9	µA

Thermal and Reliability Considerations

Thermal Data

In Table 5, the device lifetime is estimated with the MIL-217 standard in the “moderately controlled” environmental model (this model is described as corresponding to an installation in a permanent rack with adequate cooling air), depending on the device Junction Temperature. (For details see the section “Junction Temperature” on page 6.)

Note that the user must be extremely cautious with this MTBF calculation: as the MIL-217 model is pessimistic with respect to observed values due to the way the data/models are obtained (test under severe conditions). The life test results that have been measured are always better than the predicted ones.

Table 5. MTBF Versus Junction Temperature

Junction Temperature (T_J) (°C)	Estimated Lifetime (MTBF) (Year)
100	25
125	14
150	8
175	5

Table 6 summarizes the thermal resistance data related to the package of interest.

Table 6. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP176	21	°C/W
			PBGA176	66	
θ_{JC}	Junction-to-case thermal resistance		TQFP176	9.2	
			PBGA176	20.1	

Reliability Data

The number of gates and the device die size are provided for the user to calculate reliability data with another standard and/or in another environmental model.

Table 7. Reliability Data

Parameter	Data	Unit
Number of Logic Gates	524	K gates
Number of Memory Gates	400	K gates
Device Die Size	29.0	mm^2

Junction Temperature

The average chip-junction temperature T_J in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

Where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 6 on page 5.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 6 on page 5.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section “Power Consumption” on page 4.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and thereby decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Conditions

Timing Results

The delays are given as typical values in the following conditions:

- V_{DDIO} = 5V
- V_{DDCORE} = 3.3V
- Ambient Temperature = 25°C
- Load Capacitance is 0 pF.
- The output level change detection is *(0.5* x V_{DDIO}).
- The input level is (*0.3 x* V_{DDIO}) for a low-level detection and is (*0.7 x* V_{DDIO}) for a high level detection.
- The Master Clock (MCK) source is a crystal oscillator connected to the XIN input.

The minimum and maximum values given in the AC characteristics tables of this datasheet take into account the process variation and the design. In order to obtain the timing for other conditions, the following equation should be used.

$$t = \delta_{T^\circ} \times ((\delta_{VDDCORE} \times t_{DATASHEET}) + (\delta_{VDDIO} \times \sum(C_{SIGNAL} \times \delta_{CSIGNAL})))$$

where:

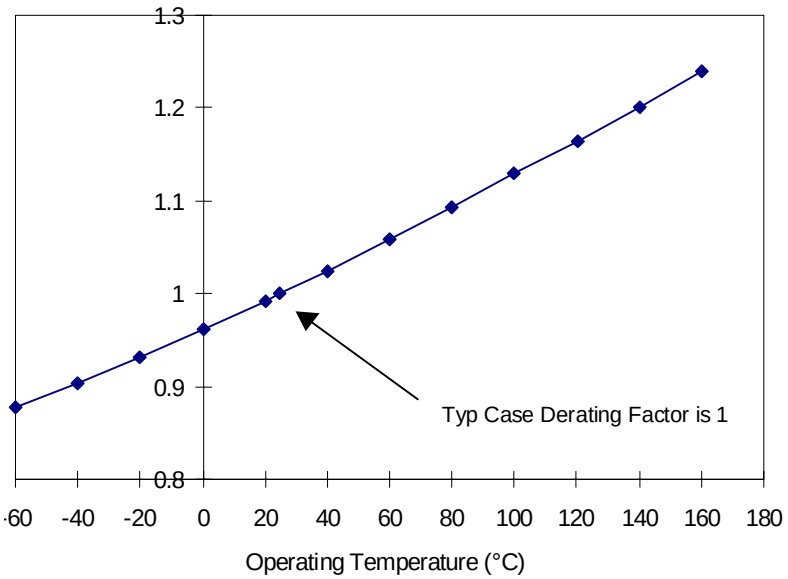
- δ_{T° is the derating factor in temperature given in Figure 1.
- $\delta_{VDDCORE}$ is the derating factor for the Core Power Supply given in Figure 2 on page 8.
- $t_{DATASHEET}$ is the minimum or maximum timing value given in this datasheet for a load capacitance of 0 pF.
- δ_{VDDIO} is the derating factor for the IO Power Supply given in Figure 3 on page 9.
- C_{SIGNAL} is the capacitance load on the considered output pin. (1)
- $\delta_{CSIGNAL}$ is the load derating factor depending on the capacitance load on the related output pins given in Min and Max in this datasheet.

The input delays are given as typical values.

Note: 1. The user must take into account the package capacitance load contribution (C_{IN}) described in Table 1 on page 3.

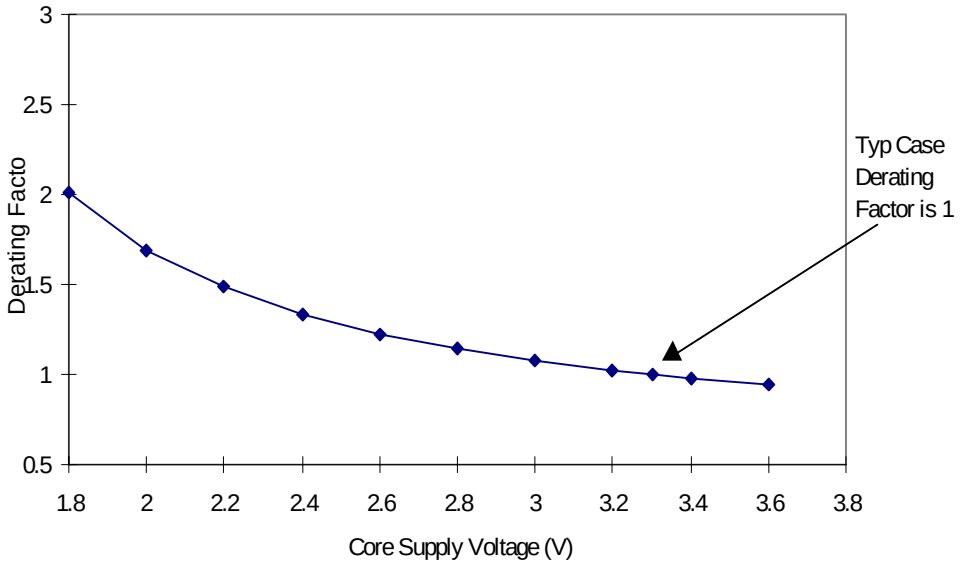
Temperature Derating Factor

Figure 1. Derating Curve for Different Operating Temperatures



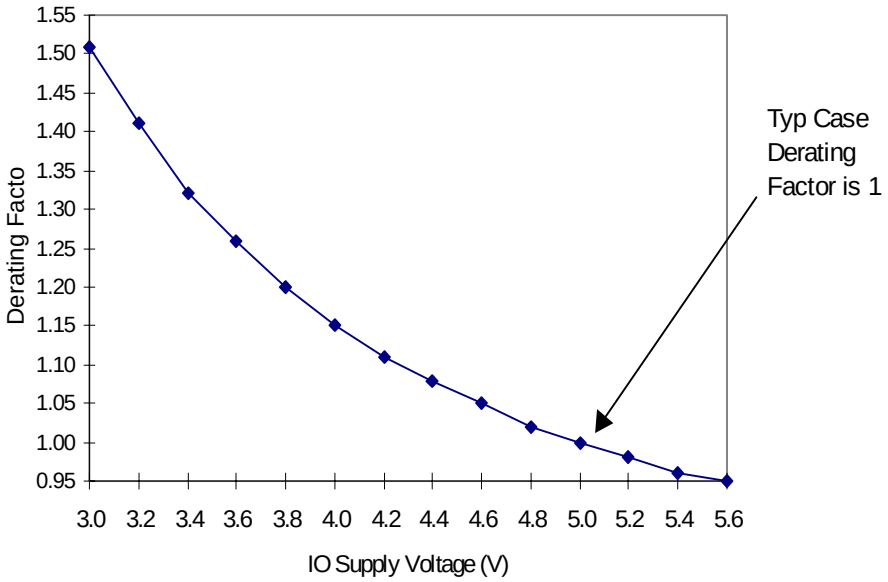
Core Voltage Derating Factor

Figure 2. Derating Curve for Different Core Supply Voltages



IO Voltage Derating Factor

Figure 3. Derating Curve for Different IO Supply Voltages



Note: The derating factor in this example is applicable only to timings related to output pins.

Crystal Oscillator Characteristics

Table 8. RTC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPRTC})$	Crystal Oscillator Frequency			32.768		KHz
C_{L1}, C_{L2}	Internal Load Capacitance ($C_{L1} = C_{L2}$)			12		pF
C_L	Equivalent Load Capacitance	$C_{L1} = C_{L2} = 12$ pF		6		pF
	Duty Cycle	Measured at the MCKO output pin	45	50	55	%
t_{ST}	Startup Time	Without any additional load capacitance and an ESR Max = 50 kΩ			300	ms
		With 13 pF external capacitor per pin and an ESR Max = 50 kΩ			700	ms

Table 9. Main Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency		3	16	20	MHz
C_{L1}, C_{L2}	Internal Load Capacitance (CL1 = CL2)			25		pF
C_L	Equivalent Load Capacitance	$C_{L1} = C_{L2} = 25$ pF		12.5		pF
	Duty Cycle		45	50	55	%
t_{ST}	Startup Time	With 10 pF external capacitor per pin and a 3 MHz crystal (1)			13	ms
		With 10 pF external capacitor per pin and a 8 MHz crystal (2)			4.2	ms
		With 10 pF external capacitor per pin and a 16 MHz crystal (3)			1.4	ms
		With 10 pF external capacitor per pin and a 20 MHz crystal (3)			1	ms

Notes:
1. With ESR (Electrical Serie Resistor) maximum equal to 200 Ω, C_S maximum = 3 pF.
2. With ESR maximum equal to 100 Ω, C_S maximum = 7 pF.
3. With ESR maximum equal to 50 Ω, C_S maximum = 7 pF.

Clock Waveforms

Table 10. Master Clock Waveform Parameters

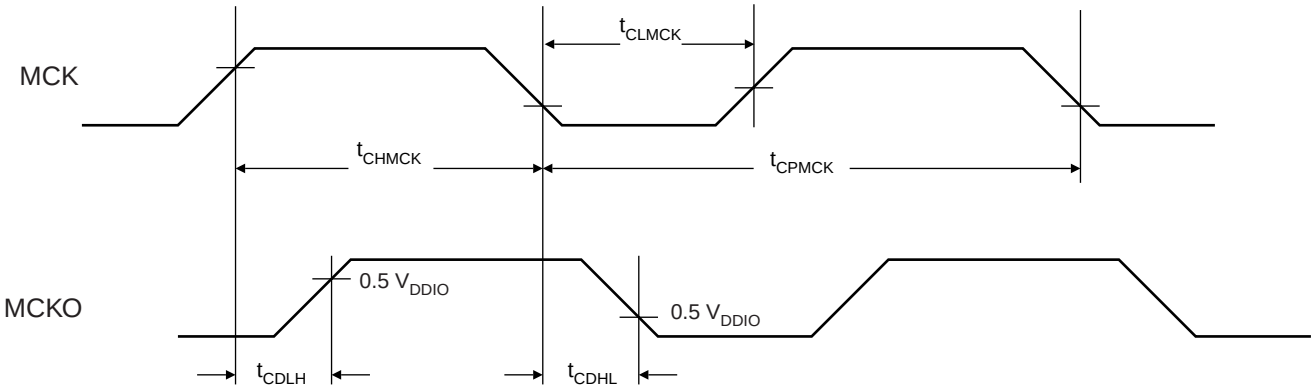
Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPMCK})$	Master Clock Frequency			41.8	MHz
t_{CPMCK}	Master Clock Period		23.9		ns
t_{CHMCK}	Master Clock High Half-period		0.45 x t_{CPMCK}	0.55 x t_{CPMCK}	ns
t_{CLMCK}	Master Clock Low Half-period		0.45 x t_{CPMCK}	0.55 x t_{CPMCK}	ns

Table 11. Clock Propagation Times

Symbol	Parameter	Conditions	Min	Max	Units
t_{CDLH} (1)	MCK Rising to MCKO Rising Edge	C_{MCKO} = 0 pF	7.5	11.7	ns
		C_{MCKO} derating	0.053	0.083	ns/pF
t_{CDHL} (1)	MCK Falling to MCKO Falling Edge	C_{MCKO} = 0 pF	7.7	12.1	ns
		C_{MCKO} derating	0.059	0.092	ns/pF

Note: 1. Applicable only when MCKO outputs Master Clock.

Figure 4. Clock Waveform



APMC Characteristics

Table 12. Master Clock Source Switch Times

MCK Source		Switch Time		
From	**To**	**Min**	**Typ**	**Max**
RTC Oscillator Output	PLL Output		$4 \times t_{CPRTC} + 3 \times t_{CPPLL}$	
PLL Output	RTC Oscillator Output		$5 \times t_{CPRTC}$	
Main Oscillator Output	PLL Output		$5 \times t_{CPRTC} + 3 \times t_{CPPLL}$	
PLL Output	Main Oscillator Output		$4 \times t_{CPRTC} + 3 \times t_{CPMAIN}$	
RTC Oscillator Output	Main Oscillator Output		$3 \times t_{CPRTC} + 3 \times t_{CPMAIN}$	
Main Oscillator Output	RTC Oscillator Output		$5 \times t_{CPRTC}$	
PLL Output Freq. 1	PLL Output Freq. 2		$7 \times t_{CPRTC} + 3 \times t_{CPPLL2}$	

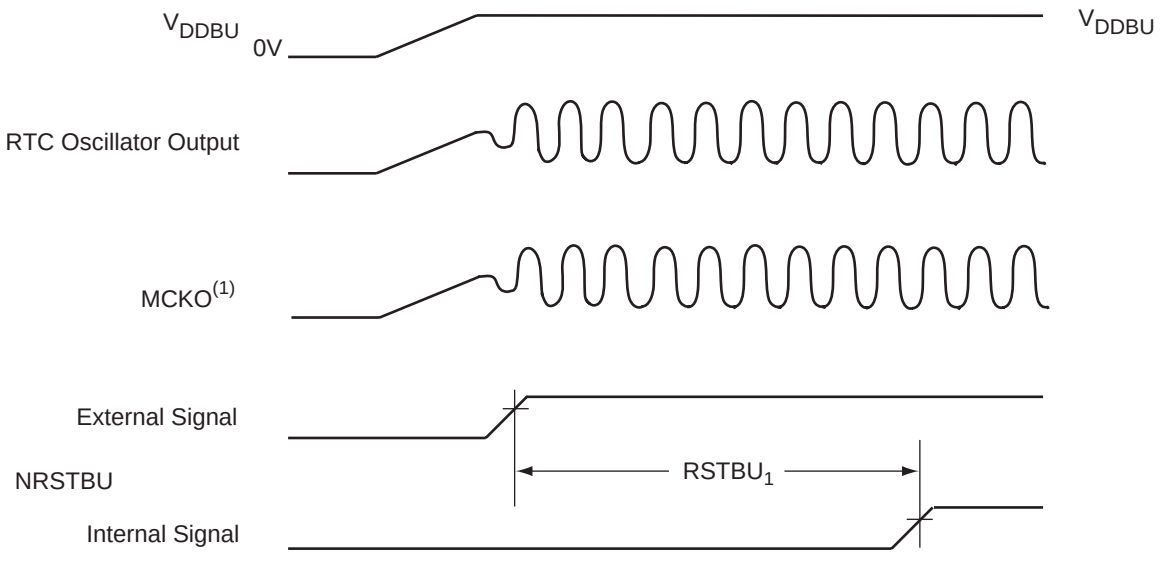
Backup Battery Reset Signal

Internally to the device, the NRSTBU signal is maintained low for $RSTBU_1$ time after the rising edge of the external signal. Therefore, the NRSTBU signal needs to be asserted only during the V_{DDBU} power ramp up by the user. This feature covers the requirement of an NRSTBU signal assertion of $10(t_{CPRTC})$ at a minimum at V_{DDBU} power up.

Table 13. Backup Battery Reset Signal Internal Assertion Delay

Symbol	Parameter	Typical Internal Delay	Units
$RSTBU_1$	NRSTBU Internal Assertion Delay	1	s

Figure 5. NRSTBU Assertion Sequence



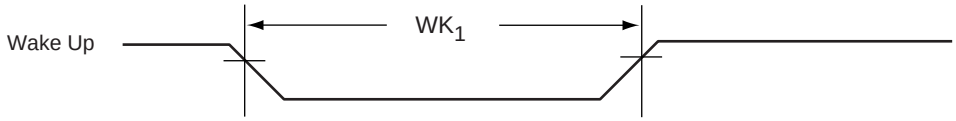
Note: 1. The MCKO Signal is certified to be valid at the NRSTBU Internal Signal rising edge.

Wake Up Signal

Table 14. Wake Up Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
WK_1	Wake Up Minimum Pulse Width	46	µs

Figure 6. Wake Up Signal



Analog Characteristics

ADC

Table 15. Channel Conversion Time Relative to ADC Clock

Parameter	Min	Typ	Max	Units
Channel Conversion Time		11		cycle
ADC Clock Frequency			800	kHz

Table 16. External Voltage Reference Input

Symbol	Parameter	Min	Max	Units
V_{REF}	ADVREF Input Voltage Range	2.4	V_{DDA}	V
	ADVREF Input Resistance	12	24	kΩ

Table 17. Analog Inputs

Parameter	Min	Typ	Max	Units
Input Voltage Range	0		V_{REF}	V
Input Leakage Current	-0.1		0.1	µA
Input Capacitance			30	pF

Table 18. Dynamic Performance

Parameter	Conditions	Min	Max	Units
Signal-to-noise Ratio				dB
Total Harmonic Distortion				dB
Inter-modulation Distortion				dB
Channel-to-Channel Isolation				dB

Table 19. Transfer Characteristics

Parameter	Conditions		Min	Max	Units
Resolution				10	Bit
Integral Non-linearity	V_{DDA} = 3.3V ±10%, ADVREF = V_{DDA}	ADC Clock = 500 kHz		±3	LSB
		ADC Clock = 800 kHz		±4	

Table 19. Transfer Characteristics

Parameter	Conditions		Min	Max	Units
Differential Non-linearity	V_{DDA} = 3.3V ±10%, ADVREF = V_{DDA}	ADC Clock = 500 kHz		±2	LSB
		ADC Clock = 800 kHz		±4	
Offset Error				±2	LSB
Gain Error				±4	LSB

DAC

Table 20. DAC Timing Characteristics

Parameter	Conditions	Min	Max	Units
Channel Setting Time	0.85V to 1.85V or 1.85V to 0.85V		6	µs

Table 21. External Voltage Reference Input

Symbol	Parameter	Min	Max	Units
V_{REF}	DAVREF Input Voltage Range	2.4	V_{DDA}	V
	DAVREF Input Resistance	12	24	kΩ

Table 22. Output Op Amp Characteristics

Parameter	Conditions	Min	Max	Units
Output Voltage Range		0	V_{REF}	V
Input Offset Voltage			10	mV
Output Source Current			5	mA
Output Sink Current			5	mA
Slew Rate	Rise or Fall	0.2		V/µs
Startup Time	Load = 50 pF /10 kΩ (in parallel)		100	µs
Overshoot	100 mV@ vcm		20	%

Table 23. Dynamic Performance

Parameter	Conditions	Min	Max	Units
Total Harmonic Distortion			TBD	dB

Table 24. Transfer Characteristics

Parameter	Conditions	Min	Max	Units
Resolution			10	Bit
Integral Non-linearity	V_{DDA} = 3.3V ±10%, DAVREF > 2.4V		4	LSB
Differential Non-linearity	V_{DDA} = 3.3V ±10%, DAVREF > 2.4V		4	LSB
Offset Error			2	LSB
Gain Error			4	LSB

AC Characteristics

EBI Signals Relative to MCK

The following tables show timings relative to operating condition limits defined in the section “Timing Results” on page 7

Table 25. General-purpose EBI Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_1	MCK Falling to NUB Valid	C_{NUB} = 0 pF	8.9	17	ns
		C_{NUB} derating	0.053	0.092	ns/pF
EBI_2	MCK Falling to NLB/A0 Valid	C_{NLB} = 0 pF	8.3	14.8	ns
		C_{NLB} derating	0.053	0.092	ns/pF
EBI_3	MCK Falling to A1 - A23 Valid	C_{ADD} = 0 pF	8	15.2	ns
		C_{ADD} derating	0.053	0.092	ns/pF
EBI_4	MCK Falling to Chip Select Change	C_{NCS} = 0 pF	8.2	15.6	ns
		C_{NCS} derating	0.053	0.092	ns/pF
EBI_5	NWAIT Setup before MCK Rising		-0.4		ns
EBI_6	NWAIT Hold after MCK Rising		5.9		ns

Table 26. EBI Write Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_7	MCK Rising to NWR Active (No Wait States)	C_{NWR} = 0 pF	8.2	13	ns
		C_{NWR} derating	0.059	0.092	ns/pF
EBI_8	MCK Rising to NWR Active (Wait States)	C_{NWR} = 0 pF	9	14.1	ns
		C_{NWR} derating	0.059	0.092	ns/pF
EBI_9	MCK Falling to NWR Inactive (No Wait States)	C_{NWR} = 0 pF	8.6	13.5	ns
		C_{NWR} derating	0.053	0.083	ns/pF
EBI_{10}	MCK Rising to NWR Inactive (Wait States)	C_{NWR} = 0 pF	8.9	13.9	ns
		C_{NWR} derating	0.053	0.083	ns/pF
EBI_{11}	MCK Rising to D0 - D15 Out Valid	C_{DATA} = 0 pF	8.3	15.4	ns
		C_{DATA} derating	0	0.086	ns/pF
EBI_{12}	NWR High to NUB Change	C_{NUB} = 0 pF	4.8	9.6	ns
		C_{NUB} derating	0.053	0.092	ns/pF
EBI_{13}	NWR High to NLB/A0 Change	C_{NLB} = 0 pF	4.6	7.4	ns
		C_{NLB} derating	0.059	0.092	ns/pF
EBI_{14}	NWR High to A1 - A23 Change	C_{ADD} = 0 pF	4.4	8.1	ns
		C_{ADD} = derating	0.059	0.092	ns/pF
EBI_{15}	NWR High to Chip Select Inactive	C_{NCS} = 0 pF	4.4	8.6	ns
		C_{NCS} derating	0.053	0.083	ns/pF
EBI_{16}	Data Out Valid before NWR High (No Wait States) (1)	C = 0 pF	t_{CHMCK} - 1.9		ns
		C_{DATA} derating	- 0.086		ns/pF
		C_{NWR} derating	0.083		ns/pF
EBI_{17}	Data Out Valid before NWR High (Wait States) (1)	C = 0 pF	n x t_{CPMCK} - 1.5 (2)		ns
		C_{DATA} derating	-0.086		ns/pF
		C_{NWR} derating	0.083		ns/pF
EBI_{18}	Data Out Valid after NWR High		4.4		ns
EBI_{19}	NWR Minimum Pulse Width (No Wait States) (1)	C_{NWR} = 0 pF	t_{CHMCK} + 0.3		ns
		C_{NWR} derating	-0.009		ns/pF
EBI_{20}	NWR Minimum Pulse Width (Wait States) (1)	C_{NWR} = 0 pF	n x t_{CPMCK} - 0.2(2)		ns
		C_{NWR} derating	-0.009		ns/pF

Notes: 1. The derating factor is not to be applied to t_{CHMCK} or t_{CPMCK}.
2. n = number of standard wait states inserted.

Table 27. EBI Read Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_{21}	MCK Falling to NRD Active (1)	C_{NRD} = 0 pF	8.5	14.5	ns
		C_{NRD} derating	0.059	0.092	ns/pF
EBI_{22}	MCK Rising to NRD Active (2)	C_{NRD} = 0 pF	7.7	14.2	ns
		C_{NRD} derating	0.059	0.092	ns/pF
EBI_{23}	MCK Falling to NRD Inactive (1)	C_{NRD} = 0 pF	8.3	14.5	ns
		C_{NRD} derating	0.053	0.083	ns/pF
EBI_{24}	MCK Falling to NRD Inactive (2)	C_{NRD} = 0 pF	7.9	12.4	ns
		C_{NRD} derating	0.053	0.083	ns/pF
EBI_{25}	D0-D15 in Setup before MCK Falling (5)		-2.2		ns
EBI_{26}	D0-D15 in Hold after MCK Falling (5)		6.8		ns
EBI_{27}	NRD High to NUB Change	C_{NUB} = 0 pF	5	9.6	ns
		C_{NUB} derating	0.053	0.092	ns/pF
EBI_{28}	NRD High to NLB/A0 Change	C_{NLB} = 0 pF	4.7	7.4	ns
		C_{NLB} derating	0.059	0.092	ns/pF
EBI_{29}	NRD High to A1-A23 Change	C_{ADD} = 0 pF	4.5	8	ns
		C_{ADD} derating	0.059	0.092	ns/pF
EBI_{30}	NRD High to Chip Select Inactive	C_{NCS} = 0 pF	4.4	8.5	ns
		C_{NCS} derating	0.053	0.083	ns/pF
EBI_{31}	Data Setup before NRD High (5)	C_{NRD} = 0 pF	11		ns
		C_{NRD} derating	0.083		ns/pF
EBI_{32}	Data Hold after NRD High (5)	C_{NRD} = 0 pF	-3.6		ns
		C_{NRD} derating	-0.053		ns/pF
EBI_{33}	NRD Minimum Pulse Width (1) (3)	C_{NRD} = 0 pF	$(n+1) \times t_{CPMCK} - 1.5$ (4)		ns
		C_{NRD} derating	-0.009		ns/pF
EBI_{34}	NRD Minimum Pulse Width (2) (3)	C_{NRD} = 0 pF	$n \times t_{CPMCK} + (t_{CHMCK} - 1.7)$(4)		ns
		C_{NRD} derating	-0.009		ns/pF

Notes:
1. Early Read Protocol.
2. Standard Read Protocol.
3. The derating factor is not to be applied to t_{CHMCK} or t_{CPMCK}.
4. n =number of standard Wait States inserted.
5. Only one of these two timings needs to be met.

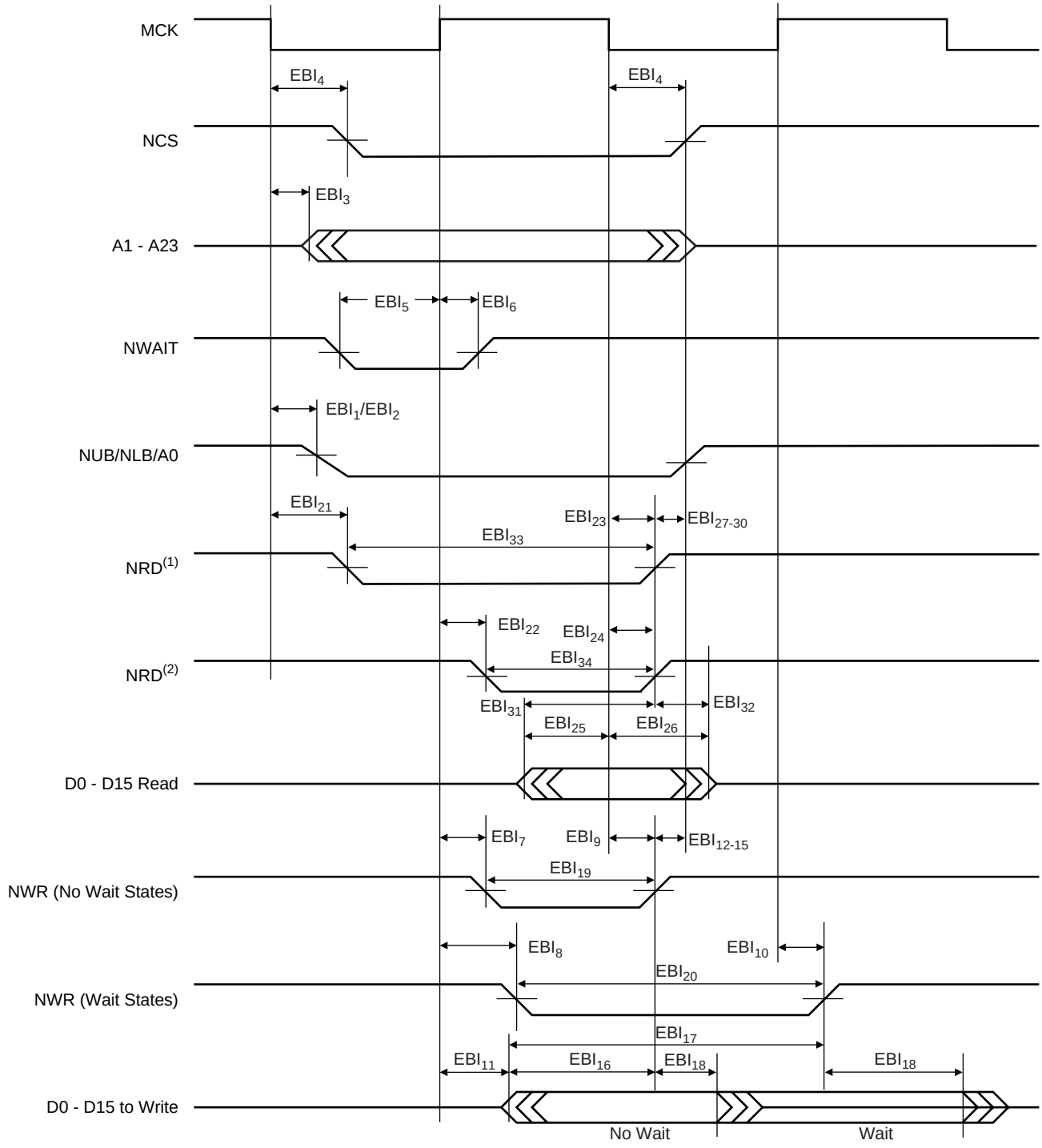
Table 28. EBI Read and Write Control Signals. Capacitance Limitation

Symbol	Parameter	Conditions	Min	Max	Units
T_{CPLNRD}(1)	Master Clock Low Due to NRD Capacitance	C_{NRD} = 0 pF	11.2		ns
		C_{NRD} derating	0.083		ns/pF
T_{CPLNWR}(2)	Master CLock Low Due to NWR Capacitance	C_{NWR} = 0 pF	10.3		ns
		C_{NWR} derating	0.083		ns/pF

Notes: 1. If this condition is not met, the action depends on the read protocol intended for use.
- Early Read Protocol: Programing an additional t_{DF} (Data Float Output Time) cycle.
- Standard Read Protocol: Programming an additional t_{DF} Cycle and an additional wait state.

2. Applicable only for chip select programmed with 0 wait state. If this condition is not met, at least one wait state must be programmed.

Figure 7. EBI Signals Relative to MCK



Notes: 1. Early Read Protocol.
2. Standard Read Protocol.

Peripheral Signals

USART Signals

The inputs must meet the minimum pulse width and period constraints shown in Table 29 and Table 30, and represented in Figure 8.

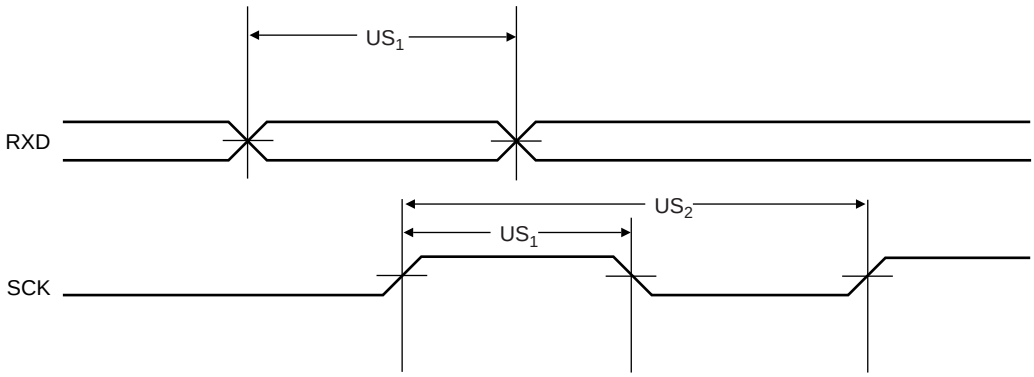
Table 29. USART Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
US_1	SCK/RXD Minimum Pulse Width	$5(t_{CPMCK}/2)$	ns

Table 30. USART Minimum Input Period

Symbol	Parameter	Min Input Period	Units
US_2	SCK Minimum Input Period	$9(t_{CPMCK}/2)$	ns

Figure 8. USART Signals



SPI Signals

The inputs must meet the minimum pulse width and period constraints shown in Table 31 and Table 32 and as represented in Figure 9.

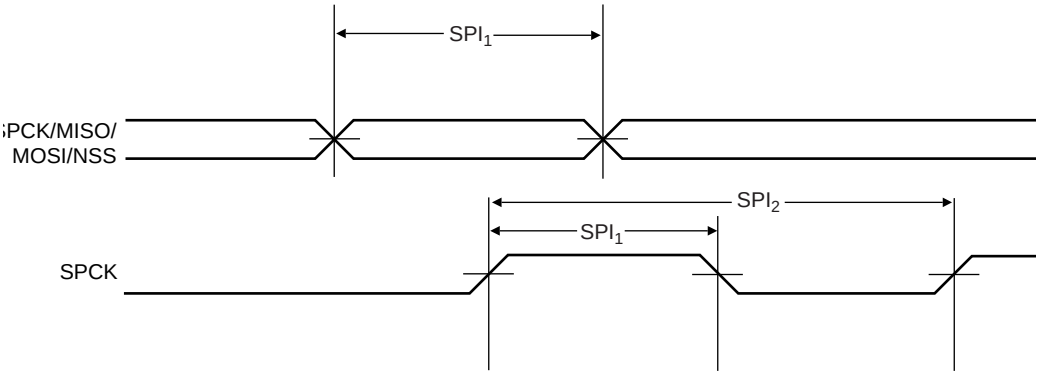
Table 31. SPI Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
SPI_1	SPK/MISO/MOSI/NSS Minimum Pulse Width	$3(t_{CPMCK}/2)$	ns

Table 32. SPI Minimum Input Period

Symbol	Parameter	Min Input Period	Units
SPI_2	SPCK Minimum Input Period	$5(t_{CPMCK}/2)$	ns

Figure 9. SPI Signals



Timer/Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is $3(t_{CPMCK})$ in Waveform Event Detection mode and $4(t_{CPMCK})$ in Waveform Total-count Detection mode. The inputs must meet the minimum pulse width and minimum input period shown in Table 33 and Table 34, and as represented in Figure 10.

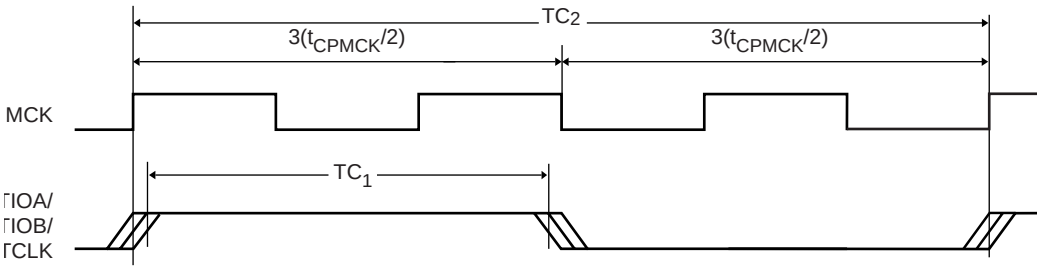
Table 33. Timer Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
TC_1	TCLK/TIOA/TIOB Minimum Pulse Width	$3(t_{CPMCK}/2)$	ns

Table 34. Timer Input Minimum Period

Symbol	Parameter	Min Input Period	Units
TC_2	TCLK/TIOA/TIOB Minimum Input Period	$5(t_{CPMCK}/2)$	ns

Figure 10. Timer Input



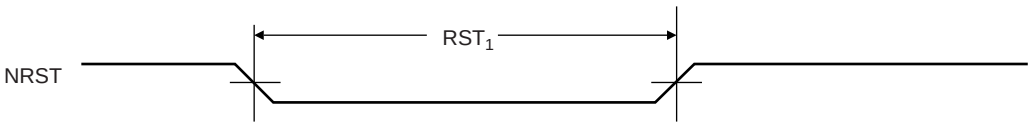
Reset Signals

A minimum pulse width is necessary, as shown in Table 35 and as represented in Figure 11.

Table 35. Reset Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
RST_1	NRST Minimum Pulse Width	310	µs

Figure 11. Reset Signal



Only the NRST rising edge is synchronized with MCK. The falling edge is asynchronous.

Advanced Interrupt Controller Signals

Inputs must meet the minimum pulse width and minimum input period shown in Table 36 and Table 37, and represented in Figure 12.

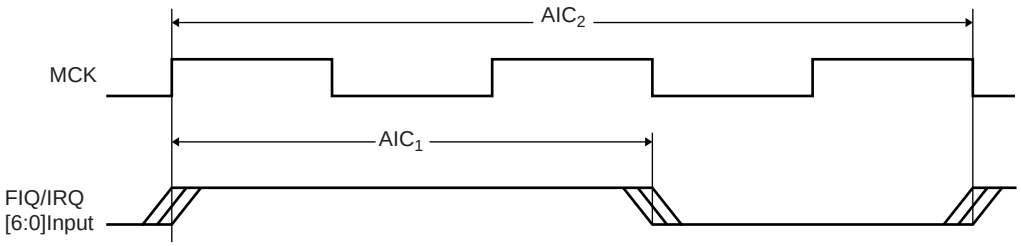
Table 36. AIC Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
AIC_1	FIQ/IRQ[6:0] Minimum Pulse Width	$3(t_{CPMCK}/2)$	ns

Table 37. AIC Input Minimum Period

Symbol	Parameter	Min Input Period	Units
AIC_2	AIC Minimum Input Period	$5(t_{CPMCK}/2)$	ns

Figure 12. AIC Signals



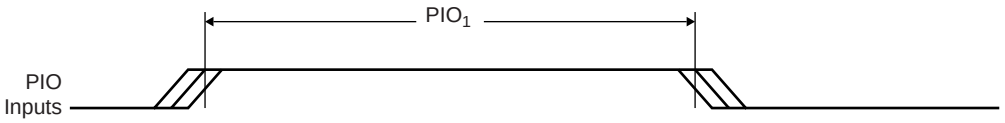
Parallel I/O Signals

The inputs must meet the minimum pulse width shown in Table 38 and represented in Figure 13.

Table 38. PIO Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
PIO_1	PIO Input Minimum Pulse Width	$3(t_{CPMCK}/2)$	ns

Figure 13. PIO Signal

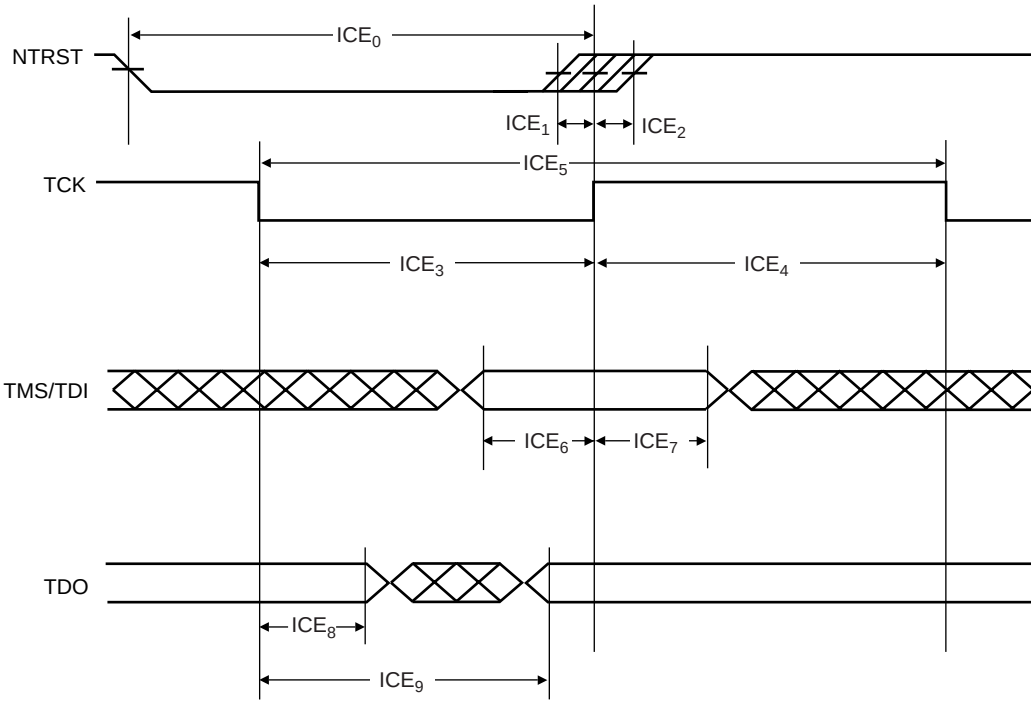


ICE Interface Signals

Table 39. ICE Interface Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
ICE_0	NTRST Minimum Pulse Width		19.3		ns
ICE_1	NTRST High Recovery to TCK High		0.4		ns
ICE_2	NTRST High Removal from TCK High		0.5		ns
ICE_3	TCK Low Half-period		42.3		ns
ICE_4	TCK High Half-period		40.3		ns
ICE_5	TCK Period		82.5		ns
ICE_6	TDI, TMS, Setup before TCK High		0.9		ns
ICE_7	TDI, TMS, Hold after TCK High		0.7		ns
ICE_8	TDO Hold Time	C_{TDO} = 0 pF	6.4		ns
		C_{TDO} derating	0		ns/pF
ICE_9	TCK Low to TDO Valid	C_{TDO} = 0 pF		14	ns
		C_{TDO} derating		0.092	ns/pF

Figure 14. ICE Interface Signal

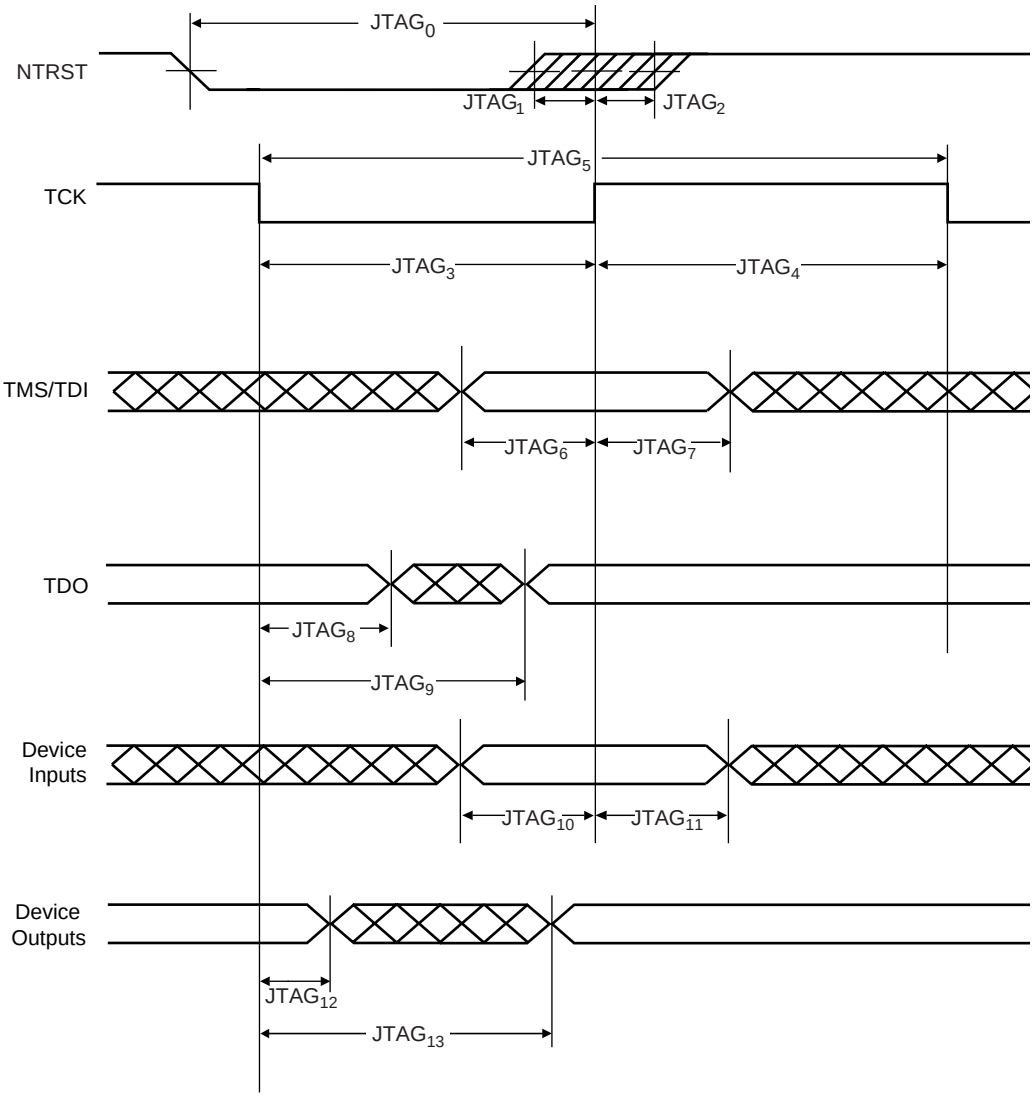


JTAG Interface Signals

Table 40. JTAG Interface Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
$JTAG_0$	NTRST Minimum Pulse Width		19.3		ns
$JTAG_1$	NTRST High Recovery to TCK Toggle		-0.1		ns
$JTAG_2$	NTRST High Removal from TCK Toggle		2.7		ns
$JTAG_3$	TCK Low Half-period		10.9		ns
$JTAG_4$	TCK High Half-period		3		ns
$JTAG_5$	TCK Period		13.8		ns
$JTAG_6$	TDI, TMS Setup before TCK High		1.5		ns
$JTAG_7$	TDI, TMS Hold after TCK High		1.9		ns
$JTAG_8$	TDO Hold Time	C_{TDO} = 0 pF	3.8		ns
		C_{TDO} derating	0		ns/pF
$JTAG_9$	TCK Low to TDO Valid	C_{TDO} = 0 pF		8.5	ns
		C_{TDO} derating		0.086	ns/pF
$JTAG_{10}$	Device Inputs Setup Time		-0.4		ns
$JTAG_{11}$	Device Inputs Hold Time		3.4		ns
$JTAG_{12}$	Device Outputs Hold Time	C_{OUT} = 0 pF	5.3		ns
		C_{OUT} derating	0		ns/pF
$JTAG_{13}$	TCK to Device Outputs Valid	C_{OUT} = 0 pF		12.6	ns
		C_{OUT} derating		0.086	ns/pF

Figure 15. JTAG Interface Signal



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