

M66312P/FP

8-Bit LED Driver with Shift Register and Latched 3-State Outputs

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Description

M66312 is a LED array driver having a 8-bit serial input and parallel output shiftregister function with 3-state output latch.

This product guarantees the output electric current of 16 mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Features

- High output current $I_{OL} = 16 \text{ mA}$, $I_{OH} = -16 \text{ mA}$
- High speed (clock frequency): 30 MHz (typ)
($C_L = 50 \text{ pF}$, $V_{CC} = 5 \text{ V}$)
- Low power dissipation: 20 μW /package (max)
($V_{CC} = 5 \text{ V}$, $T_a = 25^\circ\text{C}$, quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range: $T_a = -40$ to $+85^\circ\text{C}$

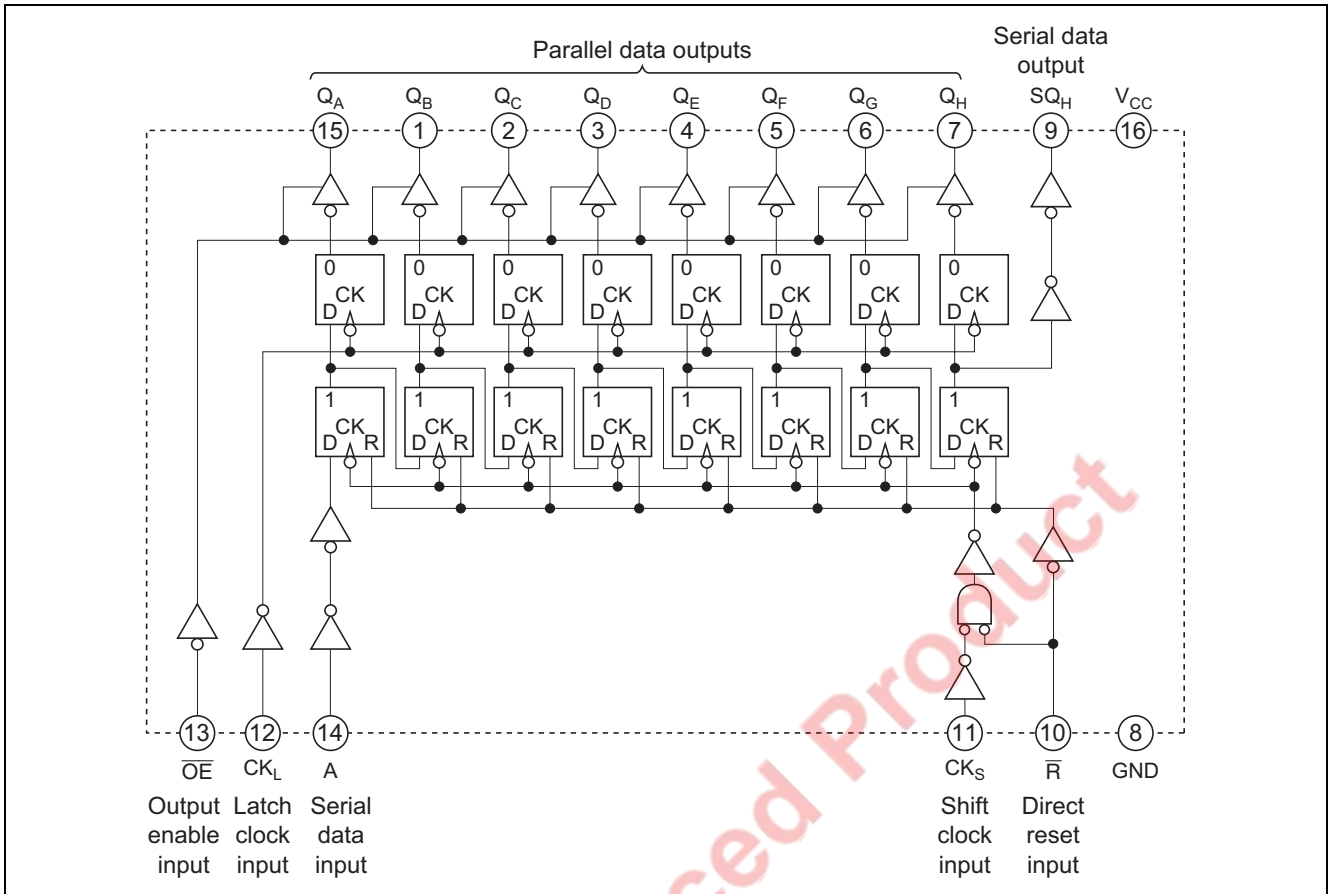
Application

LED array drive of PRINTER

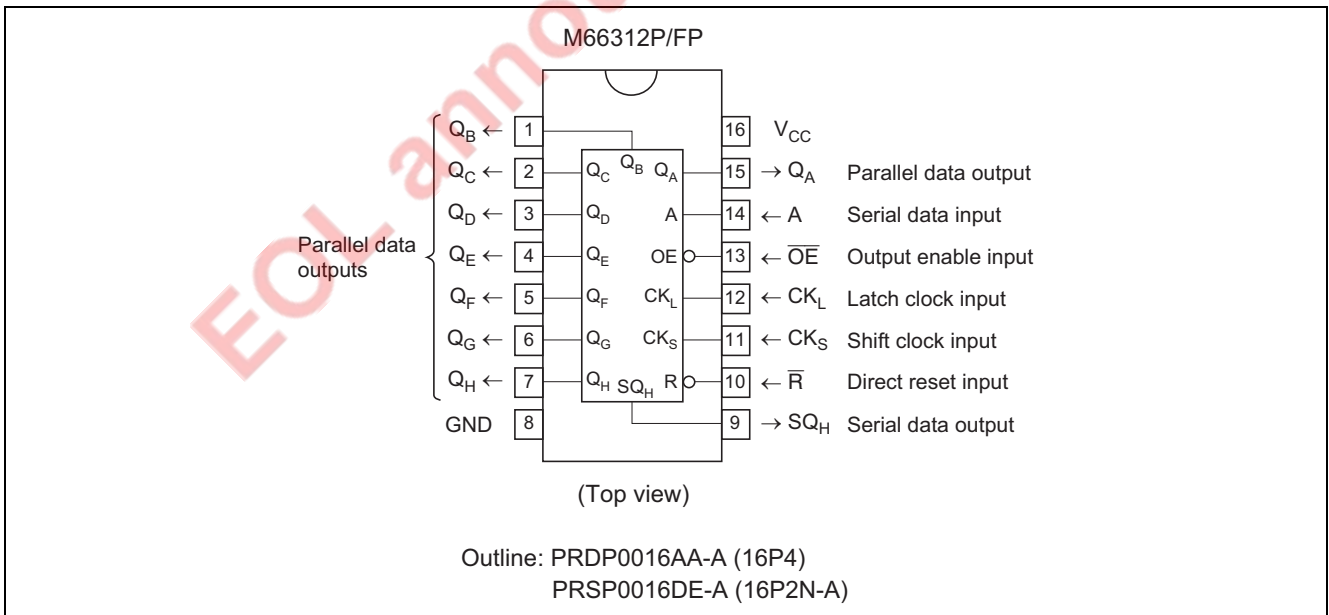
LED array drive of BUTTON TELEPHONE

EOL announced Product

Block Diagram



Pin Arrangement



Functional Description

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when “L” changes to “H”.

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S . When A is “H”, the signal of “H” shifts. When A is “L”, the signal of “L” shifts.

When the pulse is impressed to CK_L , the contents of the shifting register at that time are stored in a latching register, and they appear in the output from Q_A through Q_H are 3-state outputs.

To extend the number of bits, serial data output SQ_H is used to output the 8-bit of the shift register.

By connecting CK_S and CK_L , the shift register state delayed by 1 clock cycle is output at Q_A through Q_H .

When reset input \bar{R} is low, shift register and SQ_H will be reset. To reset Q_A through Q_H to low-level, CK_L must be changed from low-level to high-level after the shift register is reset by \bar{R} .

When output-enable input \overline{OE} is high, Q_A through Q_H will become high impedance state, but SQ_H is not changed.

Even if \overline{OE} is changed, shift operation is not affected.

Function Table ^(Note)

Operation Mode		Input					Parallel Data Output								Serial Data Output SQ_H
		\bar{R}	CK_S	CK_L	A	\overline{OE}	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	
Reset	Shift t1	L	X	X	X	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	L
	Latch t2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift latch operation	Shift t1	H	↑	X	H	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t2	H	X	↑	X	L	H	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
	Shift t1	H	↑	X	L	L	Q_A^0	Q_B^0	Q_C^0	Q_D^0	Q_E^0	Q_F^0	Q_G^0	Q_H^0	q_G^0
	Latch t2	H	X	↑	X	L	L	q_A^0	q_B^0	q_C^0	q_D^0	q_E^0	q_F^0	q_G^0	q_G^0
3 state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	q_H

- Note
- ↑: Change from low-level to high-level
 - Q^0 : Output state Q before CK_L changed
 - X: Irrelevant
 - q^0 : Contents of shift register before CK_S changed
 - q: Contents of shift register
 - t_1, t_2 : t_2 is set after t_1 is set
 - Z: High impedance

Absolute Maximum Ratings

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.5 to +7.0	V	
Input voltage	V _I	-0.5 to V _{CC} + 0.5	V	
Output voltage	V _O	-0.5 to V _{CC} + 0.5	V	
Input protection diode current	I _{IK}	-20	mA	V _I < 0 V
		20		V _I > V _{CC}
Output parasitic diode current	I _{OK}	-20	mA	V _O < 0 V
		20		V _O > V _{CC}
Output current per output pin	Q _A to Q _H	±35	mA	
	SQ _H	±25		
Supply/GND current	I _{CC}	±132	mA	V _{CC} , GND
Power dissipation	P _d	500	mW	(Note)
Storage temperature range	T _{stg}	-65 to +150	°C	

Note: M66312FP; Ta = -40 to +70°C, Ta = 70 to 85°C are derated at -6 mW/°C.

Recommended Operating Conditions

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V _{CC}	4.5	5	5.5	V
Input voltage	V _I	0	—	V _{CC}	V
Output voltage	V _O	0	—	V _{CC}	V
Operating temperature range	T _{opr}	-40	—	+85	°C
Input rising and falling time	V _{CC} = 4.5 V	tr, tf	0	—	ns
	V _{CC} = 5.5 V		0	—	

Electrical Characteristics

(V_{CC} = 4.5 to 5.5V, unless otherwise noted)

Item	Sym bol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = -40 to +85°C				
		Min	Typ	Max	Min	Max			
High-level input voltage	V _{IH}	0.70×V _{CC}	—	—	0.70×V _{CC}	—	V	V _O = 0.1 V, V _{CC} = 0.1 V I _O = 20 μA	
Low-level Input voltage	V _{IL}	—	—	0.30×V _{CC}	—	0.30×V _{CC}	V	V _O = 0.1 V, V _{CC} = 0.1 V I _O = 20 μA	
High-level output voltage Q _A to Q _H	V _{OH}	V _{CC} -0.1	—	—	V _{CC} -0.1	—	V	V _I = V _{IH} , V _{IL} V _{CC} = 4.5 V	I _{OH} = -20 μA
		3.70 ^(note)	—	—	3.55 ^(note)	—			I _{OH} = -16 mA
High-level output voltage SQ _H	V _{OH}	V _{CC} -0.1	—	—	V _{CC} -0.1	—	V	V _I = V _{IH} , V _{IL} V _{CC} = 4.5 V	I _{OH} = -20 μA
		4.0	—	—	3.9	—			I _{OH} = -4 mA
Low-level output voltage Q _A to Q _H	V _{OL}	—	—	0.1	—	0.1	V	V _I = V _{IH} , V _{IL} V _{CC} = 4.5 V	I _{OL} = 20 μA
		—	—	0.7 ^(note)	—	0.85 ^(note)			I _{OL} = 16 mA
Low-level output voltage SQ _H	V _{OL}	—	—	0.1	—	0.1	V	V _I = V _{IH} , V _{IL} V _{CC} = 4.5 V	I _{OL} = 20 μA
		—	—	0.4	—	0.5			I _{OL} = 4 mA
High-level input current	I _{IH}	—	—	0.1	—	1.0	μA	V _I = V _{CC} , V _{CC} = 5.5 V	
Low-level input current	I _{IL}	—	—	-0.1	—	-1.0	μA	V _I = GND, V _{CC} = 5.5 V	
Off state high-level output current Q _A to Q _H	I _{OZH}	—	—	1.0	—	10.0	μA	V _I = V _{IH} , V _{IL} V _{CC} = 5.5 V	V _O = V _{CC}
Off state low-level output current Q _A to Q _H	I _{OZL}	—	—	-1.0	—	-10.0	μA		V _O = GND
Quiescent supply current	I _{CC}	—	—	4.0	—	40.0	μA	V _I = V _{CC} , GND, V _{CC} = 5.5 V	

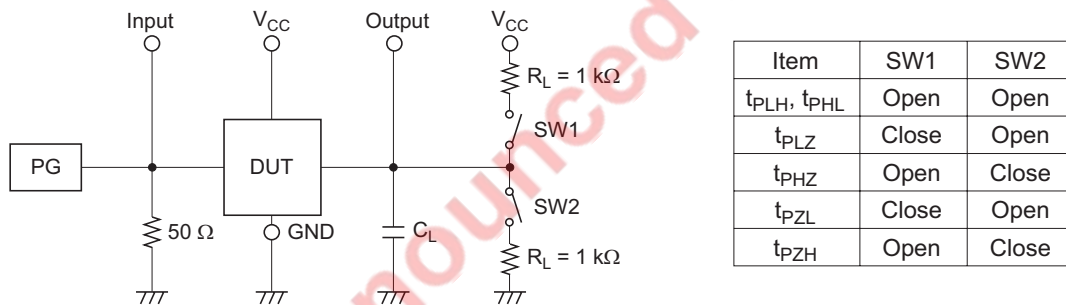
Note: Limits of single PIN operating state

Switching Characteristics

(V_{CC} = 5 V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = -40 to +85°C			
		Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	15	—	—	12	—	MHz	C _L = 50 pF
Low-level to high-level and high-level to low-level output propagation time CK _S -SQ _H	t _{PLH}	—	—	70	—	88	ns	C _L = 15 pF (Note)
	t _{PHL}	—	—	70	—	88	ns	
High-level to low-level output propagation time \bar{R} -SQ _H	t _{PHL}	—	—	60	—	76	ns	
Low-level to high-level and high-level to low-level output propagation time CK _L -Q _A to Q _H	t _{PLH}	—	—	60	—	76	ns	C _L = 50 pF (Note)
	t _{PHL}	—	—	60	—	76	ns	
Output disable time from low-level and high-level $\bar{O}\bar{E}$ -Q _A to Q _H	t _{PLZ}	—	—	50	—	64	ns	C _L = 5 pF (Note)
	t _{PHZ}	—	—	50	—	64	ns	
Output enable time to low-level and high-level $\bar{O}\bar{E}$ -Q _A to Q _H	t _{PZL}	—	—	56	—	70	ns	C _L = 50 pF (Note)
	t _{PZH}	—	—	56	—	70	ns	

Note: Test Circuit



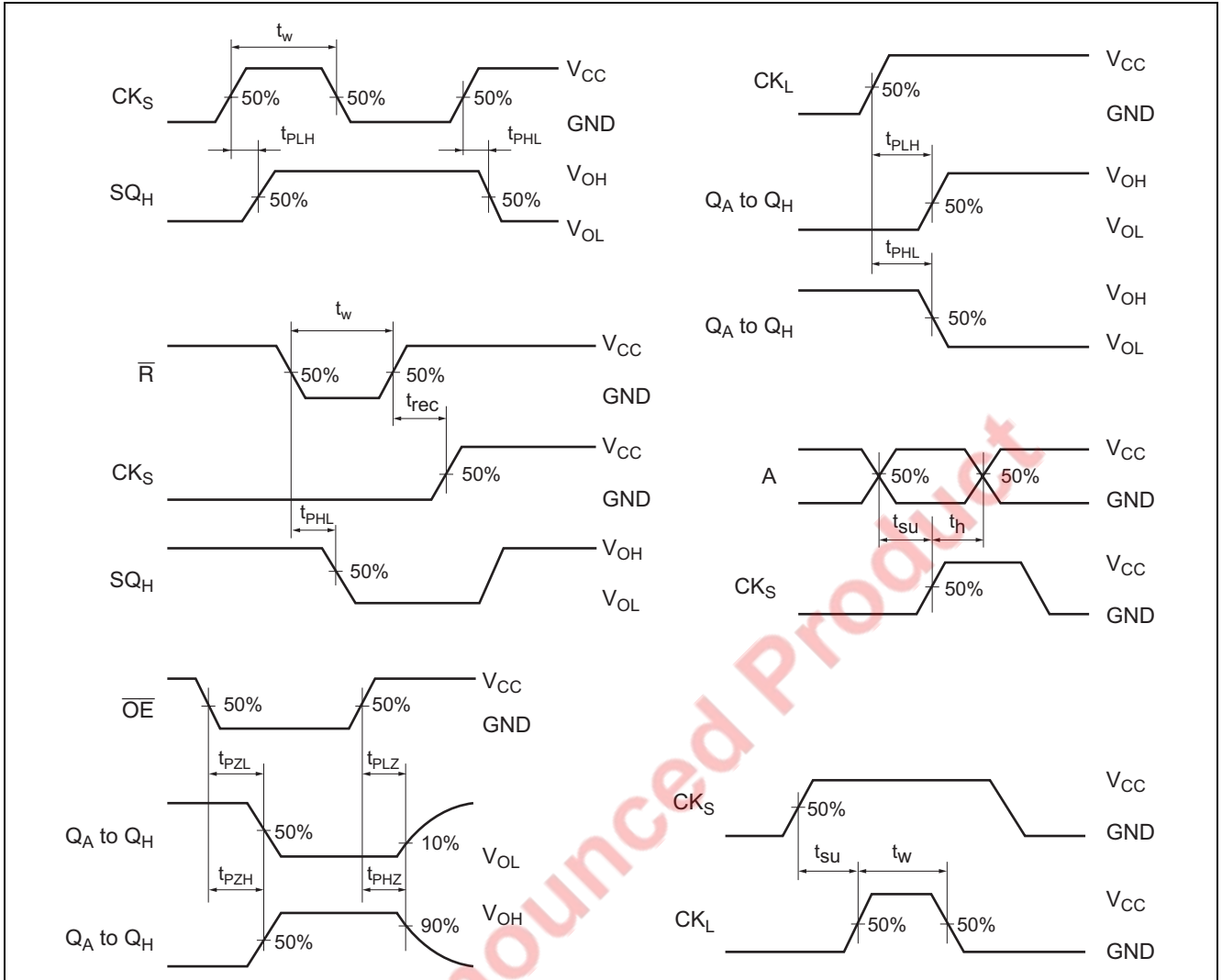
- (1) The pulse generator (PG) has the following characteristics (10% to 90%): tr = 6 ns, tf = 6 ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

Timing Requirements

(V_{CC} = 5 V)

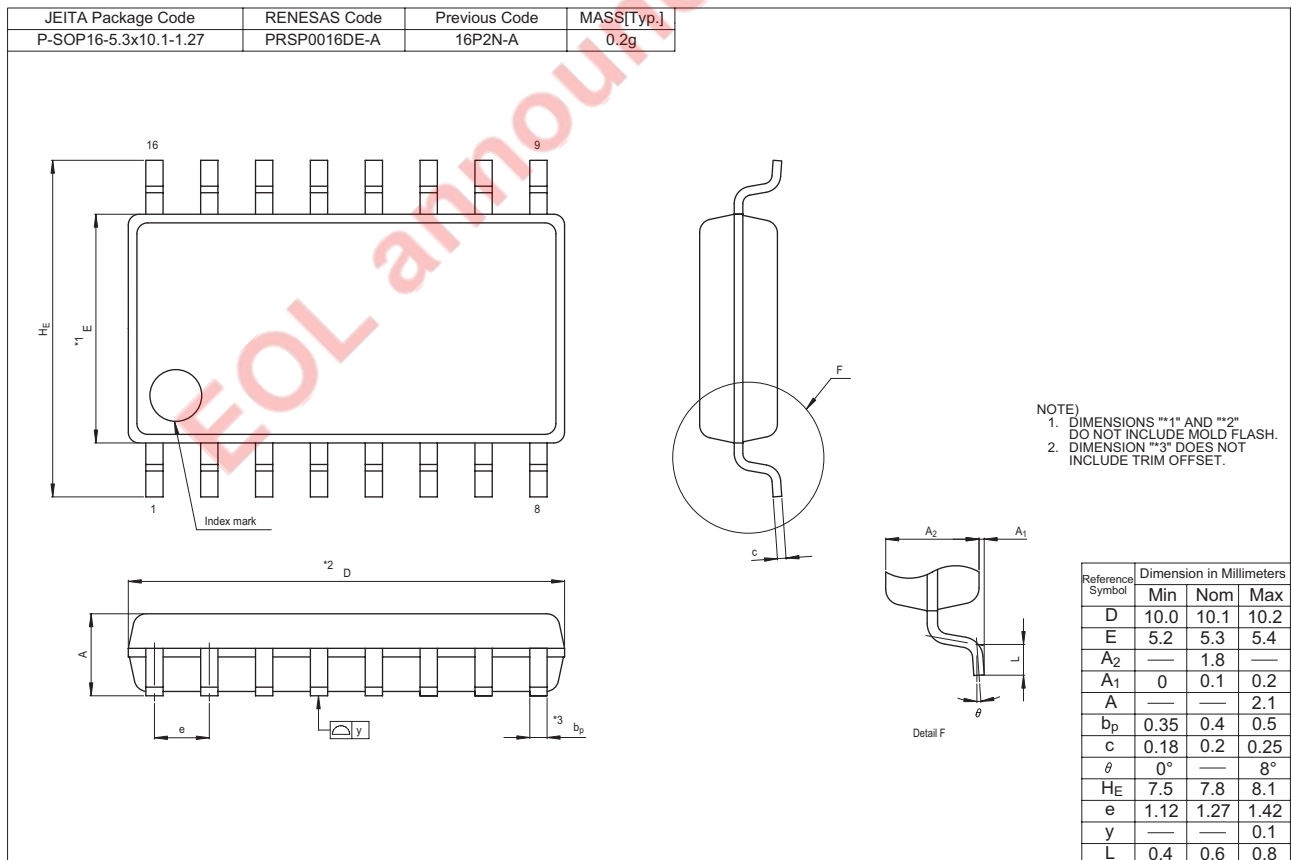
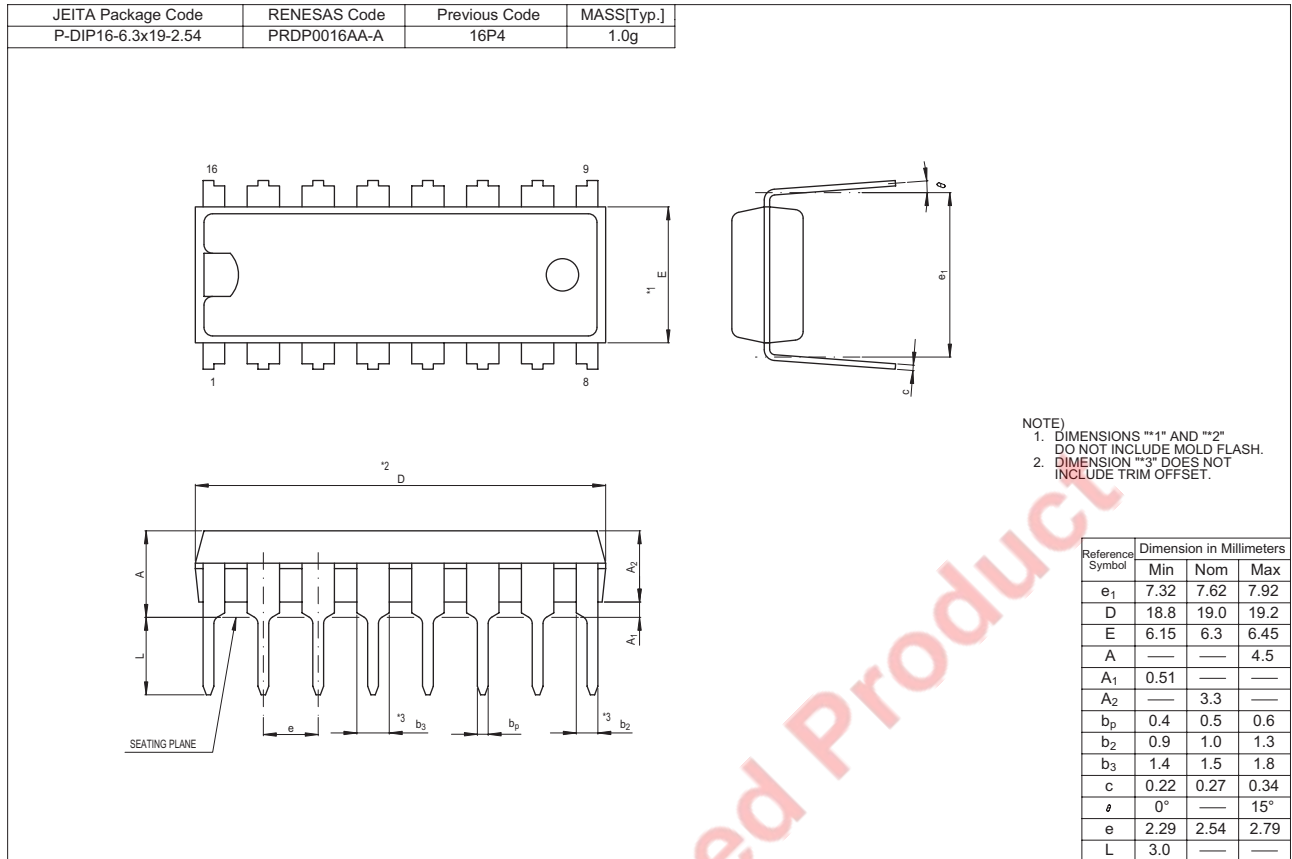
Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = -40 to +85°C			
		Min	Typ	Max	Min	Max		
CK _S , CK _L , \bar{R} pulse width	t _w	32	—	—	40	—	ns	
A setup time with respect to CK _S	t _{su}	40	—	—	50	—	ns	
CK _S setup time with respect to CK _L	t _{su}	40	—	—	50	—	ns	
A hold time with respect to CK _S	t _h	10	—	—	10	—	ns	
\bar{R} recovery time with respect to CK _S	t _{rec}	20	—	—	26	—	ns	

Timing Chart



EOL announced Product

Package Dimensions



Notes:

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Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510