

M66313FP

32-Bit LED Driver with Shift Register and Latch

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Description

The M66313FP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel-output shift register, equipped with direct set input and output latches.

The M66313FP guarantees sufficient 24 mA output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output.

The parallel outputs are open-drain outputs.

The M66313FP employs CMOS technology, allowing considerable reduction of power dissipation, compared to previous BIPOLAR or Bi-CMOS products.

In addition, the pin configuration is suitable for easy wiring on the printed circuit board.

Features

- High output current.
All parallel output $I_{OL} = +24$ mA, LEDs can be turned on simultaneously.
- Low power dissipation : 200 μ W/package (max)
($V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$, quiescent state)
- High noise margin
Employment of Schmitt-trigger circuit on all inputs allows application with long wiring.
- Direct set input (\overline{S}_D)
- Open-drain output (\overline{Q}_1 to \overline{Q}_{32})
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range ($T_a = -40$ to $+85^\circ\text{C}$)
- Pin configuration for easy layout on PCB.
(Pin configuration allows easy cascade connection or LED connection)

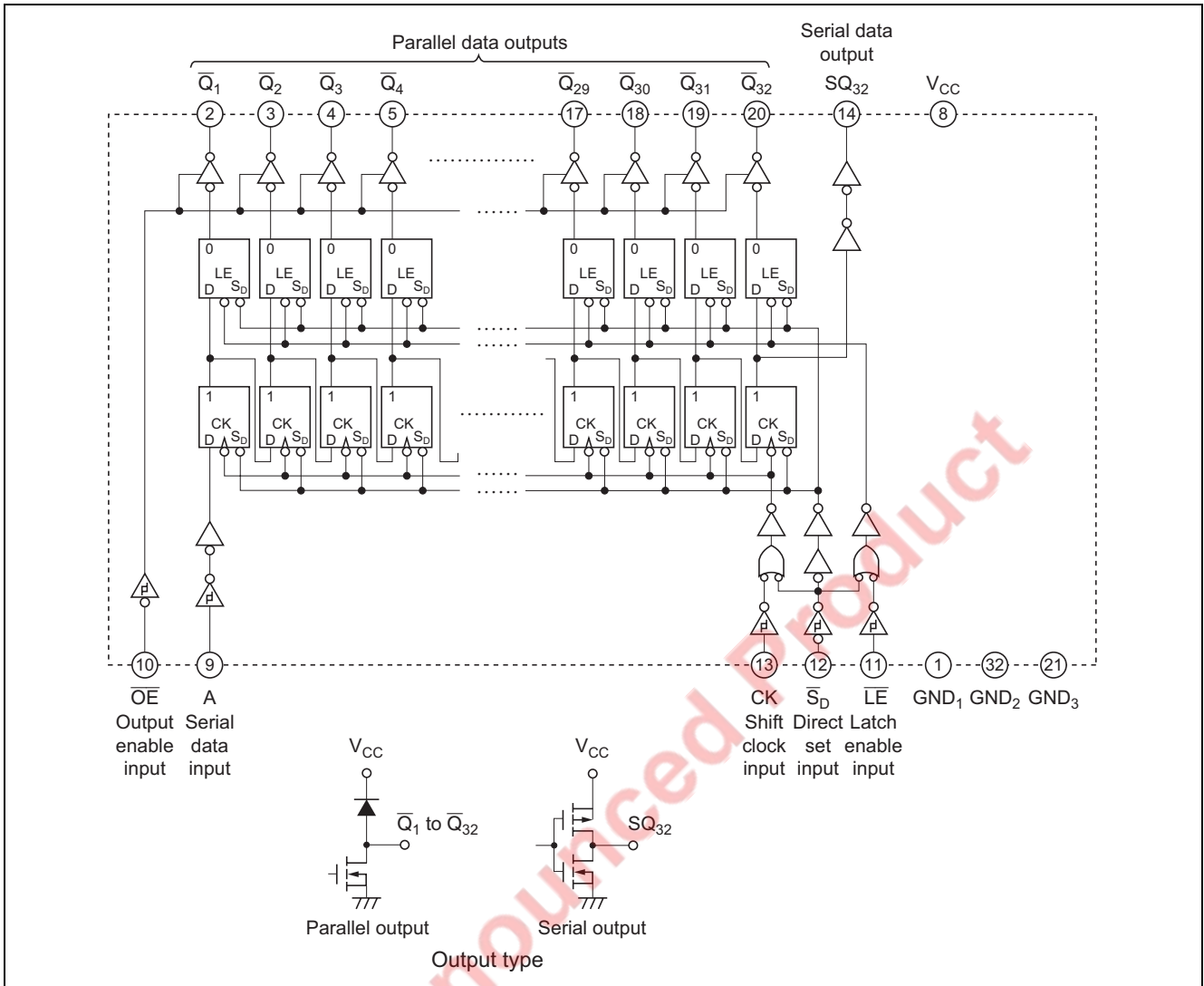
Application

LED array drive for eraser unit of a copying machine

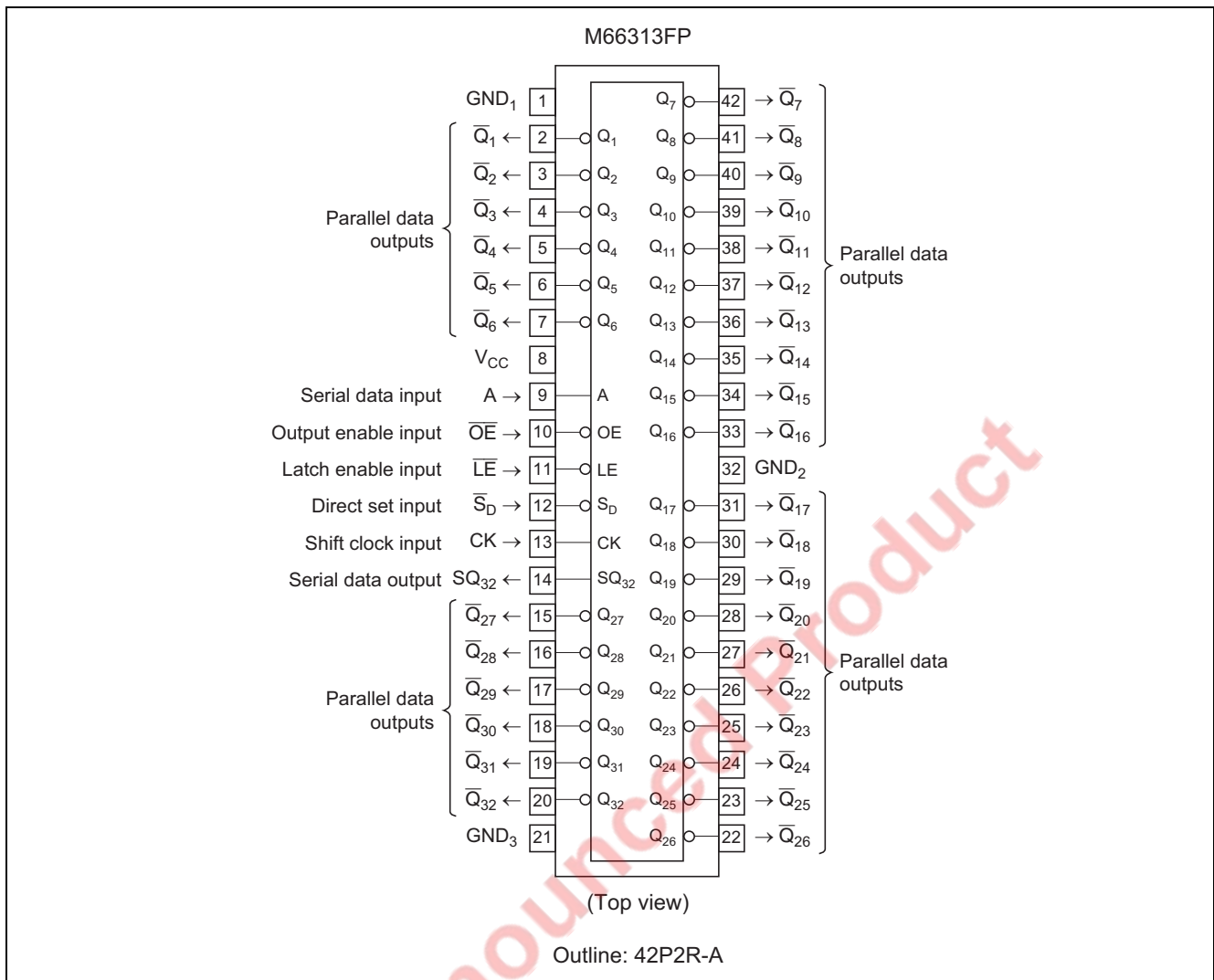
LED array drive of a button telephone set

Various LED modules

Block Diagram



Pin Arrangement



Functional Description

The employment of silicon gate CMOS process of the M66313FP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the clock input CK changes from low-level to high-level.

The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

The parallel outputs \bar{Q}_1 to \bar{Q}_{32} are open-drain outputs.

If the latch-enable input \bar{LE} is turned high-level, the content of the shift register at that instant is latched.

To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the 32nd bit.

If the direct set input \bar{S}_D is turned low-level, shift register and latches are set.

If the high-level input is applied to the output enable input \bar{OE} , \bar{Q}_1 to \bar{Q}_{32} are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift operation is not affected when \bar{OE} is changed.

Function Table (Note)

Operation Mode	Input				Parallel Data Output																												Serial Data Output SQ ₃₂					
	S _D	CK	LE	A	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉	Q ₁₀	Q ₁₁	Q ₁₂	Q ₁₃	Q ₁₄	Q ₁₅	Q ₁₆	Q ₁₇	Q ₁₈	Q ₁₉	Q ₂₀	Q ₂₁	Q ₂₂	Q ₂₃	Q ₂₄	Q ₂₅	Q ₂₆	Q ₂₇	Q ₂₈		Q ₂₉	Q ₃₀	Q ₃₁	Q ₃₂	
Set	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	
Shift	H	↑	L	H	L	L	Q ⁰ ₁	Q ⁰ ₂	Q ⁰ ₃	Q ⁰ ₄	Q ⁰ ₅	Q ⁰ ₆	Q ⁰ ₇	Q ⁰ ₈	Q ⁰ ₉	Q ⁰ ₁₀	Q ⁰ ₁₁	Q ⁰ ₁₂	Q ⁰ ₁₃	Q ⁰ ₁₄	Q ⁰ ₁₅	Q ⁰ ₁₆	Q ⁰ ₁₇	Q ⁰ ₁₈	Q ⁰ ₁₉	Q ⁰ ₂₀	Q ⁰ ₂₁	Q ⁰ ₂₂	Q ⁰ ₂₃	Q ⁰ ₂₄	Q ⁰ ₂₅	Q ⁰ ₂₆	Q ⁰ ₂₇	Q ⁰ ₂₈	Q ⁰ ₂₉	Q ⁰ ₃₀	Q ⁰ ₃₁	q ⁰ ₃₁
	H	↑	L	L	L	Z	Q ⁰ ₁	Q ⁰ ₂	Q ⁰ ₃	Q ⁰ ₄	Q ⁰ ₅	Q ⁰ ₆	Q ⁰ ₇	Q ⁰ ₈	Q ⁰ ₉	Q ⁰ ₁₀	Q ⁰ ₁₁	Q ⁰ ₁₂	Q ⁰ ₁₃	Q ⁰ ₁₄	Q ⁰ ₁₅	Q ⁰ ₁₆	Q ⁰ ₁₇	Q ⁰ ₁₈	Q ⁰ ₁₉	Q ⁰ ₂₀	Q ⁰ ₂₁	Q ⁰ ₂₂	Q ⁰ ₂₃	Q ⁰ ₂₄	Q ⁰ ₂₅	Q ⁰ ₂₆	Q ⁰ ₂₇	Q ⁰ ₂₈	Q ⁰ ₂₉	Q ⁰ ₃₀	Q ⁰ ₃₁	q ⁰ ₃₁
Latch	H	X	H	X	L	Q ⁰ ₁	Q ⁰ ₂	Q ⁰ ₃	Q ⁰ ₄	Q ⁰ ₅	Q ⁰ ₆	Q ⁰ ₇	Q ⁰ ₈	Q ⁰ ₉	Q ⁰ ₁₀	Q ⁰ ₁₁	Q ⁰ ₁₂	Q ⁰ ₁₃	Q ⁰ ₁₄	Q ⁰ ₁₅	Q ⁰ ₁₆	Q ⁰ ₁₇	Q ⁰ ₁₈	Q ⁰ ₁₉	Q ⁰ ₂₀	Q ⁰ ₂₁	Q ⁰ ₂₂	Q ⁰ ₂₃	Q ⁰ ₂₄	Q ⁰ ₂₅	Q ⁰ ₂₆	Q ⁰ ₂₇	Q ⁰ ₂₈	Q ⁰ ₂₉	Q ⁰ ₃₀	Q ⁰ ₃₁	q ₃₂	
Output disable	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q ₃₂	

Note ↑: Transition from low-to-high-level.
 Q⁰: Shows the status of output Q before CK input changes.
 X: Irrelevant
 q⁰: The content of shift register before CK changes.
 q: The content of the shift register.
 Z: High-impedance state.

Absolute Maximum Ratings

(Ta = -40 to +85°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.5 to +7.0	V	
Input voltage	V _I	-0.5 to V _{CC} + 0.5	V	
Output voltage	V _O	-0.5 to V _{CC} + 0.5	V	
Input protection diode current	I _{IK}	-20	mA	V _I < 0 V
		20		V _I > V _{CC}
Output parasitic diode current	I _{OK}	-20	mA	V _O < 0 V
		20		V _O > V _{CC}
Output current	Q ₁ to Q ₃₂	50	mA	
	SQ ₃₂	±25		
Supply/GND current	I _{CC}	-920, +20	mA	V _{CC} , GND
Power dissipation	P _d	650	mW	
Storage temperature range	T _{stg}	-65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V _{CC}	4.5	5	5.5	V
Input voltage	V _I	0	—	V _{CC}	V
Output voltage	V _O	0	—	V _{CC}	V
Operating free-air ambient temperature range	Topr	-40	—	+85	°C

Electrical Characteristics

(V_{CC} = 4.5 to 5.5 V, unless otherwise noted)

Item	Sym bol	Limits					Unit	Conditions		
		Ta = 25°C			Ta = -40 to +85°C					
		Min	Typ (Note1)	Max	Min	Max				
Positive-going threshold voltage	V _{T+}	0.35×V _{CC}	2.8	0.7×V _{CC}	0.35×V _{CC}	0.7×V _{CC}	V	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA		
Negative-going threshold voltage	V _{T-}	0.2×V _{CC}	2	0.55×V _{CC}	0.2×V _{CC}	0.55×V _{CC}	V	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA		
High-level output voltage	SQ ₃₂	V _{OH}	V _{CC} - 0.1	—	—	V _{CC} - 0.1	—	V	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	I _{OH} = -20μA
			3.83	—	—	3.66	—			I _{OH} = -4mA
Low-level output voltage	Q ₁ to Q ₃₂	V _{OL}	—	—	0.1	—	0.1	V	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	I _{OL} = 20μA
			—	0.20	0.41	—	0.50			I _{OL} = 24mA
			—	0.25	0.48	—	0.55 (Note 2)			I _{OL} = 28mA
			—	—	0.1	—	0.1			I _{OL} = 20μA
	SQ ₃₂	—	—	0.44	—	0.53	I _{OL} = 4mA			
High-level input current	I _{IH}	—	—	0.5	—	5.0	μA	V _I = V _{CC} , V _{CC} = 5.5V		
Low-level input current	I _{IL}	—	—	-0.5	—	-5.0	μA	V _I = GND, V _{CC} = 5.5V		
Maximum output leak current	Q ₁ to Q ₃₂	I _O	—	—	1.0	—	10.0	μA	V _I = V _{T+} , V _{T-} V _{CC} = 5.5V	V _O = V _{CC}
			—	—	-1.0	—	-10.0			V _O = GND
Quiescent state dissipation current	I _{CC}	—	—	40.0	—	400.0	μA	V _I = V _{CC} , GND, V _{CC} = 5.5V		

Note: 1. All typical values are at V_{CC} = 5 V, Ta = 25°C

2. Ta = -40 to +70°C

Switching Characteristics

(V_{CC} = 5V)

Item	Symbol	Limits					Unit	Conditions	
		Ta = 25°C			Ta = -40 to +85°C				
		Min	Typ	Max	Min	Max			
Maximum clock frequency	f _{max}	5	30	—	4	—	MHz	C _L = 50 pF R _L = 1 kΩ (Note 2)	
Output enable time to low-level	CK- \bar{Q}_1 to \bar{Q}_{32} (Turned on)	t _{PZL}	—	35	150	—	200		ns
Output disable time from low-level	CK- \bar{Q}_1 to \bar{Q}_{32} (Turned off)	t _{PLZ}	—	35	200	—	250		ns
Low-to-high, high-to-low output propagation time	CK-SQ ₃₂	t _{PLH}	—	35	100	—	130		ns
		t _{PHL}	—	40	100	—	130		ns
Output enable time to low-level	\bar{S}_D - \bar{Q}_1 to \bar{Q}_{32} (Turned on)	t _{PZL}	—	35	150	—	200		ns
Low-to-high output propagation time	\bar{S}_D -SQ ₃₂	t _{PLH}	—	40	100	—	130		ns
Output enable time to low-level	$\bar{L}\bar{E}$ - \bar{Q}_1 to \bar{Q}_{32} (Turned on)	t _{PZL}	—	30	100	—	130		ns
Output disable time from low-level	$\bar{L}\bar{E}$ - \bar{Q}_1 to \bar{Q}_{32} (Turned off)	t _{PLZ}	—	35	150	—	200		ns
Output enable time to low-level	$\bar{O}\bar{E}$ - \bar{Q}_1 to \bar{Q}_{32} (Turned on)	t _{PZL}	—	30	100	—	130		ns
Output disable time from low-level	$\bar{O}\bar{E}$ - \bar{Q}_1 to \bar{Q}_{32} (Turned off)	t _{PLZ}	—	35	150	—	200		ns
Input capacitance	C _I	—	3	10	—	10	pF		
Output capacitance	C _O	—	6	15	—	15	pF	$\bar{O}\bar{E}$ -V _{CC}	
Power dissipation capacitance (Note 1)	C _{PD}	—	160	—	—	—	pF		

Note 1. C_{PD} is the equivalent capacitance of IC calculated by the operating power dissipation without load. The operating power dissipation without load is given as follows.

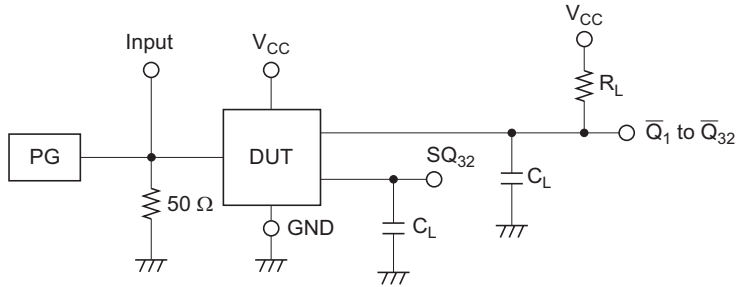
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$

Timing Requirements

(V_{CC} = 5V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = -40 to +85°C			
		Min	Typ	Max	Min	Max		
CK, \overline{LE} , \overline{SD} pulse width	t _w	100	16	—	130	—	ns	(Note 2)
Setup time A to CK	t _{su}	100	27	—	130	—	ns	
Hold time A to CK	t _h	10	5	—	15	—	ns	
Hold time \overline{LE} to CK		50	15	—	70	—	ns	
Recovery time CK to \overline{SD}	t _{rec}	50	20	—	70	—	ns	

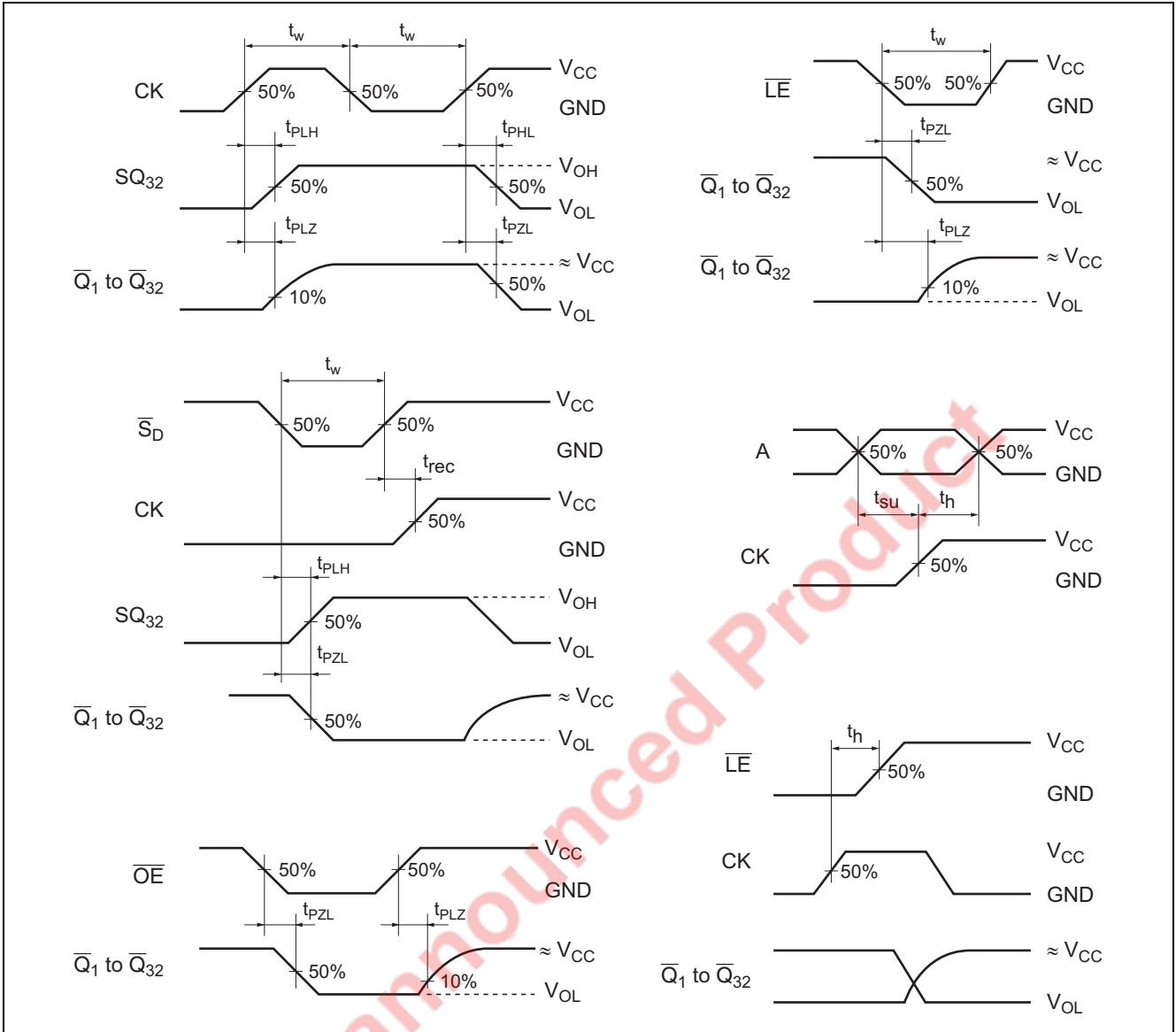
Note: 2. Test Circuit



- (1) Characteristics of pulse generator (PG): t_r = 6 ns, t_f = 6 ns
- (2) C_L includes probe and stray capacitance.

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Timing Chart



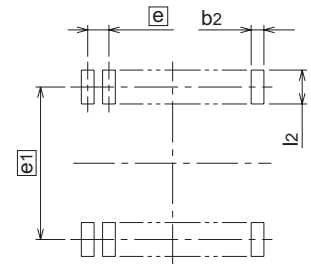
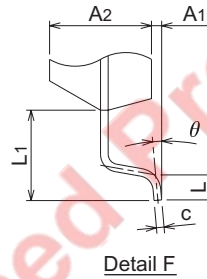
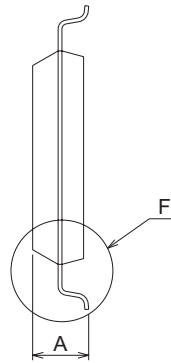
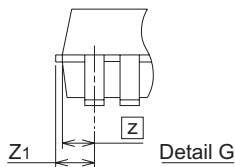
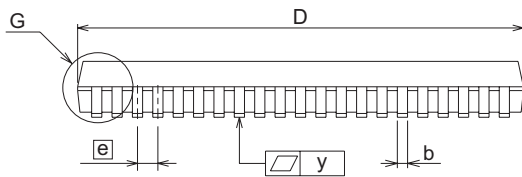
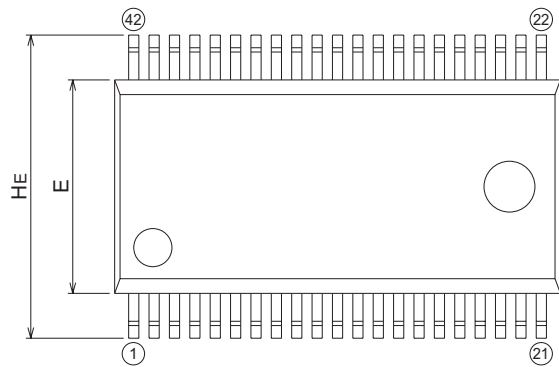
Package Dimensions

42P2R-A



Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	—	0.63	Alloy 42/Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	—	0.8	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
Z	—	0.75	—
Z1	—	—	0.9
y	—	—	0.15
theta	0°	—	10°
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—

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Notes:

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