

Silicon NPN Power Transistors

2SD211

DESCRIPTION

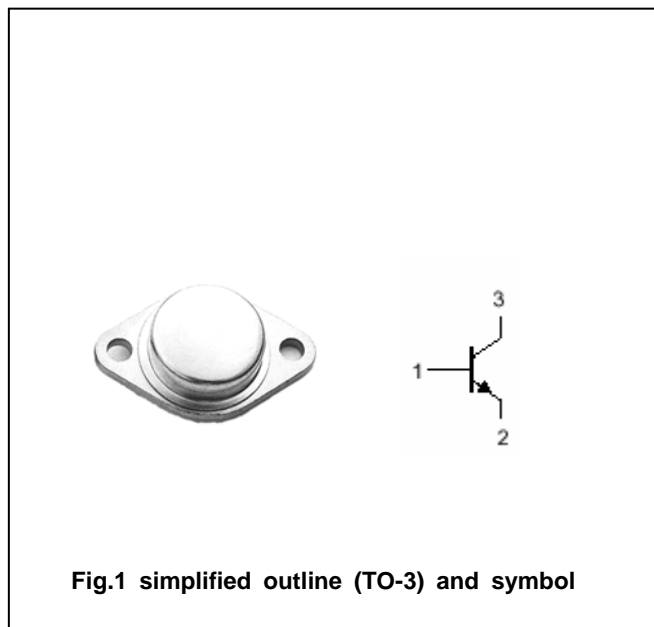
- With TO-3 package
- Large current capability
- Wide area of safe operation

APPLICATIONS

- For power amplifier and switching applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = ^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	60	V
V_{CEO}	Collector-emitter voltage	Open base	60	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		10	A
P_C	Collector power dissipation	$T_C = 25^\circ\text{C}$	100	W
T_j	Junction temperature		150	$^\circ\text{C}$
T_{stg}	Storage temperature		-55~150	$^\circ\text{C}$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =50mA ; I _B =0	60			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =5A ; I _B =0.5A			1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =5A ; I _B =0.5A			2.5	V
I _{CBO}	Collector cut-off current	V _{CB} =60V ; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =6V ; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =5A ; V _{CE} =4V	30			
f _T	Transition frequency	I _C =1A ; V _{CE} =12V		8		MHz

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PACKAGE OUTLINE

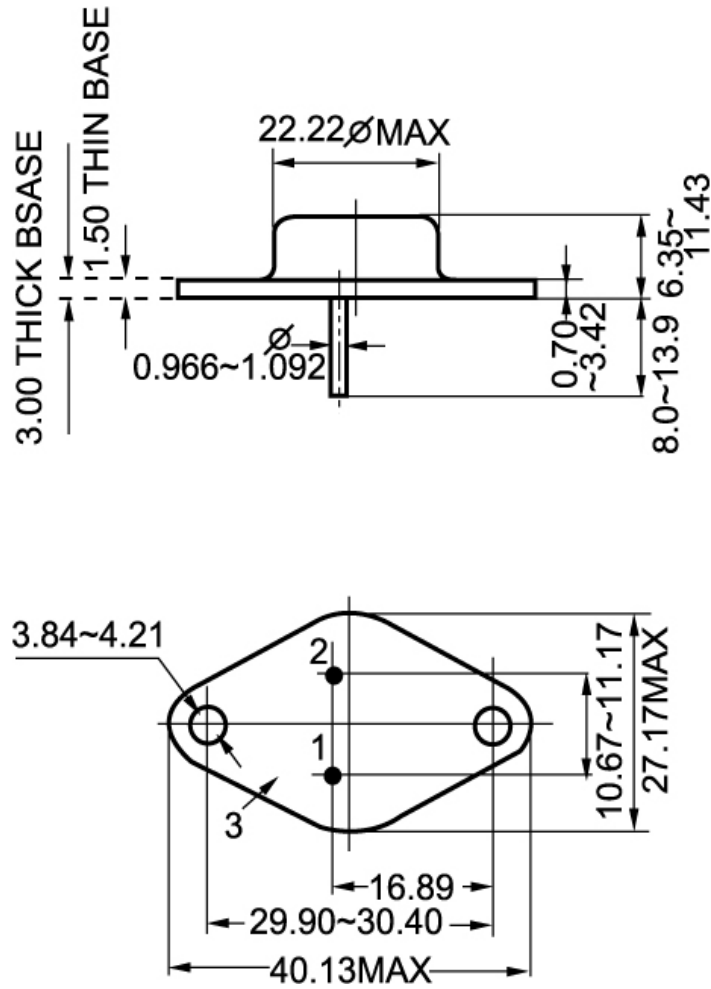


Fig.2 outline dimensions (unindicated tolerance: $\pm 0.1\text{mm}$)