BLF573S

HF / VHF power LDMOS transistor

Rev. 01 — 8 December 2008 Preliminary data sheet

1. Product profile

1.1 General description

A 300 W LDMOS RF power transistor for broadcast applications and industrial, scientific and medical applications in the HF to 500 MHz band.

Table 1. Production test information

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW	225	50	300	26.5	70

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

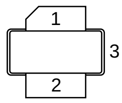
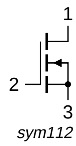
- Typical CW performance at frequency of 225 MHz, a supply voltage of 50 V and an I_{Dq} of 900 mA:
  - Average output power = 300 W
  - Power gain = 26.5 dB
  - Efficiency = 70 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF and VHF band)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF573S	-	earless flanged LDMOST ceramic package, 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	42	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 300 W [1]	0.21	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

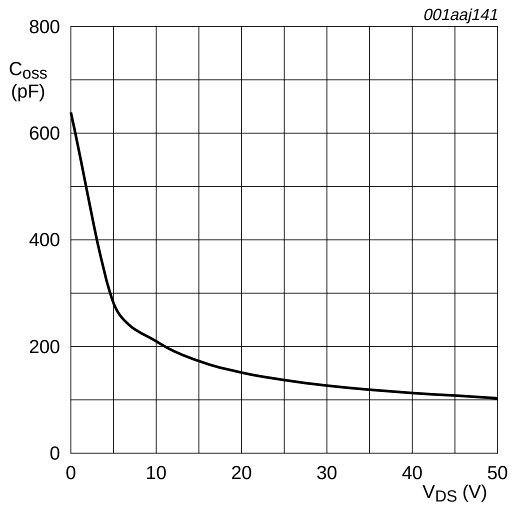
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.75 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 375 mA	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 900 mA	1.45	1.95	2.45	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	44	56	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 18.75 A	-	20	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 12.49 A	-	0.09	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	2.3	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	300	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	103	-	pF

Table 7. RF characteristics

Mode of operation: CW; f = 225 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 900 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 300 W	25	26.5	28	dB
RL_{in}	input return loss	P_L = 300 W	10	13	-	dB
η_D	drain efficiency	P_L = 300 W	67	70	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; capacitance value without internal matching

6.1 Ruggedness in class-AB operation

The BLF573S is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 900 mA; P_L = 300 W; f = 225 MHz.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Measured Z_S and Z_L test circuit impedances.

f	Z_S	Z_L
MHz	Ω	Ω
225	0.7 + j2.0	1.95 + j2.0

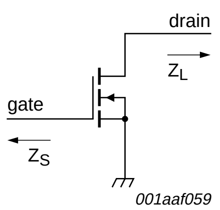
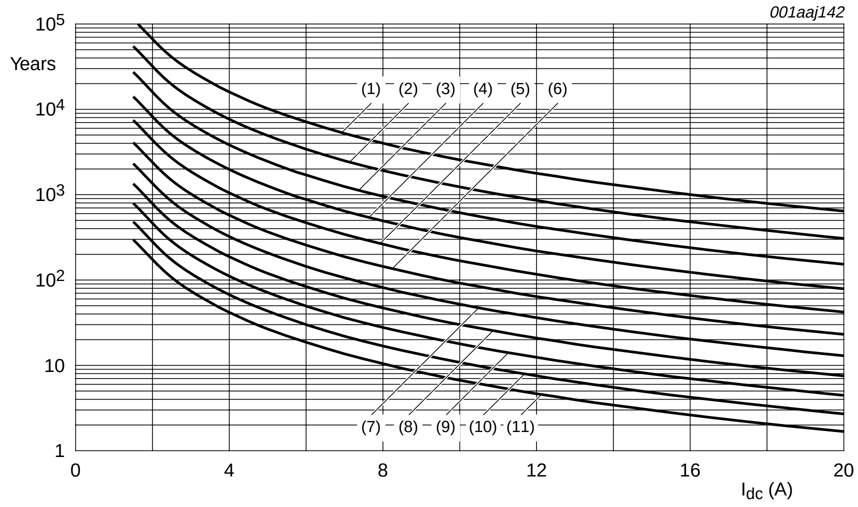


Fig 2. Definition of transistor impedance

7.2 Reliability



TTF (0.1 % failure fraction).

(1) T_j = 100 °C

(2) T_j = 110 °C

(3) T_j = 120 °C

(4) T_j = 130 °C

(5) T_j = 140 °C

(6) T_j = 150 °C

(7) T_j = 160 °C

(8) T_j = 170 °C

(9) T_j = 180 °C

(10) T_j = 190 °C

(11) T_j = 200 °C

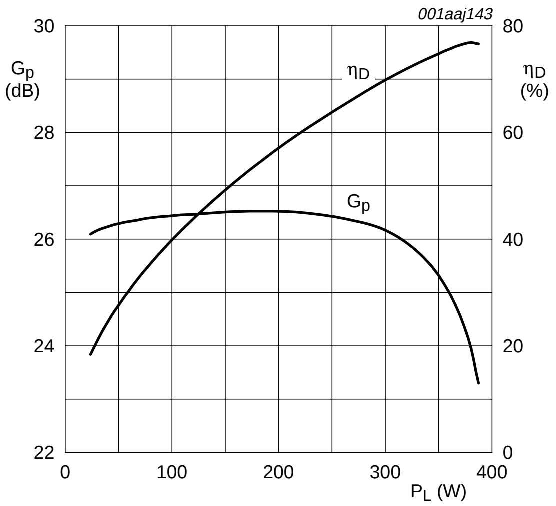
Fig 3. BLF573S electromigration (I_D, total device)

8. Test information

8.1 RF Performance

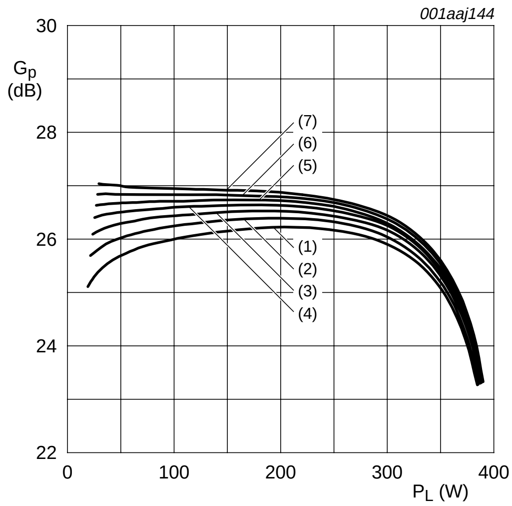
The following figures are measured in a class-AB production test circuit.

8.1.1 1-Tone CW



V_{DS} = 50 V; I_{Dq} = 900 mA; f = 225 MHz.

Fig 4. Power gain and drain efficiency as functions of load power; typical values



V_{DS} = 50 V; f = 225 MHz.

(1) I_{Dq} = 500 mA

(2) I_{Dq} = 700 mA

(3) I_{Dq} = 900 mA

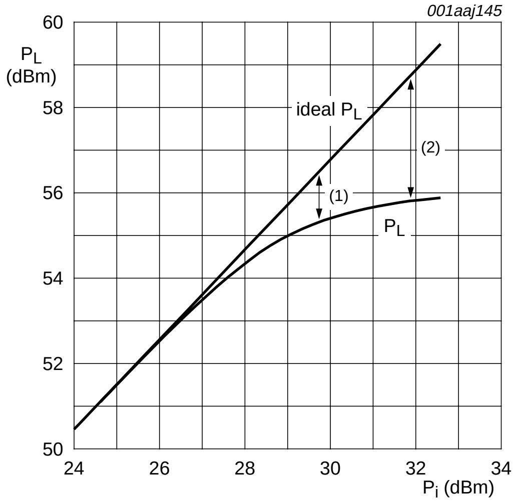
(4) I_{Dq} = 1100 mA

(5) I_{Dq} = 1300 mA

(6) I_{Dq} = 1500 mA

(7) I_{Dq} = 1700 mA

Fig 5. Power gain as function of load power; typical values



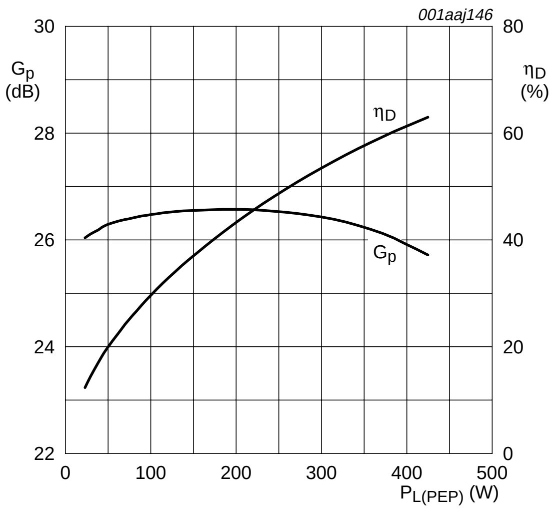
V_{DS} = 50 V; I_{Dq} = 900 mA; f = 225 MHz.

(1) $P_{L(1dB)}$ = 55.2 dBm (331 W)

(2) $P_{L(3dB)}$ = 55.8 dBm (380 W)

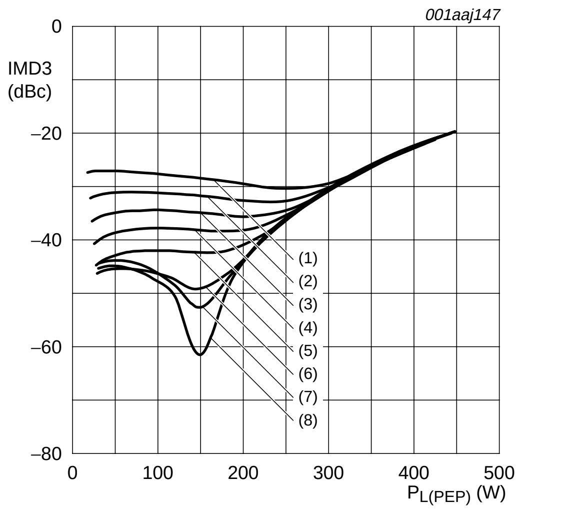
Fig 6. Load power as function of input power; typical values

8.1.2 2-Tone CW



V_{DS} = 50 V; I_{Dq} = 900 mA; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

Fig 7. Power gain and drain efficiency as functions of peak envelope load power; typical values



V_{DS} = 50 V; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

(1) I_{Dq} = 500 mA

(2) I_{Dq} = 700 mA

(3) I_{Dq} = 900 mA

(4) I_{Dq} = 1100 mA

(5) I_{Dq} = 1300 mA

(6) I_{Dq} = 1500 mA

(7) I_{Dq} = 1700 mA

(8) I_{Dq} = 1800 mA

Fig 8. Third order intermodulation distortion as a function of peak envelope load power; typical values

8.2 Test circuit

Table 9. List of components

For production test circuit, see Figure 9 and Figure 10.

Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 µm.

Component	Description	Value		Remarks
B1	ferrite SMD bead	100 Ω; 100 MHz		Ferroxcube BDS3/3/8.9-4S2 or equivalent
C1, C18	multilayer ceramic chip capacitor	100 pF	[1]	
C2	multilayer ceramic chip capacitor	39 pF	[1]	
C3, C4	multilayer ceramic chip capacitor	180 pF	[1]	
C5, C6, C7	multilayer ceramic chip capacitor	220 pF	[1]	
C8, C20	multilayer ceramic chip capacitor	1 nF	[1]	
C9	multilayer ceramic chip capacitor	4.7 µF		TDK C4532X7R1E475MT020U or equivalent
C10	multilayer ceramic chip capacitor	30 pF	[1]	
C11, C12, C13	multilayer ceramic chip capacitor	51 pF	[1]	
C14	multilayer ceramic chip capacitor	43 pF	[1]	

Table 9. List of components *...continued*

For production test circuit, see Figure 9 and Figure 10.

Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 µm.

Component	Description	Value		Remarks
C15	multilayer ceramic chip capacitor	33 pF	[1]	
C16	multilayer ceramic chip capacitor	36 pF	[1]	
C17	multilayer ceramic chip capacitor	16 pF	[1]	
C19	electrolytic capacitor	220 µF; 63 V		
L1	2 turns enamelled copper wire	D = 3 mm; d = 1 mm; length = 2 mm; leads = 2 × 6 mm		
L2	4 turns enamelled copper wire	D = 2 mm; d = 1 mm; length = 13 mm; leads = 2 × 5 mm		
L3	stripline	-		(L × W) 96 mm × 3 mm
L4, L5	stripline	-		(L × W) 15 mm × 8 mm
L6	stripline	-		(L × W) 105 mm × 6 mm
L7	stripline	-		(L × W) 3 mm × 6 mm
L8	stripline	-		(L × W) 12 mm × 6 mm
R1	metal film resistor	100 Ω; 0.6 W		

[1] American Technical Ceramics type 100B or capacitor of same quality.

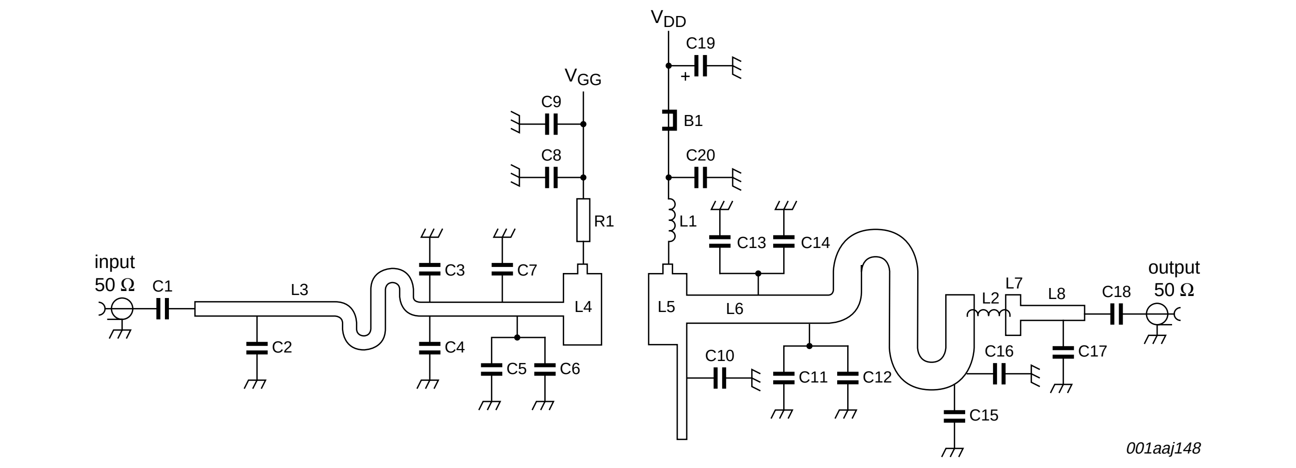


Fig 9. Class-AB common-source production test circuit

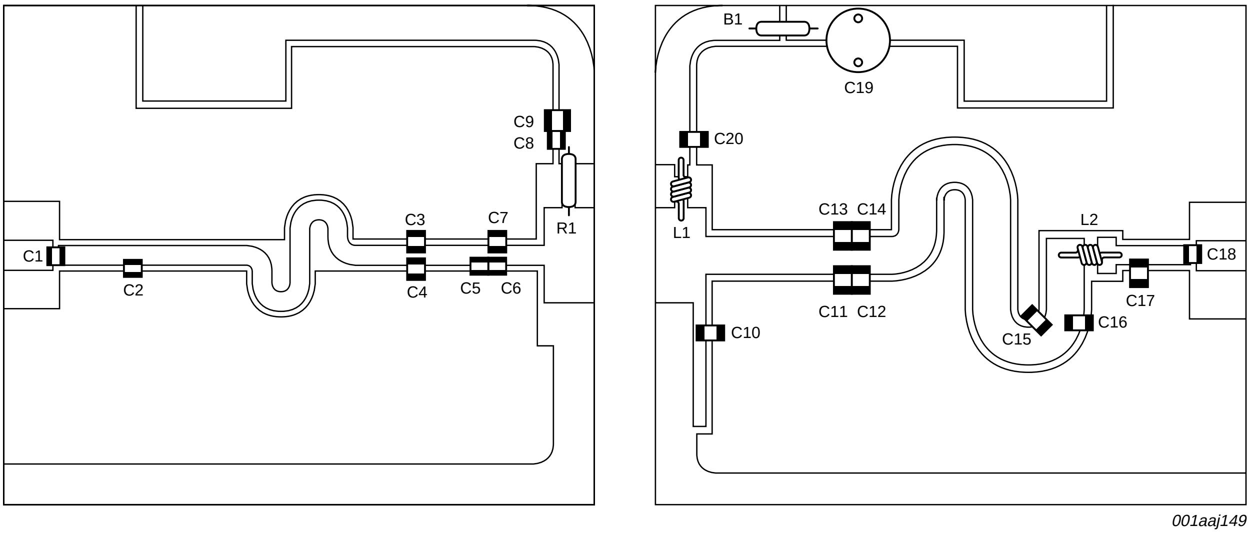
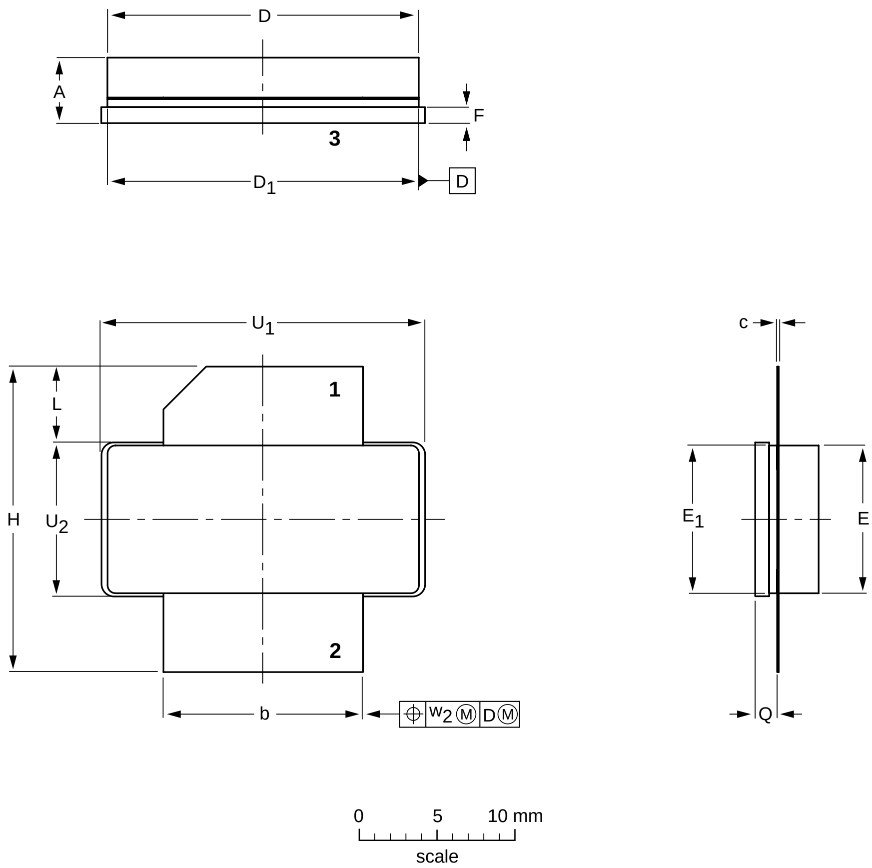


Fig 10. Component layout for class-AB production test circuit

9. Package outline

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~03-01-10~~ 07-05-09

Fig 11. Package outline SOT502B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mount Device
TTF	Time To Failure
VHF	Very High Frequency
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF573S_1	20081208	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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