

# HD74LVC373A

## Octal D-type Transparent Latches with 3-state Outputs

REJ03D0354-0400Z  
 (Previous ADE-205-112B (Z))  
 Rev.4.00  
 Jul. 27, 2004

### Description

The HD74LVC373A has eight D type latches with three state outputs in a 20 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs  $V_{IH}(\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- All outputs  $V_{OUT}(\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V or output off state})$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C})$
- High output current  $\pm 24\text{ mA} (@V_{CC} = 3.0\text{ V to }5.5\text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC373AFP	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74LVC373ATELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Function Table

#### Inputs

$\bar{G}$	LE	D	Output Q
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	$Q_0$

H: High level

L: Low level

X: Immaterial

Z: High impedance

$Q_0$ : Level of Q before the indicated steady input conditions were established.



**Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	1.5 to 5.5	V	Data hold
		2.0 to 5.5		At operation
Input / output voltage	V <sub>I</sub>	0 to 5.5	V	$\bar{G}$ , LE, D
	V <sub>O</sub>	0 to V <sub>CC</sub>	V	Output "H" or "L"
		0 to 5.5		Output "Z" or V <sub>CC</sub> :OFF
Operating temperature	T <sub>a</sub>	-40 to 85	°C	
Output current	I <sub>OH</sub>	-12	mA	V <sub>CC</sub> = 2.7 V
		-24 <sup>*2</sup>		V <sub>CC</sub> = 3.0 V to 5.5 V
	I <sub>OL</sub>	12	mA	V <sub>CC</sub> = 2.7 V
		24 <sup>*2</sup>		V <sub>CC</sub> = 3.0 V to 5.5 V
Input rise / fall time <sup>*1</sup>	t <sub>r</sub> , t <sub>f</sub>	10	ns/V	

- Notes: 1. This item guarantees maximum limit when one input switches.  
 Waveform: Refer to test circuit of switching characteristics.  
 2. Duty cycle ≤ 50%

**Electrical Characteristics**

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—		
	V <sub>IL</sub>	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V <sub>CC</sub> ×0.3		
Output voltage	V <sub>OH</sub>	2.7 to 5.5	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.7	2.2	—		I <sub>OH</sub> = -12 mA
		3.0	2.4	—		I <sub>OH</sub> = -24 mA
		3.0	2.2	—		
		4.5	3.8	—		
	V <sub>OL</sub>	2.7 to 5.5	—	0.2	V	I <sub>OL</sub> = 100 μA
		2.7	—	0.4		I <sub>OL</sub> = 12 mA
		3.0	—	0.55		I <sub>OL</sub> = 24 mA
		4.5	—	0.55		
Input current	I <sub>IN</sub>	0 to 5.5	—	±5.0	μA	V <sub>IN</sub> = 5.5 V or GND
Off state output current	I <sub>OZ</sub>	2.7 to 5.5	—	±5.0	μA	V <sub>IN</sub> = V <sub>CC</sub> , GND V <sub>OUT</sub> = 5.5 V or GND
Output leak current	I <sub>OFF</sub>	0	—	20	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V
Quiescent supply current	I <sub>CC</sub>	2.7 to 3.6	—	±10	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 3.6 to 5.5 V
		2.7 to 5.5	—	10		V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	500	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6)V, other inputs at V <sub>CC</sub> or GND

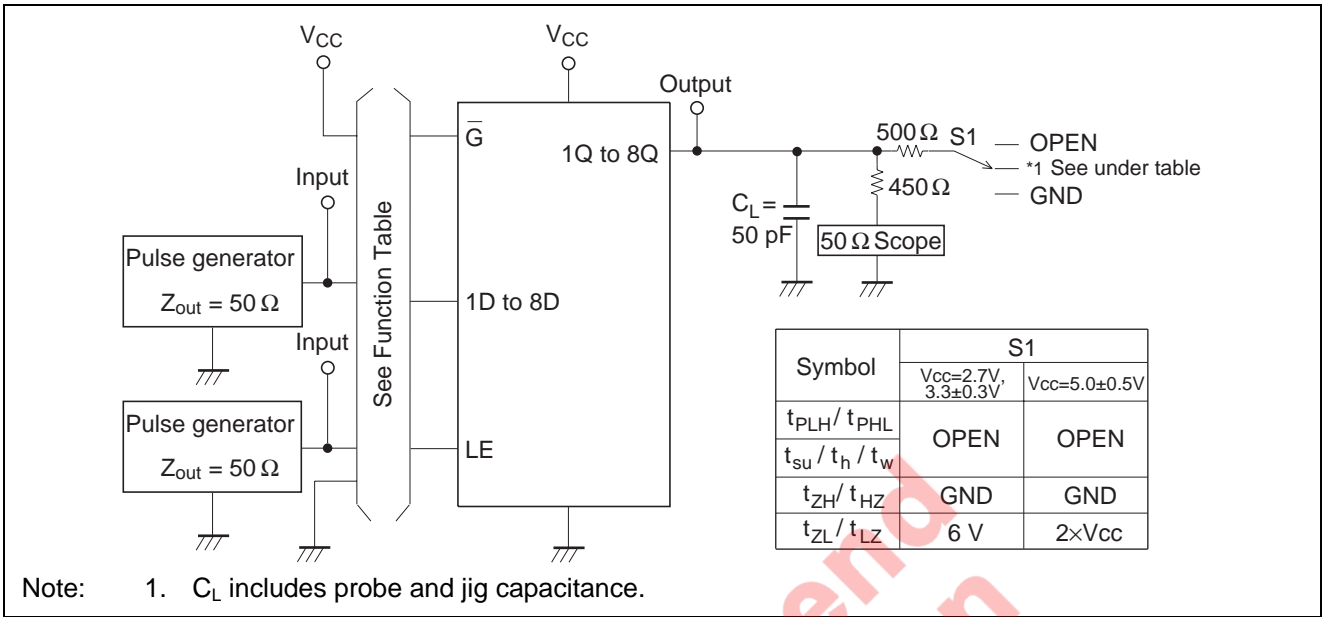
Switching Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t <sub>PLH</sub>	2.7	—	—	9.0	ns	D	Q
		3.3±0.3	1.5	—	8.0			
		5.0±0.5	—	—	6.5			
	t <sub>PHL</sub>	2.7	—	—	9.5	ns	LE	Q
		3.3±0.3	2.0	—	8.5			
		5.0±0.5	—	—	7.0			
Output enable time	t <sub>ZH</sub>	2.7	—	—	9.5	ns	$\bar{G}$	Q
		3.3±0.3	1.5	—	8.5			
		5.0±0.5	—	—	7.0			
Output disable time	t <sub>LZ</sub>	2.7	—	—	8.5	ns	$\bar{G}$	Q
		3.3±0.3	1.5	—	7.5			
		5.0±0.5	—	—	6.5			
Setup time	t <sub>su</sub>	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t <sub>h</sub>	2.7	1.5	—	—	ns		
		3.3±0.3	1.5	—	—			
		5.0±0.5	1.5	—	—			
Pulse width	t <sub>w</sub>	2.7	3.3	—	—	ns		
		3.3±0.3	3.3	—	—			
		5.0±0.5	3.3	—	—			
Between output pins skew <sup>*1</sup>	t <sub>OSLH</sub>	2.7	—	—	—	ns		
	t <sub>OShL</sub>	3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C <sub>IN</sub>	2.7	—	3.0	—	pF		
Output capacitance	C <sub>O</sub>	2.7	—	15.0	—	pF		

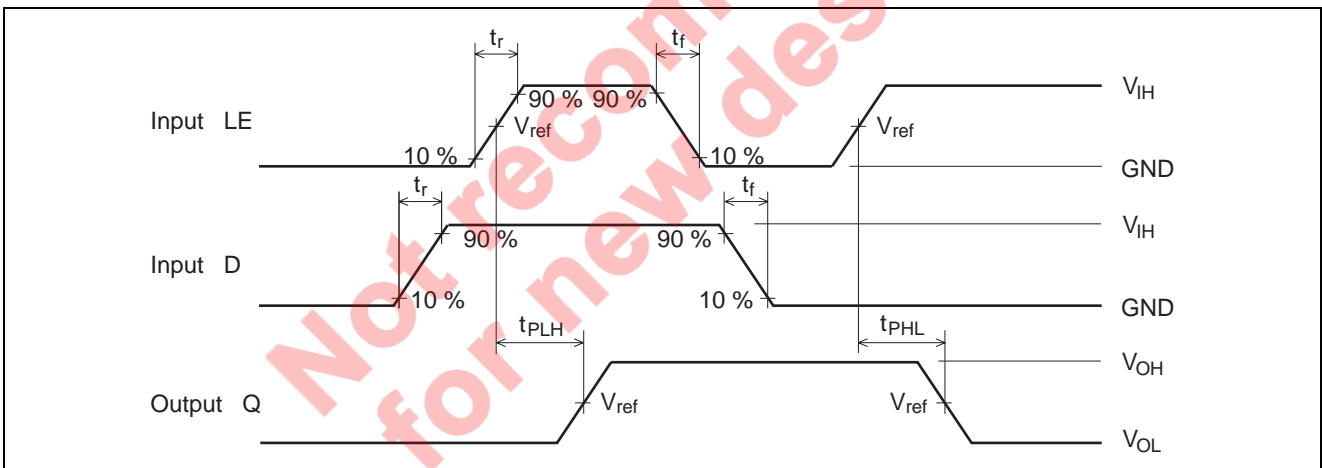
Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OShL} = |t_{PHLm} - t_{PHLn}|$$

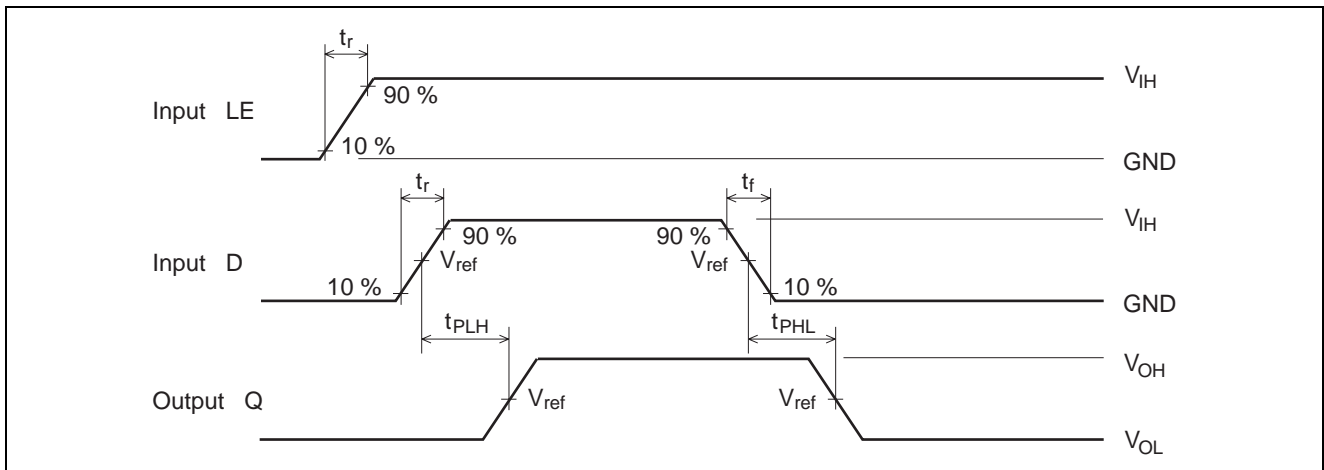
Test Circuit



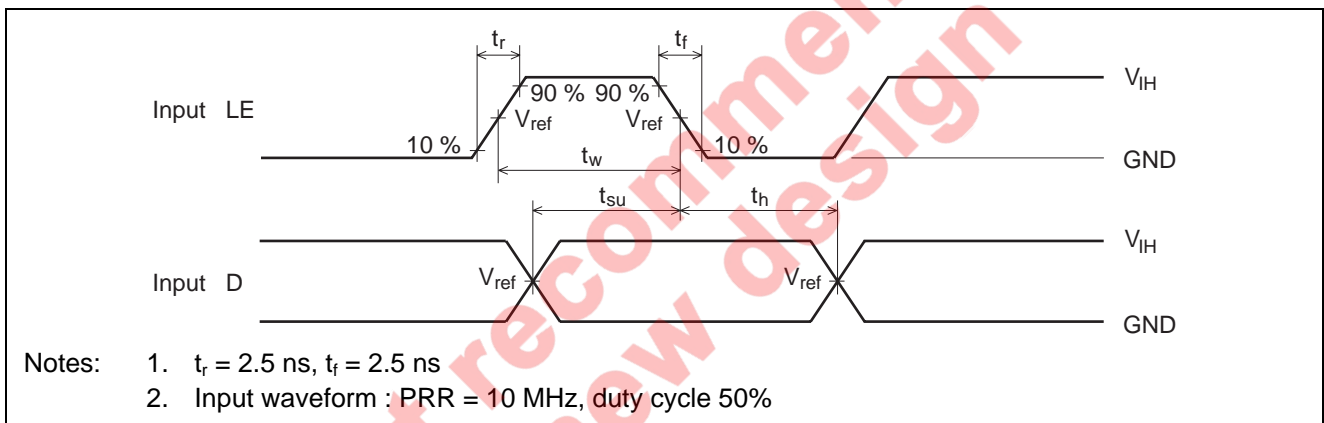
Waveforms – 1



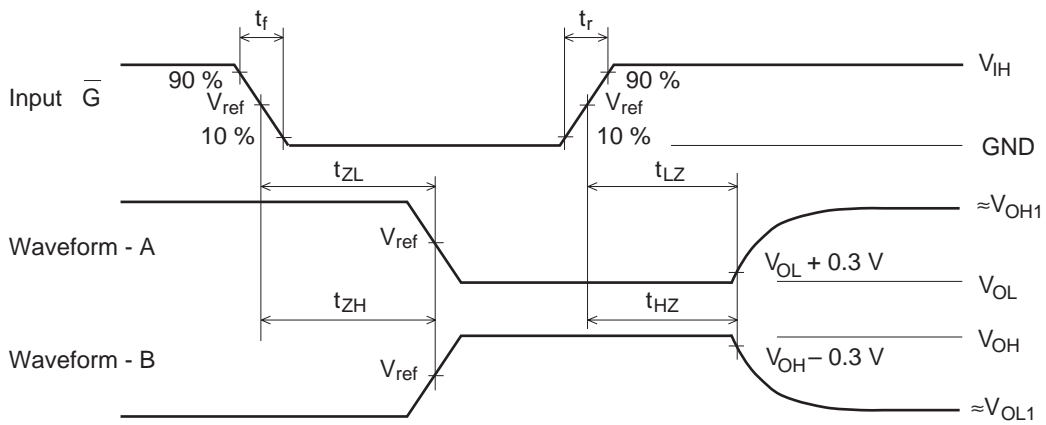
Waveforms – 2



Waveforms – 3



Waveforms – 4

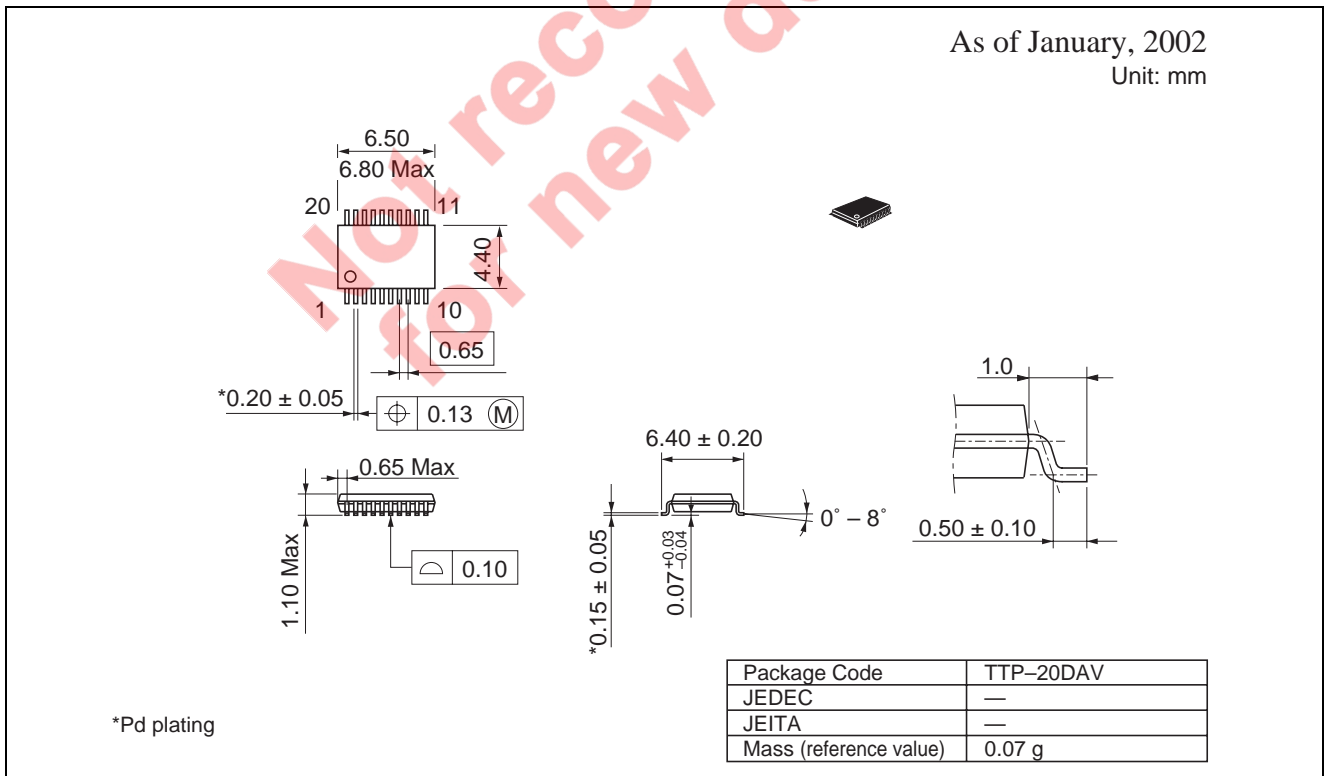
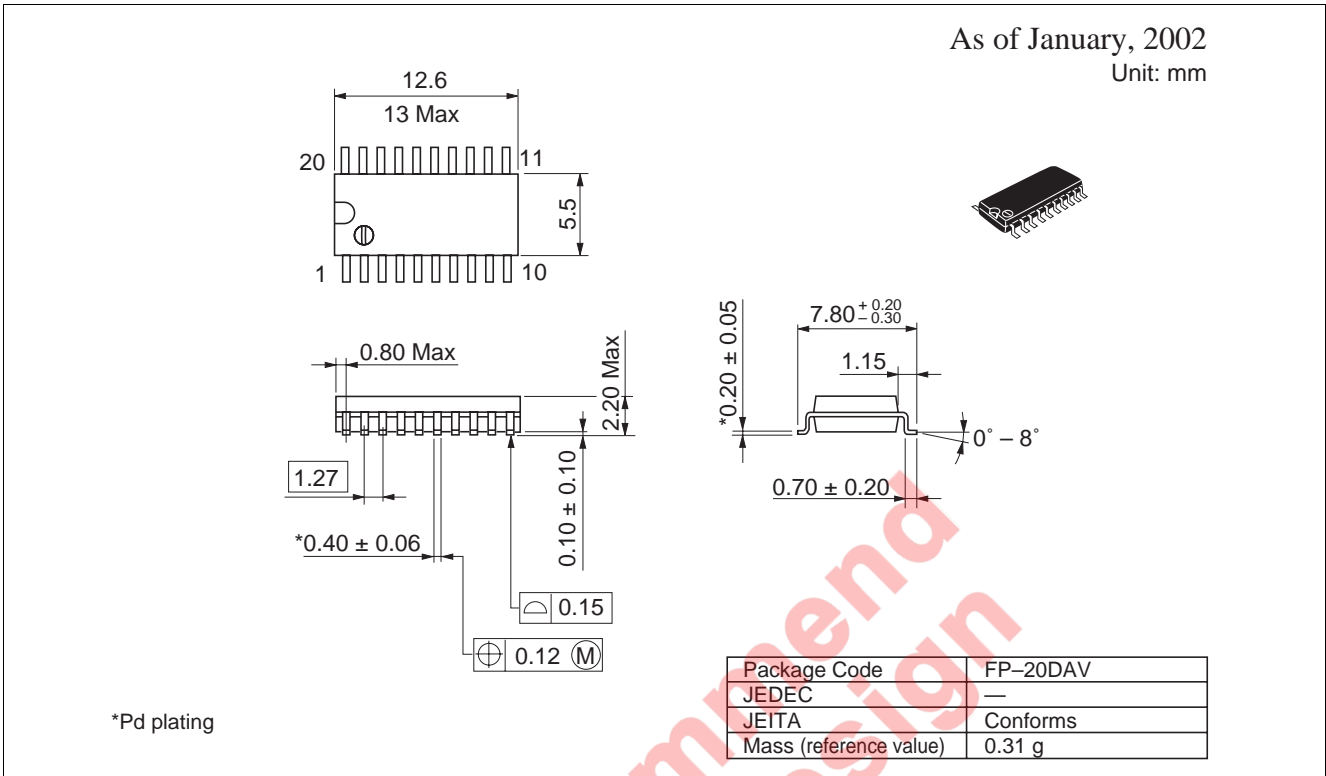


TEST	$V_{CC}=2.7V, 3.3\pm 0.3V$	$V_{CC}=5.0\pm 0.5V$
$V_{IH}$	2.7 V	$V_{CC}$
$V_{ref}$	1.5 V	50% $V_{CC}$
$V_{OH1}$	3 V	$V_{CC}$
$V_{OL1}$	GND	GND

- Notes:
1.  $t_r = 2.5$  ns,  $t_f = 2.5$  ns
  2. Input waveform : PRR = 10 MHz, duty cycle 50%
  3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
  4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.

Not recommended for new designs

Package Dimensions





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