SA50CE

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FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/HIGHSIDE DRIVE CIRCUITRY
- SINGLE ENDED SUPPLY OPERATION
- WIDE SUPPLY RANGE: UP TO 80V
- 5A CONTINUOUS OUTPUT
- HERMETIC SEALED PACKAGE
- HIGH EFFICIENCY: 95% TYPICAL
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY
- INTERNAL PWM GENERATION

8-PIN TO-3
PACKAGE STYLE CE

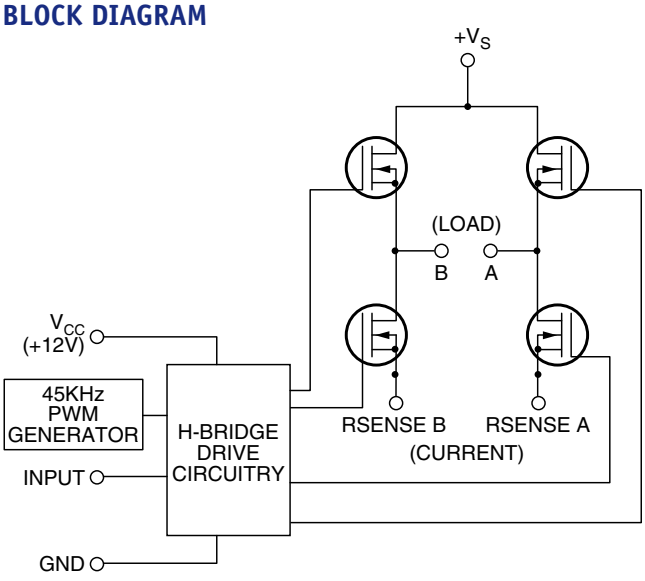
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

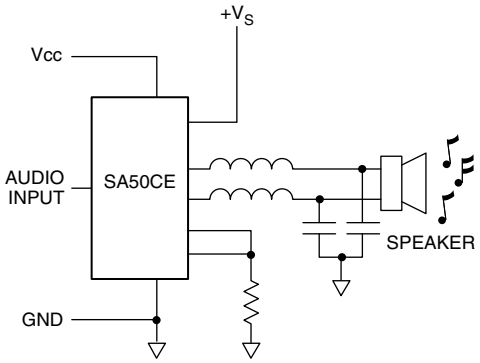
DESCRIPTION

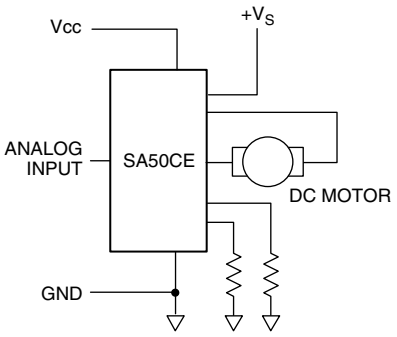
The SA50CE is a pulse width modulation amplifier that can continuously supply 5A to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and high side switches are internal to the hybrid. The PWM circuitry is internal as well, leaving the user to only provide an analog signal for the motor speed and direction, or audio signal for switchmode audio amplification. The SA50CE is packaged in a space efficient isolated 8-pin TO-3 that can be directly connected to a heatsink.

BLOCK DIAGRAM

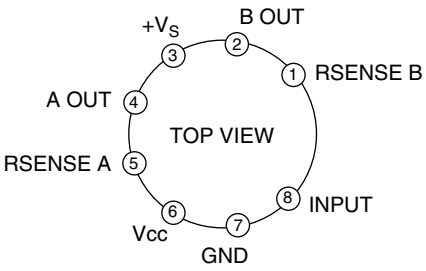


TYPICAL APPLICATIONS





EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	80V[5]
OUTPUT CURRENT, peak	7A
LOGIC SUPPLY VOLTAGE, Vcc	16V
POWER DISSIPATION, internal	72W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–65 to +125°C
INPUT VOLTAGE	+1V to Vcc – 1.5 Vdc

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
ANALOG INPUT VOLTAGES	Vcc = 9.5V to 15V				
MOTOR A, B = 50% Duty Cycle			$V_{CC}/2$		V
MOTOR A = 100% Duty Cycle High[6]			$2V_{CC}/3$		V
MOTOR B = 100% Duty Cycle High[6]			$V_{CC}/3$		V
OUTPUT					
Vds (ON) VOLTAGE, each MOSFET	Ids = 5A		1.0	1.3	Vdc
TOTAL Ron, both MOSFETs			0.4		Ω
EFFICIENCY, 5A OUTPUT	$+V_S$ = 80V		95		%
SWITCHING FREQUENCY		40	45	50	kHz
CURRENT, continuous		5			A
CURRENT, peak	t = 100 m-sec	7			A
SWITCHING CHARACTERISTICS[4]	$+V_S$ = 28V, Vcc = 12V, Ic =2A				
RISE TIME			36	54	ns
FALL TIME			170	250	ns
DEAD TIME			100		ns
POWER SUPPLY					
$+V_S$ VOLTAGE[5]	$+V_S$ I = Load I			80	V
Vcc VOLTAGE		9.5	12	15	V
Vcc CURRENT	Vcc = 12Vdc		20	30	mA
THERMAL[3]					
RESISTANCE, junction to case	Full temp range, for each transistor		2.0		°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–40		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 36W. This is an output FET rating only; normal operation at worst case conditions and maximum duty cycle only causes 19 watts internal heat generation in each active output FET. Use 40 watts maximum to size heatsink.
2. Unless otherwise noted: T_C = 25°C, Vcc = 12Vdc.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. Derate linearly to 70V at – 40°C from T_C = +25°C.

CAUTION

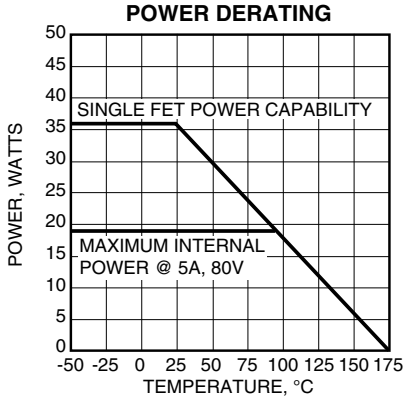
The SA50CE is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

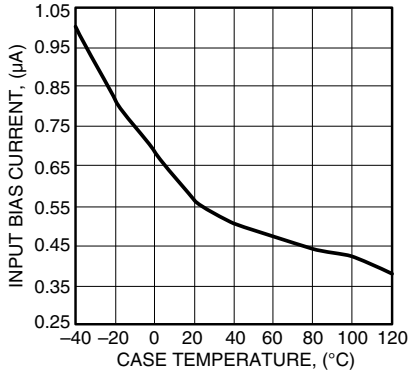
WARNING—AMPLIFIER PROTECTION

The SA50CE contains an internal logic chip that turns on and turns off output MOSFET drivers at a certain sequence. Noises or oscillation caused by external wiring inductance, lack of proper power supply bypass capacitors, ground, supply and local internal loops, may be fed back to this logic chip and cause it to turn on one or more MOSFET drivers at the wrong time, thus destroying the SA50CE. A well laid out PC board with low impedance copper ground plane and excellent bypassing is necessary for the SA50CE to function properly. A low ESR high frequency bypass capacitor, such as a 0.1 µf 100V X7R ceramic, or better, should be mounted as close to the Vs and ground pins as possible to avoid radiation of high frequency transients on the power supply wiring. The Apex EK-SA50CE evaluation board is recommended for fast and easy breadboarding of circuits using the SA50CE.

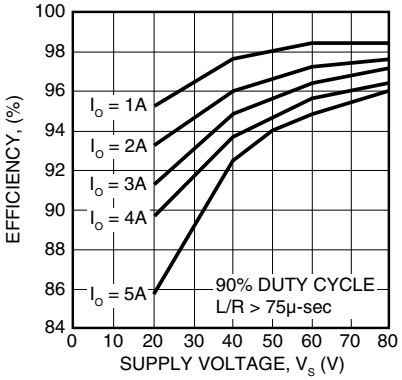
POWER DERATING



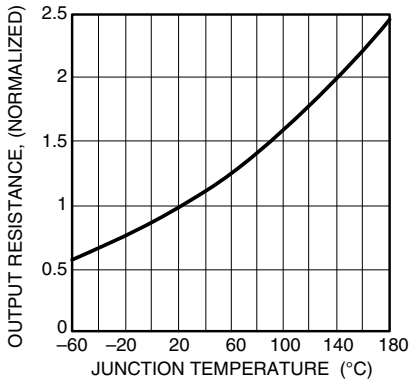
INPUT CURRENT VS TEMP



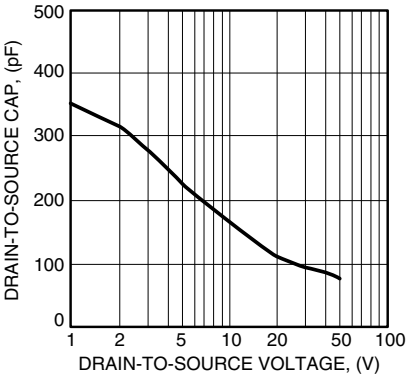
EFFICIENCY vs. POWER SUPPLY VOLTAGE



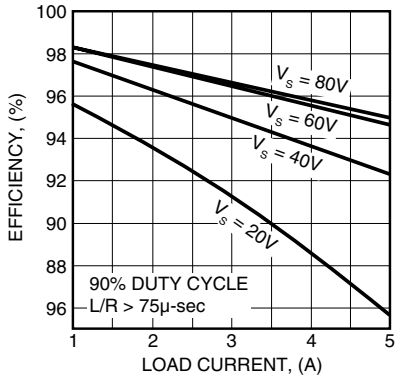
OUTPUT RESISTANCE DRIFT



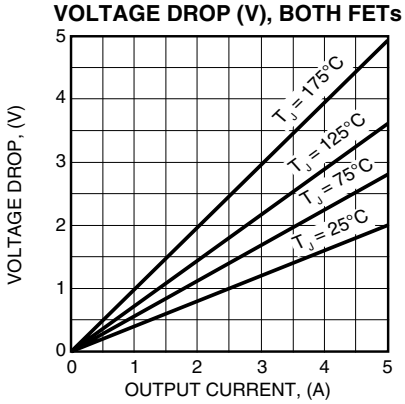
H-BRIDGE FET CAPACITANCE



EFFICIENCY vs. LOAD CURRENT



VOLTAGE DROP (V), BOTH FETs



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

PIN DESCRIPTION

V_{CC} - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. Proper by-passing to GND with sufficient capacitance to suppress any voltage transients, and to ensure removing any drooping during switching, should be done as close to the pins on the hybrid as possible.

A OUT - is the output pin for one half of the bridge. Increasing the input voltage causes increasing duty cycle at this output.

B OUT - is the output pin for the other half of the bridge. Decreasing the input voltage causes increasing duty cycles at this point.

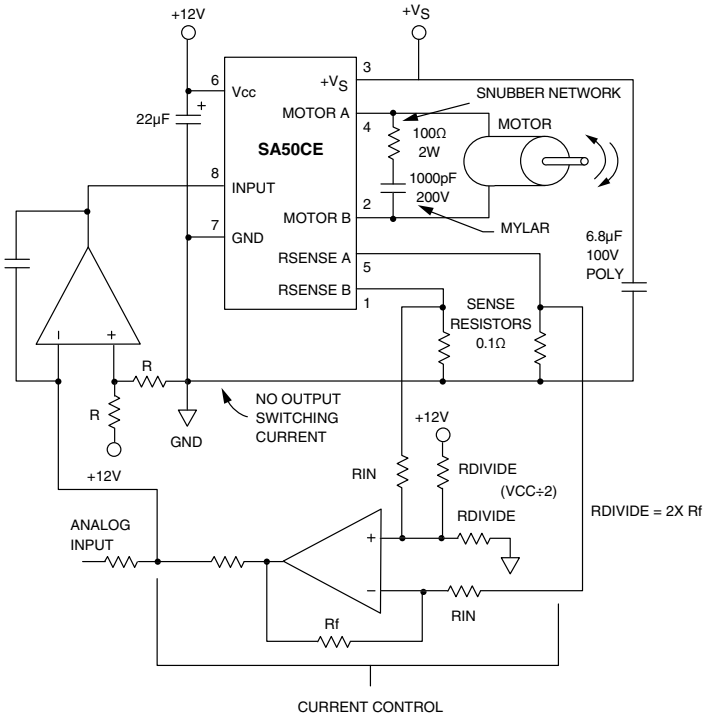
RSENSE A - This is the connection for the bottom of the A half bridge. This can have a sense resistor connected to the V_S return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

GND - is the return connection for the input logic and V_{CC}.

RSENSE B - This is the connection for the bottom of the B half bridge. This can have a sense resistor connection to the V_S return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

INPUT - is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than $V_{CC}/2$ will produce greater than 50% duty cycle pulses out of A OUT. A voltage lower than $V_{CC}/2$ will produce greater than 50% duty cycle pulses out of B OUT.

TYPICAL SYSTEM OPERATION



This is a diagram of a typical application of the SA50CE. The design Vcc voltage is +12 volts. V_{CC} is internally bypassed with a good low ESR ceramic capacitor. A higher ESR bulk capacitor, such as a tantalum electrolytic, may be used externally in parallel. The analog input can be an analog speed control voltage from a potentiometer, other analog circuitry or by microprocessor and a D/A converter. This analog input gets pulled by the current control circuitry in the proper direction to reduce the current flow in the bridge if it gets too high. The gain of the current control amplifier will have to be set to obtain the proper amount of current limiting required by the system.

Current sensing is done in this case by a 0.1Ω sense resistor to sense the current from both legs of the bridge separately. It is important to make the high current traces as big as possible to keep inductance down. The storage capacitor connected to the V_S and the hybrid GND should be large enough to provide the high energy pulse without the voltage sagging too far. A low ESR capacitor will be required. Mount capacitor as close to the hybrid as possible. The connection between GND and the V_S return should not be carrying any motor current. The sense resistor signal is common mode filtered as necessary to feed the limiting circuitry. This application will allow full four quadrant torque control for a closed loop servo system.

A snubber network is usually required, due to the inductance in the power loop. It is important to design the snubber network to suppress any positive spikes above $+V_S$ and negative spikes below –2V with respect to pin 7 (GND).

