CybraTech

SOC-3000/i

Scale-On-Chip™ ASIC

Technical Specification Rev.B1

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GENERAL

Features

Scale-On-Chip System

- Single-Chip Scale electronics
- Full OIML R-76 compliance
  - *SOC-3000* - 3000 d
  - *SOC-3000i* - 6000 d
- Up to eight load cells
- 6-wire load cell connection (including Sense inputs)

Peripherals

- Supports LCD and LED displays:
  - LCD: Up to 20 digits (160 segments, 4×40)
  - LED: Up to 24 digits
- Keyboard: Up to 64 keys
- Serial communication: RS-232/485
- I/O (set-points): Up to 40 lines
- Temperature sensor input

CPU

- Enhanced 80C51TBO
- 4 cycles/instruction
- 120KByte, field-programmable Flash program and data memory
- 4KByte RAM
- 4KByte non-volatile Data Flash

Analog–to–Digital Converter

- Resolution-20 bits
- Sample rate-5, 10, 20 samples per second
- Programmable gain-0.5, 0.75, 1, 1.5, 2

Power

- 5/3.3V operation, 15mA
- Battery operation support
- Power failure detector

Applications

- Price computing scales
- Weighing indicators
- Counting scales
- Checkout scales

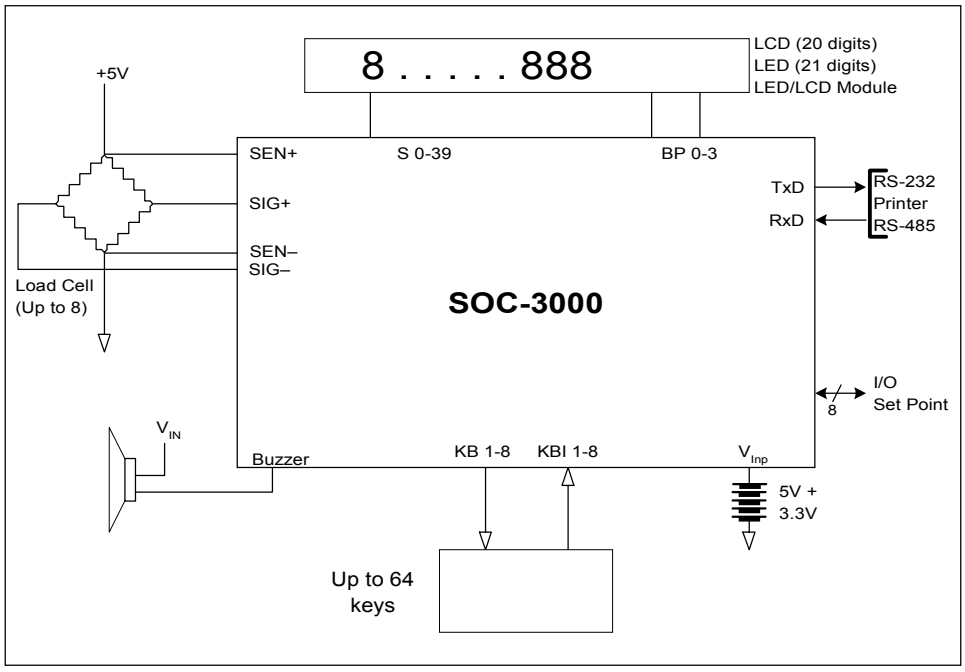

FIGURE 1: SOC-3000 TYPICAL APPLICATION

General Description

The SOC-3000 ASIC is an 84-pin, single-chip scale intended to replace present-day, multiple-component weighing scale electronic circuitry designs. It includes the pre-amplifier, ADC converter, display drivers, keyboard controller, serial communication, embedded CPU and field-programmable program and data memory.

As a "stand-alone" unit it incorporates all scale hardware functions and represents a true breakthrough in scale manufacturing. It eliminates the risks, costs and inventory needs associated with discrete components.

The SOC-3000 comes with a comprehensive software library, which implements hardware drivers, such as the display and keyboard, as well as most of the standard weighing functions. A complete development environment is available, enabling youto tailor and customize the application according to specific needs.

The general SOC-3000 block diagram is presented in Figure 2.

Advantages

- Generic OIML R-76 approval
- Minimize hardware and software development
- Significantly cuts time-to-market
- Reduces inventory needs

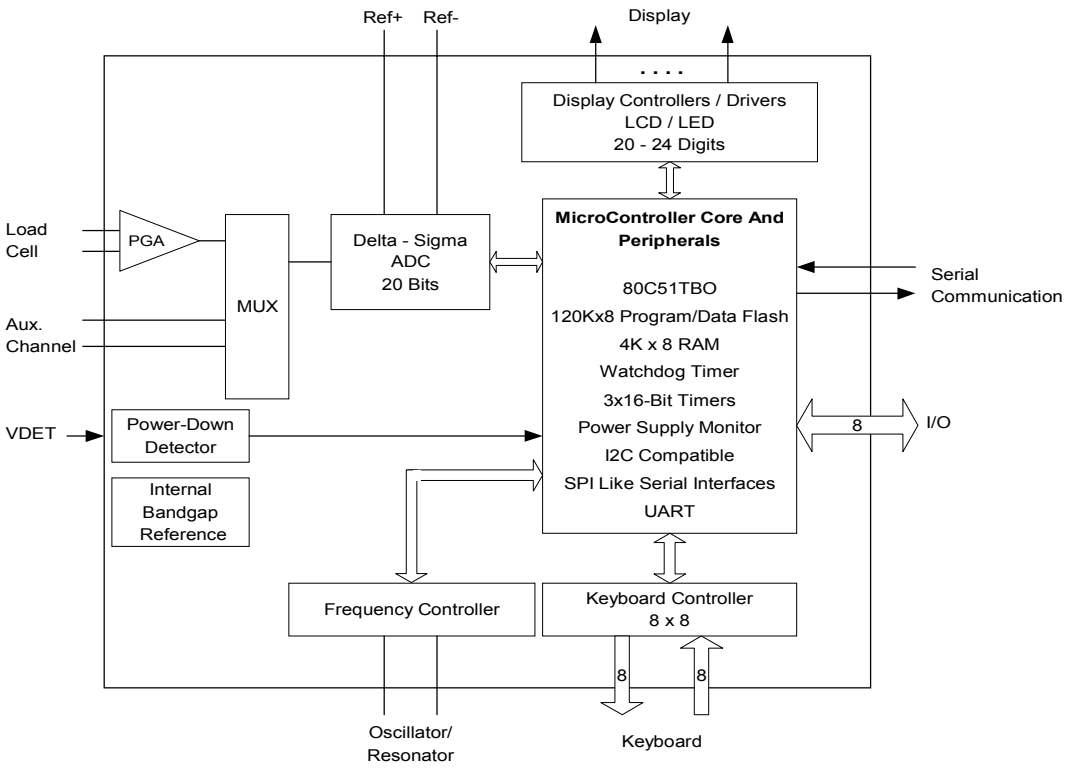

FIGURE 2: SOC-3000 BLOCK DIAGRAM

SPECIFICATIONS

Analog-to-Digital Converter (ADC)

ADC Converter Main Channel – Wheatstone Bridge (Load Cell)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Differential Input Voltage	0		+10	mV	
Programmable Gain	0.5		2		Up to 8 load cell
Offset Drift vs. Temperature			20	ppm/ºC	
Gain Drift vs. Temperature			4	ppm/ºC	
Integral Non-linearity			0.004	%	Of full scale
Common-Mode Rejection (CMR)	120			dB	
Power Supply Rejection	120			dB	
Output Noise		200		nVp-t-p	±1 count
Resolution			20	bit	
Sample Rate	5	10	20	Samples/s	

ADC Converter Auxiliary Channel

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Analog Input Voltage	0		0.8	V	
Offset Drift			20	ppm/ºC	
Gain Drift			4	ppm/ºC	
Resolution			20	Bit	
Sample Rate	5	10	20	Samples/s	

Reference Inputs

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Reference Input			5	V	Ratiometric

Digital Input

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
V_{IH} (Input High Voltage)	2		5	V	TTL Level excluding XTAL
V_{IL} (Input Low Voltage)	0.0		0.8	V	TTL Level excluding XTAL
XTAL Input V_{IH} (Input High Voltage) V_{IL} (Input Low Voltage)	 2.5		 0.4	 V V	 V_{DD} = 3.3V V_{DD} = 3.3V

Digital Output

For LCD Display mode:

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
V_{OH} (Output High Voltage)			5	V	LCD Output set by user by external resistors
V_{OL} (Output Low Voltage)	0.0		V_{LCD}	V	LCD Output set by user by external resistors

For I/O mode:

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
V_{OH} (Output High Voltage)			3.3	V	
V_{OL} (Output Low Voltage)	0.0		0.8	V	

Flash Memory

PARAMETER	MIN	TYP	MAX	UNIT
Endurance	10,000	100,000		Cycles
Data Retention	100			Years
Erase Full Memory Single Block (4kByte)			 100 25	 ms ms
Program Byte			20	us

CPU

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Enhanced 80C51TBO					
Reset Signal Threshold			3.98	V	
Start-Up Time					
• From Power On		500		ms	
• From Idle Mode		1		ms	
• From Power Down		1		ms	Oscillator power-down not through OSCEN bit.
		500		ms	Oscillator power-down through OSCEN bit.
From Watchdog Reset		1		ms	

Frequency Source Input

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Frequency Level			16	MHz	Crystal oscillator or resonator

Power Supply and Monitor

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Input Voltage Monitor	4.50		4.75	V	
Power Fail Input Monitor Level			2.21	V	Set by external resistors
Analog Voltage Input (AV_{CC})	4.75	5.00	5.25	V	
Digital Voltage Input (V_{CC})	3.00	3.30	3.60	V	
Power Supply Current (I_{IN})					5V and 3.3V .
CPU Freq. = 16 MHz		21		mA	Without connected I/O ports
CPU Freq. = 8 MHz		15		mA	All controllers operating.
CPU Freq. = 4 MHz		12		mA	Depends on the software
CPU Freq. = 2 MHz		11		mA	program and the Flash memory
CPU Freq. = 1 MHz		10		mA	utilization.
CPU Freq. = 0.5 MHz		10		mA	

Environmental Conditions

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Temperature	-10	20	40	ºC	Full performance
	-20	20	70	ºC	Operation
Humidity	0		95	%	Non-condensing

Absolute Maximum Rating*

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
AV_{CC}			6	V	Analog power
V_{DD}			4	V	Digital power
V_{CC}			6	V	Power
Input Signal Voltage			3.6	V	
Operating Temperature	–20		+70	ºC	
Storage Temperature	–20		+85	ºC	
Lead Temperature					
Manual soldering			300	ºC	Soldering for 10 seconds
Reflow soldering			225	ºC	60 seconds

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. The functional operation of the device under these or any other conditions outside of the range listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.

Outline Dimensions

The outline dimensions of the SOC-3000 PLCC-84 case is shown in Figure 3.

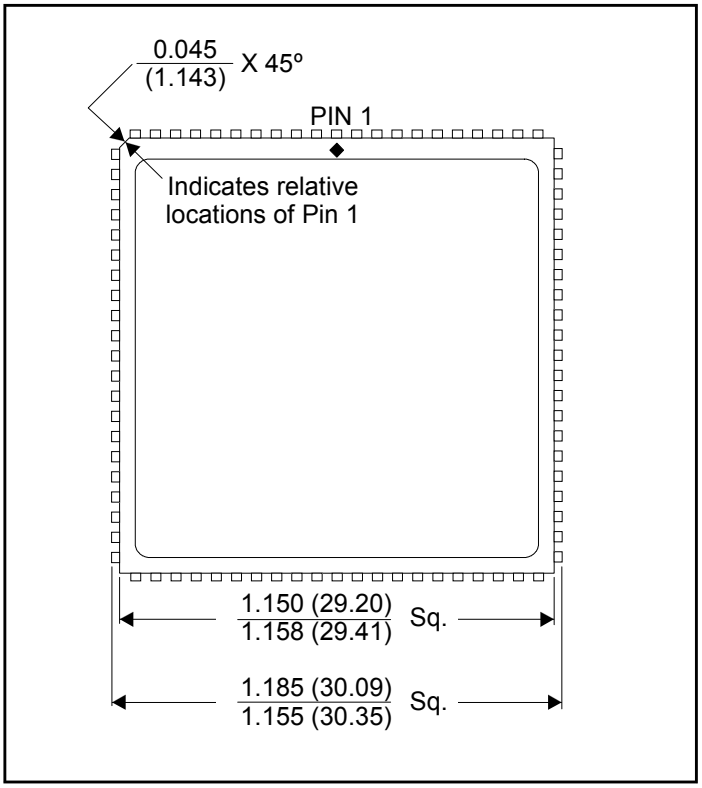

FIGURE 3: MECHANICAL OUTLINE DRAWING

Scale Main Board Layout And Assembly Process Parameters For SOC-3000

1. Pad definition will be according to Figure 4.
2. Solder mask opening should be 3mil (total 6 mil).
3. Board finish may be HAL (hot air leveling), immersion gold over nickel or immersion.
4. Verify that the SOC-3000 components are packaged in hermetically sealed package. If the packaging is damaged or has been opened, perform the following drying procedure to assure that SOC-3000 components are completely dry:
   - **Components drying procedure:**
     Place the SOC-3000 components in their tray and put them into a baking oven to dry at a temperature of 105ºC for a minimum of 6 hours.
5. Reflow temperature profile should be set according to the paste parameters.
6. Maximum reflow temperature should be **less than** 225 ºC.
7. Recommended paste: Koki, AIM, Multicore
   a. Type 3
   b. NC
   c. RMA or equivalent

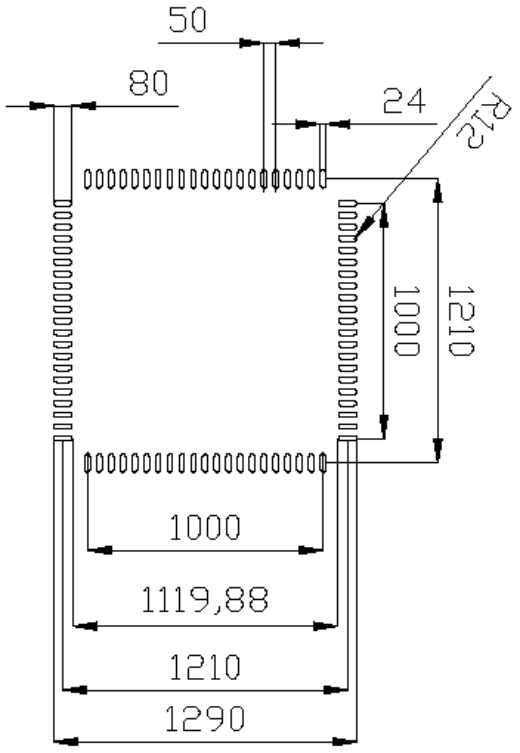

FIGURE 4: PCB BOARD LAYOUT

(Dimensions are in milli inches (mil))

PIN CONFIGURATION

The SOC-3000 pin configuration for LCD and LED displays is presented in Table 1 and Table 2, respectively, followed by a glossary of terms used in the tables.

General notes on SOC-3000 pin configuration are presented in Table 3, page 15.

The physical pin arrangement is shown in Figure 5, page 15.

The physical pin configuration for an LCD display is shown in Figure 6, page 16, followed by a quick reference table in Table 4, page 18.

The physical pin configuration for a LED display is shown in Figure 7, page 17, followed by a quick reference table in Table 5, page 19.

TABLE 1: SOC-3000 PIN CONFIGURATION FOR LCD DISPLAY

PIN	NAME	DESCRIPTION	2nd FUNCTION	DESCRIPTION	PULL-UP RESISTOR
1	KIN4	Keyboard Controller Input See "Keyboard Controller", page 31	I.O 15.3	I/O, See "I/O Operation", page 65	50k
2	KIN3		I.O 15.4		
3	KIN2		I.O 15.5		
4	KIN1		I.O 15.6		
5	KIN0		I.O 15.7		
6	VDD	Digital Power Supply			
7	BUZZER / P1.7 (CPU)	Buzzer			25k
8	P1.5 (CPU)	CPU I/O Port See Note 11			10k
9	P1.4 (CPU)				
10	XTAL OUT	Frequency Clock Source			
11	XTAL IN				
12	TXD	Serial Communication Tx			
13	RXD	Serial Communication Rx			100k
14	PWR_OFF / P3.4/Timer 0	Power Off Control	P3.4 (CPU)	CPU I/O Ports, or: P3.4 – Timer 0	50k
15	MAIN_DET / P3.5 /Timer1	Battery/AC power supply detector input	P3.5 (CPU)		
16	EL / P1.6 (CPU)	Electro-luminescent light control See Note 11	P1.6 (CPU)		
17	VLCD	LCD Display voltage			
18	BP1	LCD Display Multiplexer Backplanes, See "LCD Controller/Driver", page 35	OUT 4.0	I/O See "I/O Operation", page 69	
19	BP2		OUT 4.1		
20	BP3		OUT 4.2		
21	BP4		OUT 4.3		

PIN	NAME	DESCRIPTION	2nd FUNCTION	DESCRIPTION	PULL-UP RESISTOR
22	S1	LCD Display Segment See “LCD Controller/Driver”, page 35	OUT 5.0	I/O See “I/O Operation”, page 69	
23	S2		OUT 5.1		
24	S3		OUT 5.2		
25	S4		OUT 6.0		
26	S5		OUT 6.1		
27	S6		OUT 6.2		
28	S7		OUT 6.3		
29	S8		OUT 7.0		
30	S9		OUT 7.1		
31	S10		OUT 7.2		
32	S11		OUT 7.3		
33	S12		OUT 8.0		
34	S13		OUT 8.1		
35	S14		OUT 8.2		
36	S15		OUT 8.3		
37	S16		OUT 9.0		
38	S17		OUT 9.1		
39	S18		OUT 9.2		
40	S19				
41	S20				
42	S21				
43	S22				
44	S23				
45	S24				
46	S25				
47	S26				
48	S27		OUT 10.0		
49	S28		OUT 11.0		
50	S29		OUT 11.1		
51	S30		OUT 11.2		
52	S31		OUT 11.3		
53	S32		OUT 12.0		
54	S33		OUT 12.1		
55	S34		OUT 12.2		
56	S35		OUT 12.3		
57	S36		OUT 12.4		
58	S37		OUT 13.0		

PIN	NAME	DESCRIPTION	2nd FUNCTION	DESCRIPTION	PULL-UP RESISTOR
59	S38		OUT 13.1		
60	S39		OUT 13.2		
61	S40		OUT 13.3		
62	VCC	Power Supply			
63	RESET	Reset			50k
64	GND	Digital Ground			
65	VDET/ INT0~	Power voltage detector input / Interrupt 0 Input			
66	SIG2+	2nd AD channel input signal +			
67	SIG2–	2nd AD channel input signal –			
68	AGND	Analog Ground			
69	SEN–	Load cell sense input –			
70	SIG1–	Load cell signal input –			
71	SIG1+	Load cell signal input +			
72	SEN+	Load cell sense input +			
73	AVCC	Analog power supply			
74	KOUT7	Keyboard Controller Inputs See “Keyboard Controller”, page 31	I.O 14.0	I/O See “I/O Operation”, page 69	50k
75	KOUT6		I.O 14.1		
76	KOUT5		I.O 14.2		
77	KOUT4		I.O 14.3		
78	KOUT3		I.O 14.4		
79	KOUT2		I.O 14.5		
80	KOUT1		I.O 14.6		
81	KOUT0		I.O 14.7		
82	KIN7	Keyboard Controller Inputs See “Keyboard Controller”, page 31	I.O 15.0		
83	KIN6		I.O 15.1		
84	KIN5		I.O 15.2		

TABLE 2: SOC-3000 PIN CONFIGURATION FOR LED DISPLAY

PIN	NAME	DESCRIPTION	2nd FUNCTION	DESCRIPTION	PULL-UP RESISTOR
1	KIN4	Keyboard Controller Input See "Keyboard Controller", page 31	I.O 15.3	I/O See "I/O Operation", page 69	50k
2	KIN3		I.O 15.4		
3	KIN2		I.O 15.5		
4	KIN1		I.O 15.6		
5	KIN0		I.O 15.7		
6	VDD	Digital Power Supply			
7	BUZZER / P1.7 (CPU)	Buzzer P1.7='1' – ON P1.7='0' – OFF See Note 10, 11			25k
8	P1.5 (CPU)	CPU I/O Port. See Note 11			10k
9	P1.4 (CPU)				
10	XTAL OUT	Frequency Clock Source			
11	XTAL IN				
12	TXD	Serial Communication Tx			
13	RXD	Serial Communication Rx			100k
14	PWR_OFF / P3.4 / Timer 0	Power Off Control	P3.4 (CPU)	CPU I/O port, or: P3.4 – Timer 0 P3.5 – Timer 1 See Note 11	50k
15	MAIN_DET / P3.5 / Timer 1	Battery/AC power supply detector input	P3.5 (CPU)		
16	EL	Electro-luminescent light control	P1.6 (CPU)	See Note 11	
17	NC	Not Used			
18	OUT 4.0	Outputs.	OUT 4.0	I/O See "I/O Operation", page 69	
19	OUT 4.1		OUT 4.1		
20	OUT 4.2		OUT 4.2		
21	OUT 4.3		OUT 4.3		
22	SEG A1	Display Segment Out, see "LED Parallel Display Controller Block Diagram", page 45	OUT 5.0		
23	SEG B1		OUT 5.1		
24	SEG C1		OUT 5.2		
25	SEG D1		OUT 6.0		
26	SEG E1		OUT 6.1		
27	SEG F1		OUT 6.2		
28	SEG G1		OUT 6.3		
29	SEG DP1		OUT 7.0		
30	SEG A2		OUT 7.1		
31	SEG B2		OUT 7.2		
32	SEG C2		OUT 7.3		
33	SEG D2		OUT 8.0		

PIN	NAME	DESCRIPTION	2nd FUNCTION	DESCRIPTION	PULL-UP RESISTOR
34	SEG E2	Display Segment Out, see “LED Parallel Display Controller Block Diagram”, page 45.	OUT 8.1	Output, I/O See “I/O Operation”, page 69	
35	SEG F2		OUT 8.2		
36	SEG G2		OUT 8.3		
37	SEG DP2		OUT 9.0		
38	SEG A3		OUT 9.1		
39	SEG B3		OUT 9.2		
40	SEG C3				
41	SEG D3				
42	SEG E3				
43	SEG F3				
44	SEG G3				
45	SEG DP3				
46	DIG 1	Display Digit Mux Control See “LED Parallel Display Controller”, page 45			
47	DIG 2				
48	DIG 3		OUT 10.0	I/O See “I/O Operation”, page 69	
49	DIG 4		OUT 11.0		
50	DIG 5		OUT 11.1		
51	DIG 6		OUT 11.2		
52	DIG 7		OUT 11.3		
53	OUT 12.0	Output See “I/O Operation”, page 69			
54	OUT 12.1				
55	OUT 12.2				
56	OUT 12.3				
57	OUT 12.4				
58	LED_SI_CLK	LED Serial Interface Display Module Clock, Data, Strobe and Blank See “LED Serial Interface Display Controller”, page 49.	OUT 13.0	I/O See “I/O Operation”, page 69	
59	LED_SI_Data		OUT 13.1		
60	LED_SI_ST		OUT 13.2		
61	LED_SI_BL		OUT 13.3		
62	VCC	Power Supply			
63	RESET	Reset			50k
64	GND	Digital Ground			
65	VDET/ INT0~	Power voltage detector input / Interrupt 0 Input			
66	SIG2+	2nd ADC channel input signal +			
67	SIG2–	2nd ADC channel input signal –			
68	AGND	Analog Ground			
69	SEN–	Load cell sense input –			

PIN	NAME	DESCRIPTION	2nd FUNCTION	DESCRIPTION	PULL-UP RESISTOR
70	SIG1–	Load cell signal input –			
71	SIG1+	Load cell signal input +			
72	SEN+	Load cell sense input +			
73	AVCC	Analog power supply			
74	KOUT7	Keyboard Controller Output, See "Keyboard Controller", page 31	I.O 14.0	I/O See "I/O Operation", page 69	50k
75	KOUT6		I.O 14.1		
76	KOUT5		I.O 14.2		
77	KOUT4		I.O 14.3		
78	KOUT3		I.O 14.4		
79	KOUT2		I.O 14.5		
80	KOUT1		I.O 14.6		
81	KOUT0		I.O 14.7		
82	KIN7	Keyboard Controller Input, See "Keyboard Controller", page 31	I.O 15.0		
83	KIN6		I.O 15.1		
84	KIN5		I.O 15.2		

GLOSSARY OF TERMS

TERM	DEFINITION
BP	Backplane
CLK	Clock
DIG	Digit
I.O	Input/Output
KIN	Keyboard In
KOUT	Keyboard Out
P/PWR	Power
REG	Register
RX	Receive
SEG	Segment
SI	Serial Interface
TX	Transmit

TABLE 3: NOTES ON SOC-3000 PIN CONFIGURATION

#	COMPONENT	REMARKS
1	LCD Controller/Driver	• Bit programmable
2	LED Controller	• V_{oh} @ I_o = 1.5mA • Bit programmable
3	Output Pins	CMOS–3.3V
4	Input Pins	CMOS–3.3V
5	VDET	• Less than 5V • Threshold level – 2.1V. • The input (on the analog chip) tolerates input voltage applied while the SOC-3000 is powered off.
6	VDD	3.3V ±5%
7	VCC	5V ±5%
8	AVCC	5V ±5%
9	Keyboard Controller	Bit programmable
10	Buzzer	P1.7 is used as the BUZZER control pin. During power-up the SOC-3000 asserts 3 pulses on this line.
11	Port 1.x	Manipulation of this pin should be made using BIT mapping of the port, since bits P1.0-P1.1 are allocated to the bank select register.

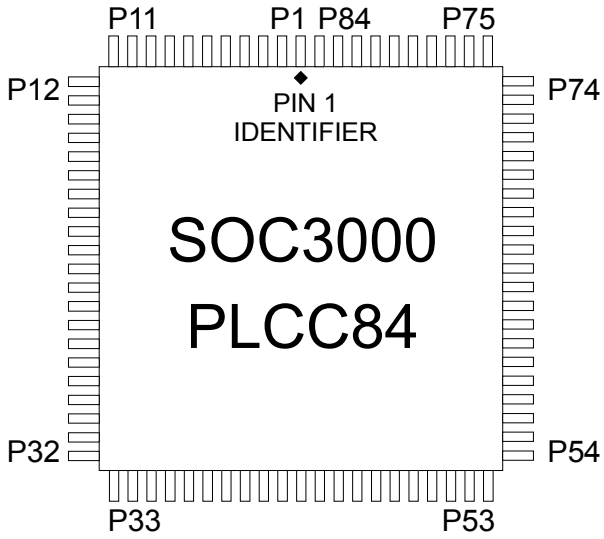

FIGURE 5: SOC-3000 PIN ARRANGEMENT

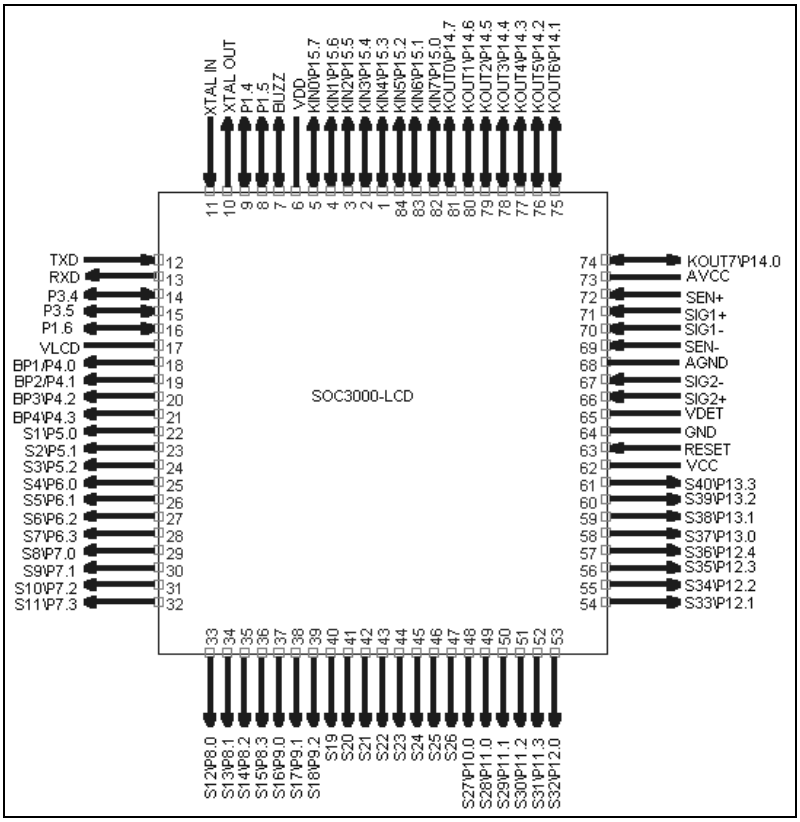

FIGURE 6: SOC-3000 LCD DISPLAY PIN CONFIGURATION

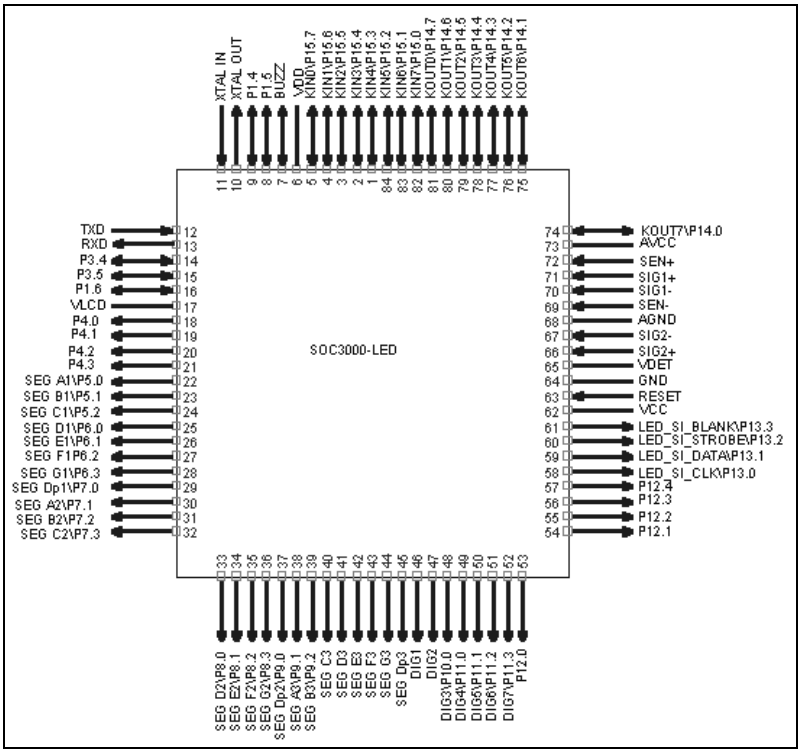

FIGURE 7: SOC-3000 LED DISPLAY PIN CONFIGURATION

TABLE 4: SOC-3000 QUICK REFERENCE PIN CONFIGURATION FOR LCD DISPLAY

PIN	NAME
1	KIN4 / I.O 15.3
2	KIN3 / I.O 15.4
3	KIN2 / I.O 15.5
4	KIN1 / I.O 15.6
5	KIN0 / I.O 15.7
6	VDD
7	BUZZER / P1.7
8	P1.5 (CPU)
9	P1.4 (CPU)
10	XTAL OUT
11	XTAL IN
12	TXD
13	RXD
14	PWR_OFF / P3.4 (CPU) / Timer 0
15	MAIN_DET / P3.5 (CPU) / Timer 1
16	EL / P1.6 (CPU)
17	VLCD
18	BP1 / OUT 4.0
19	BP2 / OUT 4.1
20	BP3 / OUT 4.2
21	BP4 / OUT 4.3

PIN	NAME
22	S1 / OUT 5.0
23	S2 / OUT 5.1
24	S3 / OUT 5.2
25	S4 / OUT 6.0
26	S5 / OUT 6.1
27	S6 / OUT 6.2
28	S7 / OUT 6.3
29	S8 / OUT 7.0
30	S9 / OUT 7.1
31	S10 / OUT 7.2
32	S11 / OUT 7.3
33	S12 / OUT 8.0
34	S13 / OUT 8.1
35	S14 / OUT 8.2
36	S15 / OUT 8.3
37	S16 / OUT 9.0
38	S17 / OUT 9.1
39	S18 / OUT 9.2
40	S19
41	S20
42	S21

PIN	NAME
43	S22
44	S23
45	S24
46	S25
47	S26
48	S27 / OUT 10.0
49	S28 / OUT 11.0
50	S29 / OUT 11.1
51	S30 / OUT 11.2
52	S31 / OUT 11.3
53	S32 / OUT 12.0
54	S33 / OUT 12.1
55	S34 / OUT 12.2
56	S35 / OUT 12.3
57	S36 / OUT 12.4
58	S37 / OUT 13.0
59	S38 / OUT 13.1
60	S39 / OUT 13.2
61	S40 / OUT 13.3
62	VCC
63	RESET

PIN	NAME
64	GND
65	VDET / INT 0~
66	SIG2+
67	SIG2–
68	AGND
69	SEN–
70	SIG1–
71	SIG1+
72	SEN+
73	AVCC
74	KOUT7 / I.O 14.0
75	KOUT6 / I.O 14.1
76	KOUT5 / I.O 14.2
77	KOUT4 / I.O 14.3
78	KOUT3 / I.O 14.4
79	KOUT2 / I.O 14.5
80	KOUT1 / I.O 14.6
81	KOUT0 / I.O 14.7
82	KIN7 / I.O 15.0
83	KIN6 / I.O 15.1
84	KIN5 / I.O 15.2

TABLE 5: SOC-3000 QUICK REFERENCE PIN CONFIGURATION FOR LED DISPLAY

PIN	NAME
1	KIN4 / I.O 15.3
2	KIN3 / I.O 15.4
3	KIN2 / I.O 15.5
4	KIN1 / I.O 15.6
5	KIN0 / I.O 15.7
6	VDD
7	BUZZER / P1.7
8	P1.5 (CPU)
9	P1.4 (CPU)
10	XTAL OUT
11	XTAL IN
12	TXD
13	RXD
14	PWR_OFF / P3.4 / Timer 0
15	MAIN_DET / P3.5 / Timer 1
16	EL / P1.6
17	Not Connected
18	OUT / OUT 4.0
19	OUT / OUT 4.1
20	OUT / OUT 4.2
21	OUT / OUT 4.3

PIN	NAME
22	SEG A1 / OUT 5.0
23	SEG B1 / OUT 5.1
24	SEG C1 / OUT 5.2
25	SEG D1 / OUT 6.0
26	SEG E1 / OUT 6.1
27	SEG F1 / OUT 6.2
28	SEG G1 / OUT 6.3
29	SEG DP1 / OUT 7.0
30	SEG A2 / OUT 7.1
31	SEG B2 / OUT 7.2
32	SEG C2 / OUT 7.3
33	SEG D2 / OUT 8.0
34	SEG E2 / OUT 8.1
35	SEG F2 / OUT 8.2
36	SEG G2 / OUT 8.3
37	SEG DP2 / OUT 9.0
38	SEG A3 / OUT 9.1
39	SEG B3 / OUT 9.2
40	SEG C3
41	SEG D3
42	SEG E3

PIN	NAME
43	SEG F3
44	SEG G3
45	SEG DP3
46	DIG 1
47	DIG 2
48	DIG 3 / OUT 10.0
49	DIG 4 / OUT 11.0
50	DIG 5 / OUT 11.1
51	DIG 6 / OUT 11.2
52	DIG 7 / OUT 11.3
53	OUT 12.0
54	OUT 12.1
55	OUT 12.2
56	OUT 12.3
57	OUT 12.4
58	OUT 13.0
59	OUT 13.1
60	OUT 13.2
61	OUT 13.3
62	VCC
63	RESET

PIN	NAME
64	GND
65	VDET / INT 0 ~
66	SIG2+
67	SIG2–
68	AGND
69	SEN–
70	SIG1–
71	SIG1+
72	SEN+
73	AVCC
74	KOUT7/I.O 14.0
75	KOUT6/I.O 14.1
76	KOUT5/I.O 14.2
77	KOUT4/I.O 14.3
78	KOUT3/I.O 14.4
79	KOUT2/I.O 14.5
80	KOUT1/I.O 14.6
81	KOUT0/I.O 14.7
82	KIN7/I.O 15.0
83	KIN6/I.O 15.1
84	KIN5/I.O 15.2

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CPU 80C51TBO

The reference source for data given here is "M8051TBO Technical Specifications", Virtual IP Group, Inc., Version M8051TS97DF01. Refer to this manual for complete CPU specification.

Features

- 8-bit CPU
- Compatible with standard 80C31
- Four 8-bit I/O ports
- Three 16-bit timers
- On-chip oscillator and clock circuitry
- 256-byte on-chip, 8051-compatible SFR RAM
- 64Kbyte program memory with bank switching
- 4Kbyte XDATA RAM for data memory
- High-speed architecture of 4 cycles/instruction
- Dual data pointers

Advantages

- Fast running and improved performance
- No wasted clock and memory cycles
- Works efficiently with all types of peripheral devices
- Improved power consumption characteristics
- On-chip Power-On/Reset

Architecture

The CPU block diagram is presented in Figure 8.

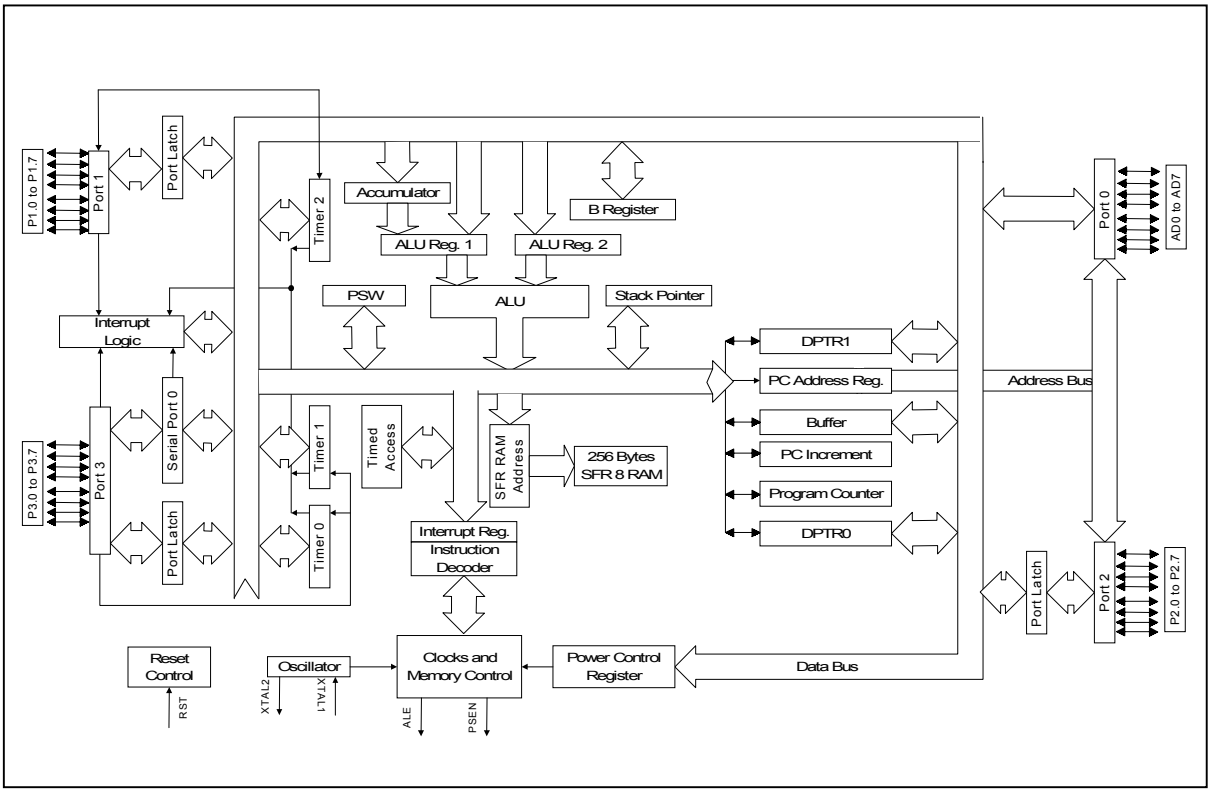

FIGURE 8: CPU BLOCK DIAGRAM

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Memory Organization

The SOC-3000 is an 8051-compatible device with an 80C310 memory chip. As with all such devices, the SOC-3000 has separate address spaces for Program and Data memory. They are:

- Flash memory – memory space containing non-volatile, in-circuit re-programmable code and data (such as calibration data). The code in the Flash memory may be in-circuit programmed at a byte level, although it must first be erased, the erasing being performed in page blocks. The program memory space can be in-circuit programmed through the serial port.
- RAM memory – Random Access memory used as "scratchpad memory" for the software.

Flash (Program & Non-Volatile Data) Memory Mapping and Usage

The 8051-compatible SOC-3000 supports a maximum code space of 64K. Programs larger than 64K are handled by bank switching to select one of a number of code banks residing at one physical address.

In the SOC-3000, there is one 32K Common-Program Area mapped from address 0000H to 7FFFH (Figure 9) and three 32K code banks mapped from code address 8000H to FFFFH (Figure 9). The code banks are selected using bits in a memory- mapped address.

The Flash memory may be dynamically allocated between the Program and the Non-Volatile Data memory. This eliminates the need of external EEPROM usually used for storing calibration parameters and other non-volatile variable data.

The Flash memory is built of 4K Bytes of erasable blocks whose boundary is located at 4k address (multiples of 1000H).

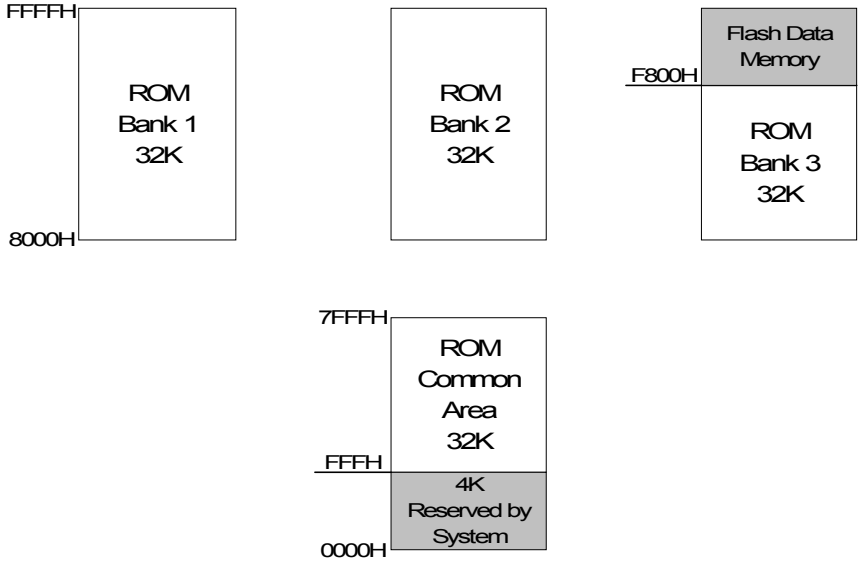

FIGURE 9: SOC-3000 PROGRAM MEMORY MAP

Application Program Start Address

The start address of the application program should be located at 1000H, as the first 4kBytes are reserved for the SOC-3000/I system.

Serial Downloading (In-Circuit Programming)

As part of its embedded boot software the SOC-3000 facilitates serial code and data download via the standard UART serial port. Serial download mode is automatically entered upon power-up or reset if one of the following conditions exist:

1. No valid program is programmed in the Flash memory.
2. A request for download process was initiated via the UART during the first 200 ms after power-up/reset.

Once in this mode, you can download code or data files into the Flash memory, while the device is located on its target board. The is the PC serial download utility, **CybraTech Cloader executable,** is provided together with the device and its documentation and software library.

The SOC-3000/I may be programmed only if, within 200ms after power-up or RESET, it establishes communication with the **Cloader executable**, or if the application program is not available or not valid (checksum error). Figure 10describes the startup procedure of the SOC-3000.

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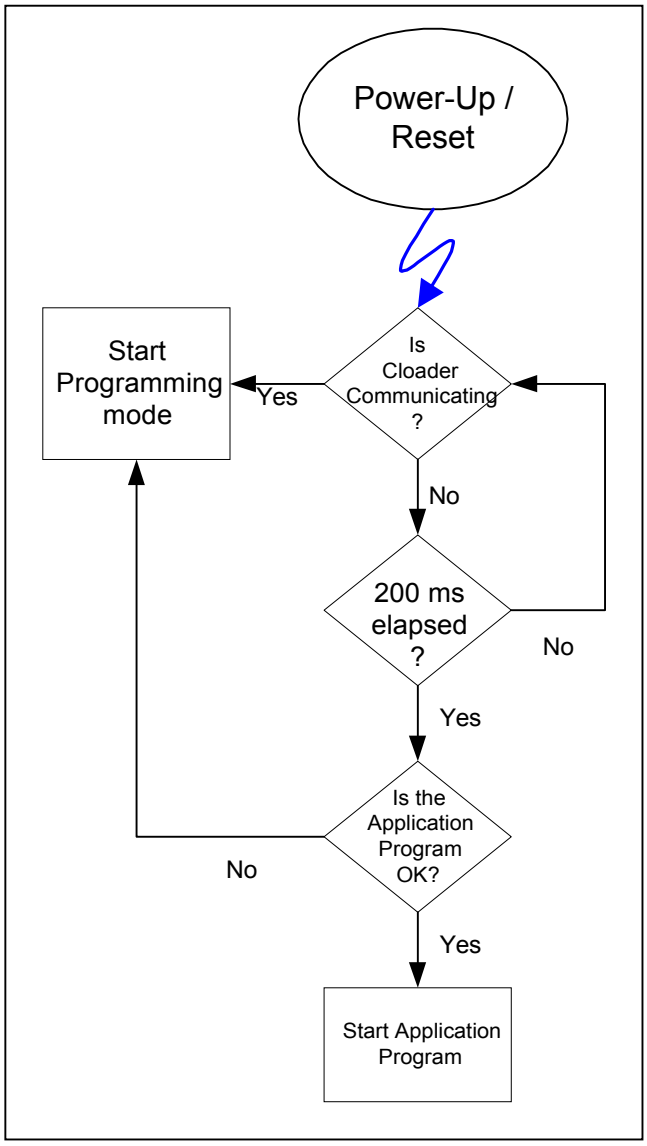

FIGURE 10: SOC-3000/I STARTUP PROCEDURE

Using the Flash for Data Memory

The Flash memory may be used for storing non-volatile data. To update the data area while the program is running, the Flash must be defined as DATA area instead of as CODE area. **CybraTech Flash Manager** software manages this process in an efficient and reliable manner. It provides the means to read, write, erase and update the Flash Data area. A detailed description of the **CybraTech Flash Manager** function is included in the SOC-3000 Software Function Library user manual, document number: SOC-0000-SW01-OM.

Data Memory Mapping

The SOC-3000 "scratchpad" data memory is stored in 4Kbyte RAM mapped as XDATA, as shown in Figure 11, in addition to the CPU 256-byte RAM.

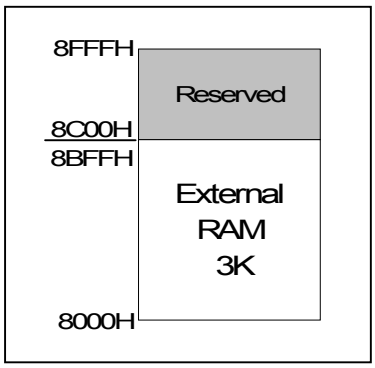

FIGURE 11: SOC-3000 DATA MEMORY MAP

Memory Bank Select Register

The memory bank select register is implemented using the 80C51TBO Port 1 bits P1.0 – P1.1. P1.0 is the least significant bit. Manipulation of other Port 1 I/O pins must be carried out without affecting these bits.

NOTE**: The page register is WRITE ONLY! Reading P1.0-P1.1 may result in an ambiguous result.**

CPU SFRs and Configuration Registers (CFR)

The CPU SFRs (Special Function Registers) are compatible with the 8051 instruction set. For more information, please refer to "M8051TBO Technical Specifications".

The CPU controls the peripherals and their operating modes through Configuration Registers (CFR) mapped as XDATA.

The CFR registers for each peripheral are described below in Table 32, page 62.

Instruction Set

All instructions in the 8051-compatible SOC-3000 instruction set perform the same functions as in the 8051. They identically oversee bit and flag operations and other status functions. Only the clock configuration differs.

For absolute timing of real time events, the timing of software loops can be calculated. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

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In the SOC-3000, the MOVX instruction may take only two machine cycles or eight oscillator cycles, while the "MOV direct, direct" instruction uses three machine cycles or 12 oscillator cycles. Thus, the execution times of the two instructions differ. This is because the SOC-3000 usually uses one instruction cycle for each instruction byte.

Note that a machine cycle requires just four clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five.

Reset

The Reset signal is generated by an internal circuitry in the ASIC. The signal thresholds are:

RESET Falling edge on Vcc=3.98V.

RESET Rising edge on Vcc=4.19V.

The hystheresis of the RESET signal is set so that normal operation of the internal Flash memory is guaranteed.

Interrupt Vectors

The interrupt vectors of the SOC-3000/I are shifted compared with the interrupt vectors of a standard 80C51TBO vectors by an offset of 1000H.

Table 6 details the SOC-3000/I interrupt vectors:

TABLE 6: INTERRUPT VECTORS DESCRIPTION

INTERRUPT SOURCE	FLAG	VECTOR LOCATION	PRIORITY
External Interrupt 0	IE0	1003H	1 (Highest)
Timer 0 Overflow	TF0	100BH	2
External Interrupt 1	IE1	1013H	3
Timer 1 Overflow	TF1	101BH	4
Serial Port	RI + TI	1023H	5
Timer 2 Overflow	TF2 + EXF2	102BH	6

ADC CONTROLLER INTERFACE

Features

- Resolution – 20 bit
- Programmable gain –0.5, 0.75, 1, 1.5, 2
- Programmable sample rate of 5, 10 or 20 samples per second
- Voltage detection input and alarm

Controller Registers

ADC Converter (ADC) controller interface includes a semaphore register (one byte), a control register (two bytes) and a data/status register (four bytes).

The ADC controller registers are defined in Table 7.

TABLE 7: ADC CONTROLLER REGISTERS DESCRIPTION

FUNCTION	ADDRESS	BIT	REMARKS
Controller Clock Enable	C200H	7	1 = Enable 0 =Disable
Controller RESET	C406H	All	0xFF = Reset
Semaphore Register	E100H	0-1	Read/Write
Data Registers	E103H to E106H	All	Read only
Control Register	E101H to E102H	All	Write only

Semaphore Register

The semaphore register bit definitions are shown in Table 8.

TABLE 8: ADC CONTROLLER INTERFACE SEMAPHORE REGISTER BIT DEFINITIONS

ADDRESS	BIT 7 … BIT 2	BIT 1	BIT 0 (LSB)
E100H	Don't Care	Tx Semaphore (Controller to ADC Converter)	Rx Semaphore (ADC Converter to Controller)

Control Register

The control register bit definitions and its functions and are given in Table 9, page 28.

.

TABLE 9: ADC CONTROLLER INTERFACE CONTROL REGISTER BIT FUNCTIONS

BYTE #	ADDRESS	BIT	FUNCTION	SETTINGS
1	E101H	0 (LSB)	Interrupt Enable	**0** = Disable **1** = Enable
		1-7	Don't Care	Don't Care
2	E102H	0-1 (bit 0 – LSB)	Sample Rate	**00** = 20 Hz (default) & F.S=100,000 Counts **01** = 10 Hz & F.S. = 200,000 Counts **10** = 10 Hz& F.S. = 100,000 Counts **11** = 5 Hz& F.S. = 200,000 Counts
		2-4	Gain Power Down	**000** = 0.50 **001** = 0.75 **010** = 1.00 **011** = 1.50 **100** = 2.00 **111** = Power Down
		5	ADC Channel	**0** = Main (default) channel **1** = Secondary channel
		6	Don't Care	Don't Care
		7	Don't Care	Don't Care

Status/Data Registers

The data register bit definitions are shown in Table 10. The bit functions are described in Table 11.

TABLE 10: ADC CONTROLLER INTERFACE DATA REGISTER BIT DEFINITIONS

BYTE #	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	E103H	D7	D6	D5	D4	D3	D2	D1	D0
2	E104H	D15	D14	D13	D12	D11	D10	D9	D8
3	E105H	G1/PD1	G0/PD0	SR1	SR0	D19	D18	D17	D16
4	E106H	0	0	0	0	0	0	CH	G2/PD2

TABLE 11: ADC CONTROLLER INTERFACE DATA REGISTER BIT FUNCTIONS

BIT	FUNCTION
D_i	ADC Reading Data **D0 = LSB** **D19 = MSB**
SR_i	Sample Rate
G_i/PD_i	Gain/Power Down
CH	Active ADC Channel

Operation

Initialization:

To enable the ADC controller interface:

1. Enable the ADC controller interface clock source in Clock Enable register C200H: Set C200H, Bit 7 to 1.
2. Reset the ADC controller interface:
   Write FF to register C406H.
3. Set the Configuration registers (CFR) address for ADC controller interface function:
   CFR address C10CH = 1FH.
4. Enable interrupt:
   Set E101H, Bit 0 to 1.
5. Check the semaphore byte at address E100H.

   If Receive semaphore bit at E100H is Ready (Bit 0 = 0), signaling the CPU that the ADC controller can receive data, the CPU performs the following operations:

   a. Sets the Transmit semaphore bit at E100H to **Busy** (Bit 1 = **1)** to prevent transmission of data from the ADC controller.

   b. Programs the control register **E101–E102H** of the ADC controller to initialize controller operation.

Normal operation:

6. After the ADC controller has been initialized, the following operations are performed:

   a. The CPU resets the Transmit semaphore bit at E100H to **Ready** (Bit 1 = **0**) to signal the ADC controller that it can now transmit data.

   b. The ADC controller sets the Receive semaphore bit at E100H to **Busy** (Bit 0 = **1**) to prevent further data transmission to the controller.

   c. The ADC controller sends ADC converter data to data registers at **E103H** to **E106H.**

7. After sending the data of registers **E103H** to **E106H**, the ADC controller resets the Receive semaphore bit at E100H to **Ready** (Bit 0 = **0**), signaling the CPU that the controller can now receive new data.

   One ADC controller operation cycle is now complete.

Steps 6 through 7 are repeated cyclically.

The ADC internal counts output is dependent upon the input signal, the gain and the operation mode setting. Table 12 defines the relation between the internal counts output of the zero signal input of the full-scale signal and the ADC settings.

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TABLE 12: ADC OUTPUT COUNTS VS. ADC SETTINGS

GAIN	SAMPLE RATE * (HZ)	ADC RESOLUTION MODE * (IN COUNTS)	ADC OUTPUT AT ZERO SIGNAL INPUT (COUNTS)	MAXIMUM FULL-SCALE INPUT (MILLI-VOLTS)	ADC OUTPUT (COUNTS)
0.5	20	100,000	153,200	10	205,000
	10	100,000	153,200	10	205,000
	10	200,000	306,400	10	412,000
	5	200,000	306,400	10	412,000
0.75	20	100,000	153,200	10	231,000
	10	100,000	153,200	10	231,000
	10	200,000	306,400	10	464,000
	5	200,000	306,400	10	464,000
1.0	20	100,000	153,200	10	257,000
	10	100,000	153,200	10	257,000
	10	200,000	306,400	10	514,000
	5	200,000	306,400	10	514,000
1.5	20	100,000	153,200	6.6	257,000
	10	100,000	153,200	6.6	257,000
	10	200,000	306,400	6.6	514,000
	5	200,000	306,400	6.6	514,000
2.0	20	100,000	153,200	5	257,000
	10	100,000	153,200	5	257,000
	10	200,000	306,400	5	514,000
	5	200,000	306,400	5	514,000

* ADC Resolution mode is defined in Table 9, Register E102H, bits 0-1 – Sample Rate.

KEYBOARD CONTROLLER

Features

- Supports up to 64 keys (8×8)
- Programmable anti-bounce mechanism (4-18 ms)
- Automatic key matrix scanning
- Automatically detects excessively long or constant key depression
- When Interrupt mode enabled, generates an interrupt when any key is pressed or released

Functional Description

Keyboard Controller Matrix Configuration

The keyboard matrix configuration showing the 8 × 8 matrix is given in Figure 12. The key values at each junction are in hexadecimal.

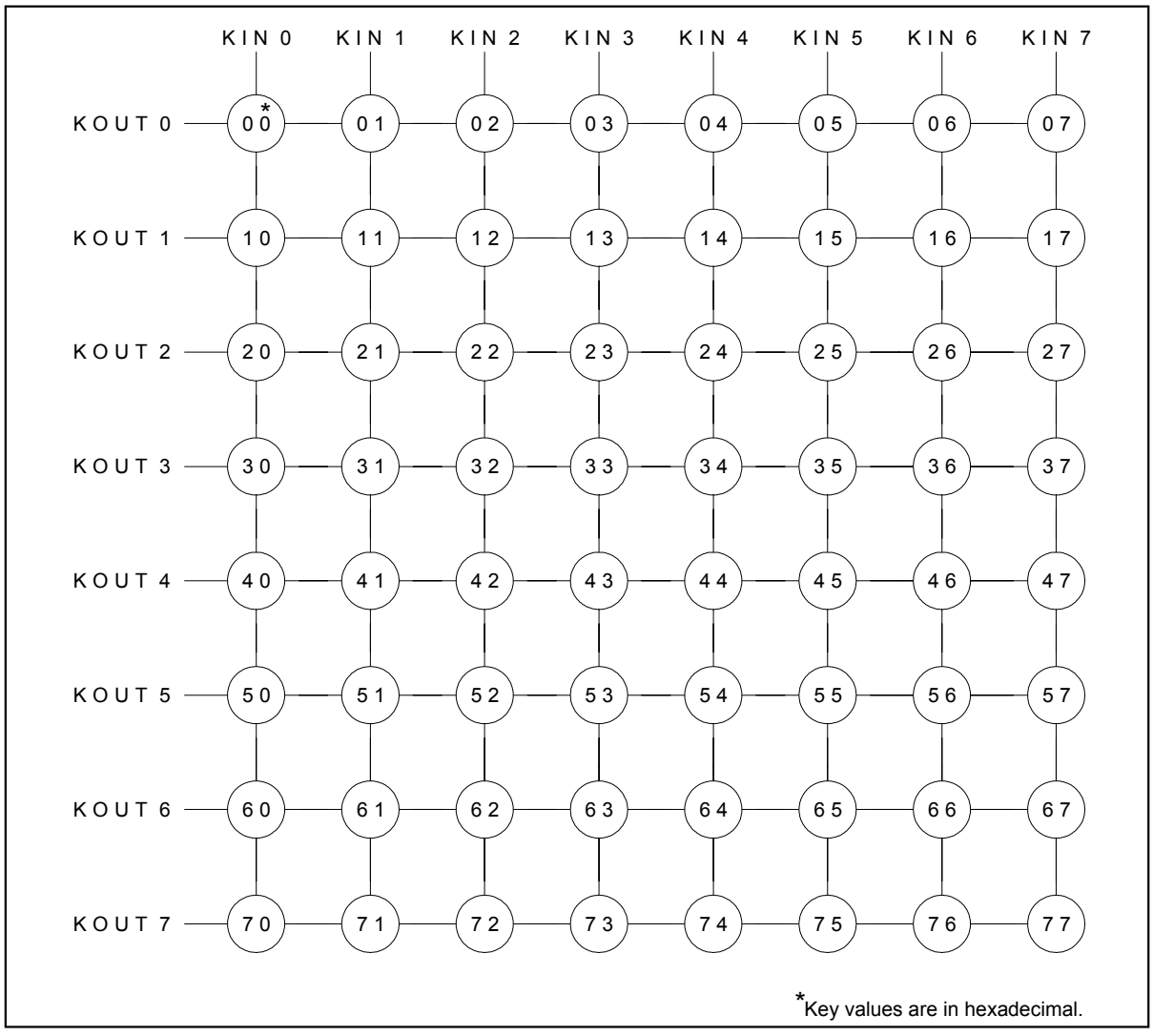

FIGURE 12: KEYBOARD MATRIX CONFIGURATION

Controller Registers

Keyboard controller interface includes a control register (one byte) and a data/status register (two bytes).

The Keyboard controller registers are defined in Table 13.

TABLE 13: KEYBOARD CONTROLLER REGISTERS DESCRIPTION

FUNCTION	ADDRESS	BIT	REMARKS
Controller Clock Enable	**C200H**	2	1= Enable 0= Disable
Controller RESET	**C400H**	All	0xFF = Reset
Data Registers	**F100H** to F**101H**	All	Read only
Control Register	**F100H**	All	Write only

Registers Description

Control Register

The keyboard control register bit definitions, functions, and settings are displayed in Table 14.

TABLE 14: KEYBOARD CONTROLLER CONTROL REGISTER BIT FUNCTIONS

ADDRESS	BIT	FUNCTION	SETTINGS
F100H	0-2 (bit 0 -LSB)	Anti-Bounce Timeout	**000** = 4 ms **001** = 6 ms **010** = 8 ms **011** = 10 ms **100** = 12 ms **101** = 14 ms **110** = 16 ms **111** = 18 ms
	3	Interrupt Enable/Disable	**0** = Enable **1** = Disable (default)
	4-7	Don't Care	Don't Care

Data Registers

Keyboard data is stored in two 8-bit registers.

The data register bit functions are shown in Table 15.

NOTE

*When Control Register Address **F101H**, bit 7 is set to **1** (Released), key-code value bits 0 to 6 in address **F101H** are meaningless.*

TABLE 15: KEYBOARD CONTROLLER DATA REGISTER BIT DEFINITIONS

BYTE #	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	F100H	X	X	X	X	X	X	X	Key Error **0** = Legal **1** = Error
2	F101H	Release Sign **0** = Pressed **1** = Released	D6	D5	D4	D3	D2	D1	D0

Operation

At power on, the keyboard controller is reset and the scanning rate is set to 10 µs.

Initialization:

To enable the keyboard controller:

1. Enable the keyboard controller clock source in Clock Enable register **C200H**:
   Set C200H, Bit 2 to **1**.
2. Reset the keyboard controller:
   Write **FF** to register **C400H**.
3. Set CFR address for keyboard controller function:
   CFR addresses **C10DH** and **C10EH** = **FF** (Table 32, page 62).
   This causes the following results:
   - Enables keyboard input pins (**1** to **5** and **82** to **84)** (Table 32; page 62; Table 1, page 9; Table 2, page 12)
   - Enables keyboard output pins (**74** to **81**) (Table 32, Table 1, Table 2)
4. Enable keyboard interrupt:
   Set F100H, Bit 3 to **0**.
5. Set anti-bounce timeout:
   Set F100H, Bits 0, 1 and 2, as shown in Table 14.

Normal Operation:

6. Read keyboard key-code value bits, as follows:
   - Read register F100H, Bit 0:
     If **0**, key-code value is legal.
     If **1**, key-code value is illegal (Error).
   - Read key code from register F101H, bits 0 to 6:
     When key pressed, values are valid.
   - Read F101H, bit 7:
     If 0, key pressed and keyboard values (bits 0 to 6) are valid.
     If 1, key released and keyboard values are meaningless.

LCD CONTROLLER/DRIVER

Features

- Selectable backplane drive configuration, static or multiplex drive ratios of 1:2, 1:3 or 1:4
- Selectable display bias configuration, static, or 1/2 bias or 1/3 bias
- Internal LCD bias generation with voltage-follower buffers
- Drives up to 40 segments with the capacity to generate 20 numeric characters
- 20 × 8-bit memory display data
- User-selected LCD voltages

Functional Description

The SOC-3000 LCD controller/driver interfaces to LCD (Liquid Crystal Display) with low multiplex rates.

The controller/driver generates drive signals for static drive mode (no multiplexing) or multiplexed LCDs with multiplex drive ratios of 1:2, 1:3 or 1:4, depending on the number of backplane outputs. The driver supports up to four backplanes, each supporting 40 segments.

The LCD Controller/Driver block diagram is shown in Figure 13.

The driver supports numeric, alphanumeric and dot matrix display configurations. The number of characters of each type that can be displayed depends on the number of backplanes and the number of segments required per character. The maximum display capacity for each display configuration is shown in Table 16.

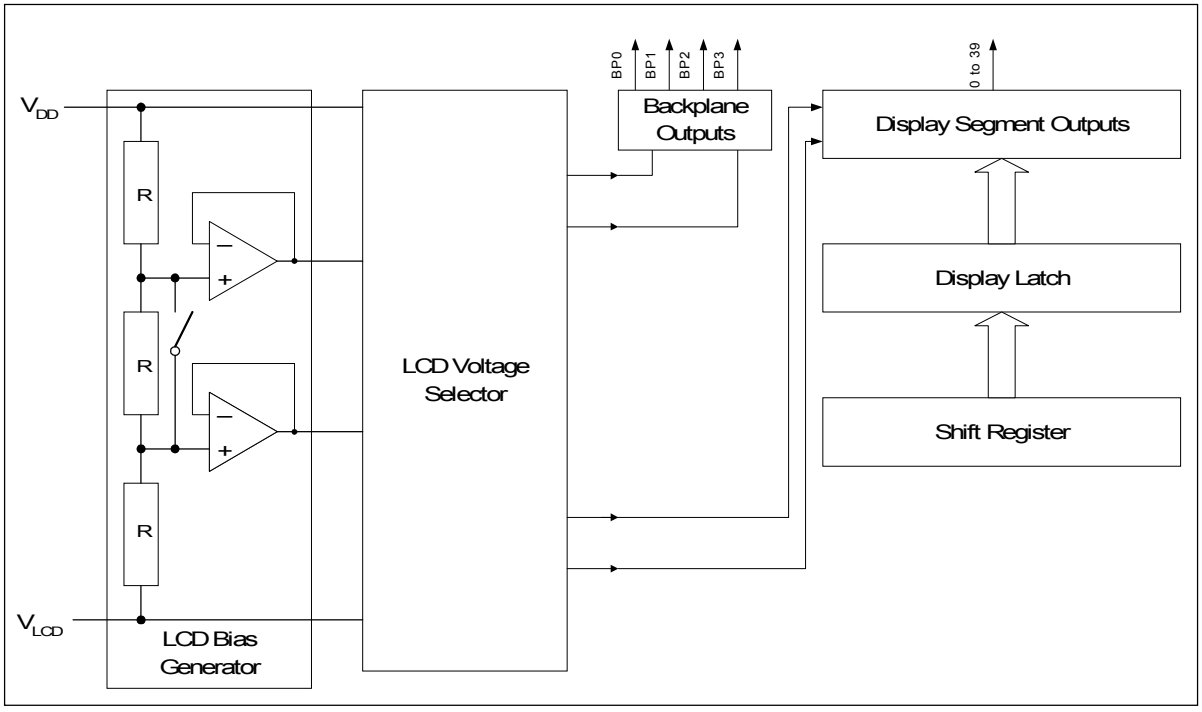

FIGURE 13: LCD CONTROLLER/DRIVER BLOCK DIAGRAM

TABLE 16: MAXIMUM DISPLAY CAPACITY PER DISPLAY CONFIGURATION

NUMBER OF BACKPLANES	SEGMENTS OR SYMBOLS	NUMERIC (7 SEGMENTS)
4	160	20
3	120	15
2	80	10
1	40	5

LCD Bias Generator

The operative LCD voltage is derived from $V_{DD} - V_{LCD}$ (Figure 13). The three resistors connected in series between V_{DD} and V_{LCD} in the bias generator function as a voltage divider to produce 1/2 (for the 1:2 multiplex drive ratio) and 1/3 (for the 1:2, 1:3 and 1:4 multiplex drive ratio) biasing voltages. The bias configuration for each of the multiplex drive ratios is given in Table 17.

For additional information on LCD drivers refer to LCD driver components datasheets such as Phillips PCF8756.

TABLE 17: LCD BIAS CONFIGURATIONS

MULTIPLEX DRIVE MODE	# BACKPLANES	# LEVELS	BIAS CONFIGURATION
Static	1	2	Static
1:2	2	3	1/2
1:2	2	4	1/3
1:3	3	4	1/3
1:4	4	4	1/3

Drive Mode Waveforms

The waveforms for the Static drive mode are given in Figure 14, page 37.

The waveforms for the 1:2 Multiplex Drive Ratio–1/2 Bias are given in Figure 15, page 38.

The waveforms for the 1:2 Multiplex Drive Ratio–1/3 Bias are given in Figure 16, page 39.

The waveforms for the 1:3 Multiplex Drive Ratio are given in Figure 17, page 40.

The waveforms for the 1:4 Multiplex Drive Ratio are given in Figure 18, page 41.

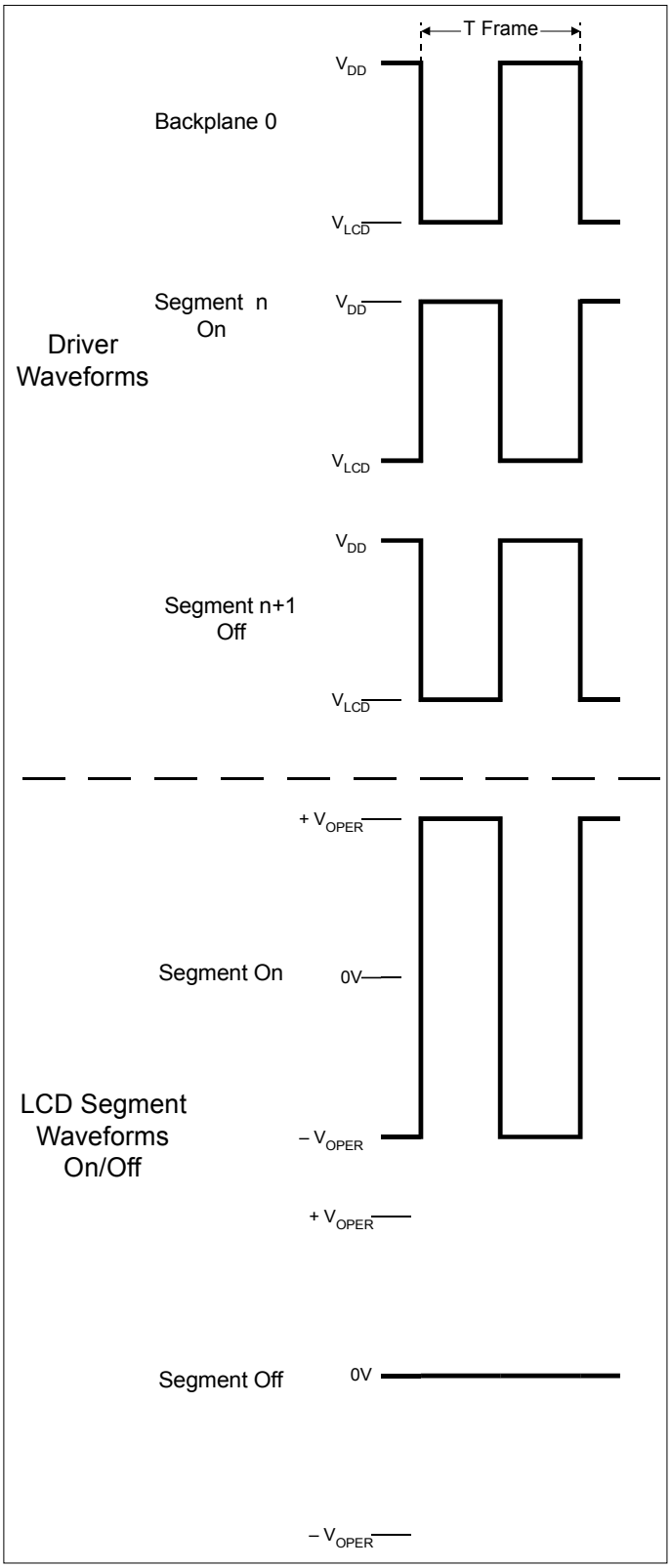

FIGURE 14: STATIC DRIVE MODE WAVEFORMS

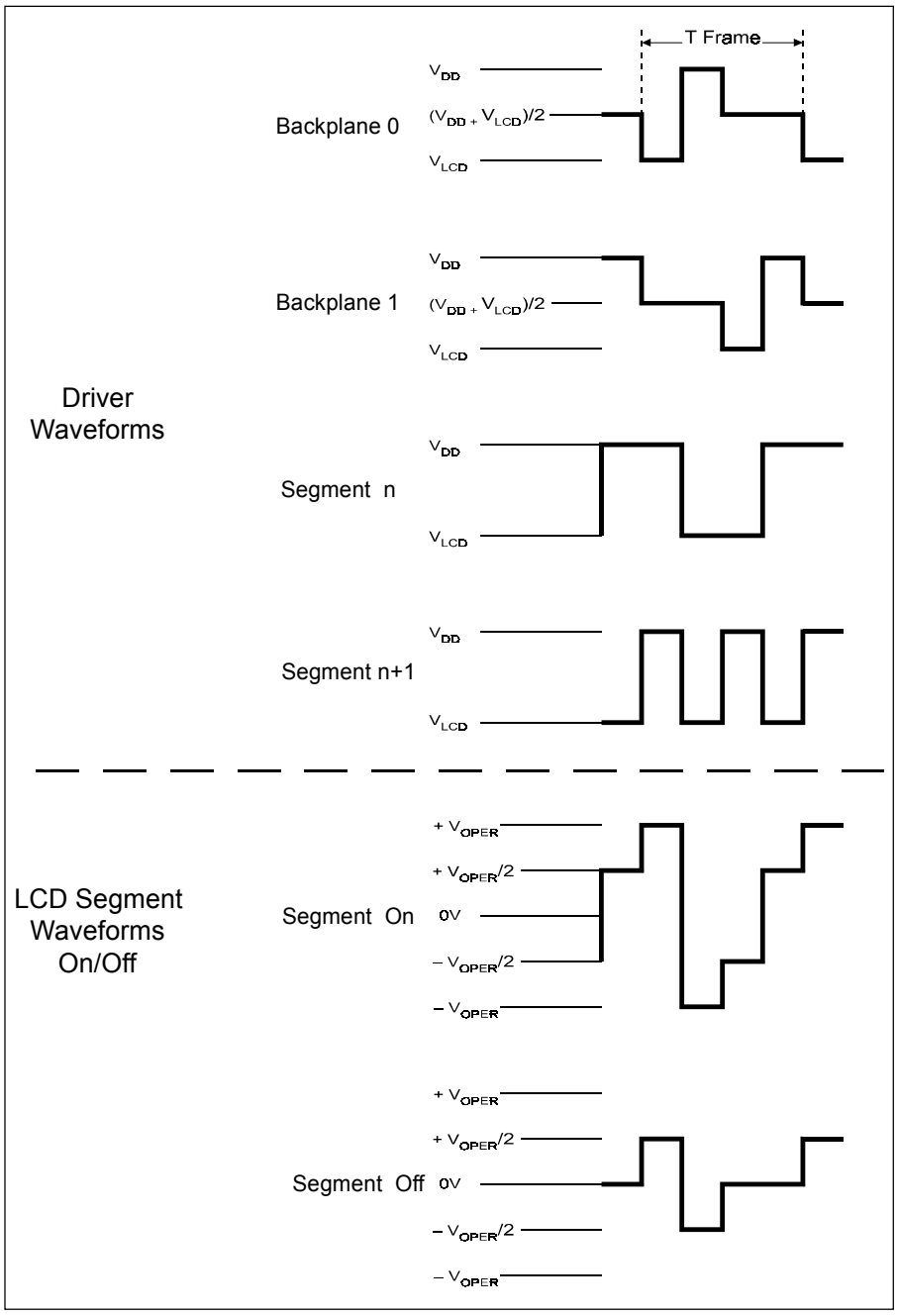

FIGURE 15: 1:2 MULTIPLEX DRIVE RATIO–1/2 BIAS WAVEFORMS

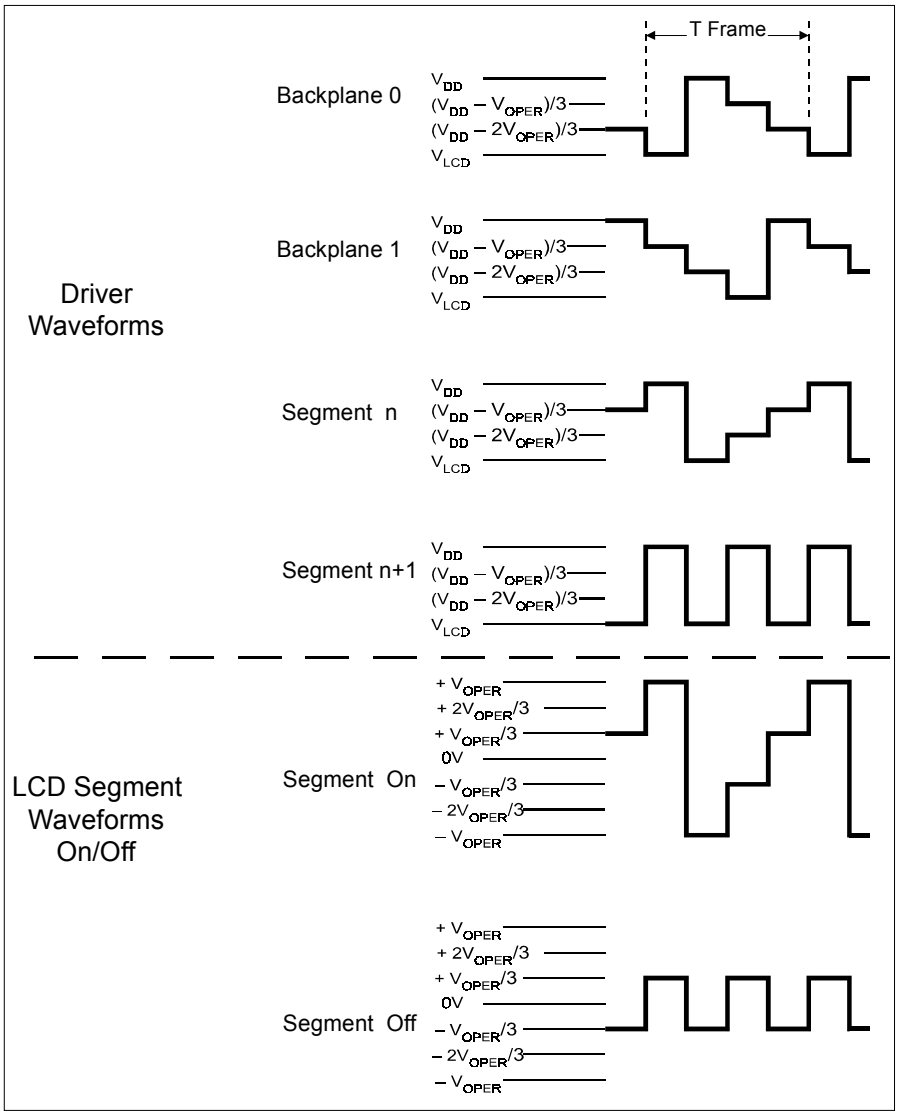

FIGURE 16: 1:2 MULTIPLEX DRIVE RATIO–1/3 BIAS WAVEFORMS

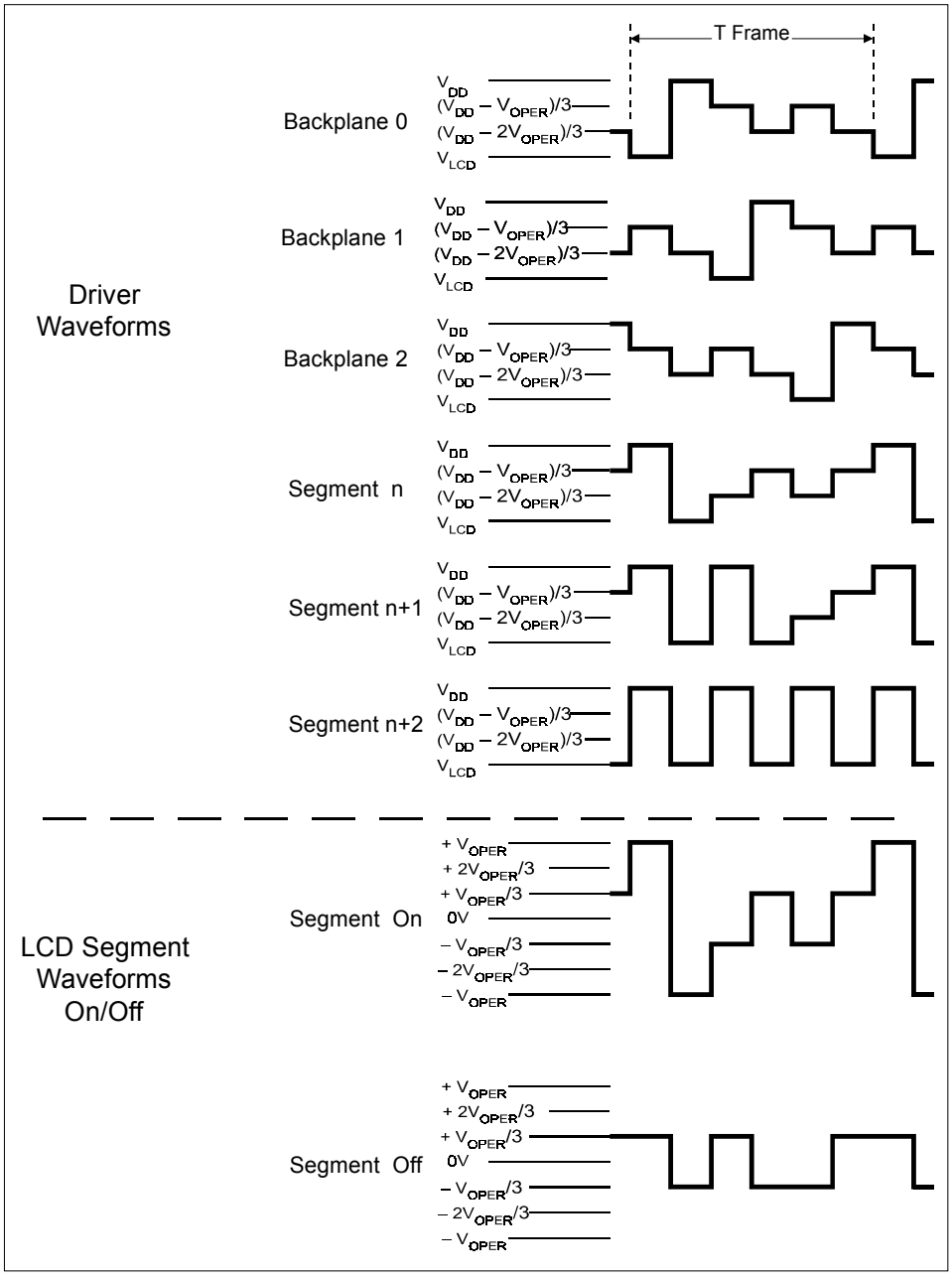

FIGURE 17: 1:3 MULTIPLEX DRIVE RATIO WAVEFORMS

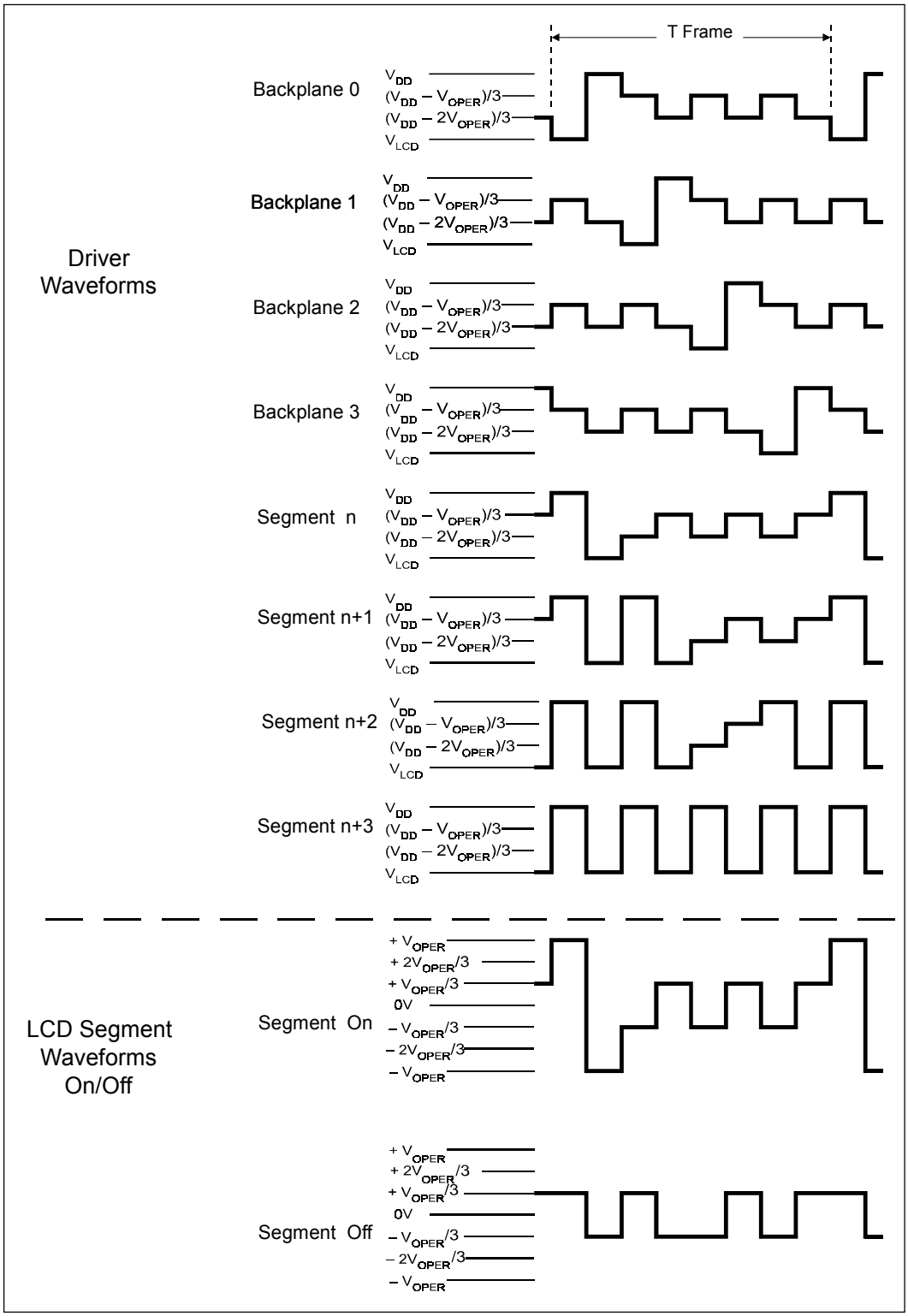

FIGURE 18: 1:4 MULTIPLEX DRIVE RATIO WAVEFORMS

Registers Description

LCD controller /driver command and data are stored in a 21-byte × 8-bit, static display RAM with one control register and 20 data registers.

The controller registers are defined in Table 18.

TABLE 18: LCD CONTROLLER/DRIVER REGISTERS DESCRIPTION

FUNCTION	ADDRESS	BIT	REMARKS
Controller Clock Enable	**C200H**	0	1= Enable 0= Disable
Controller RESET	**C401H**	All	0xFF = Reset
Data Registers	**C801H** to **C814H**	All	Write only
Control Register	**C800H**	All	Read/Write

Control Register

The control-register bit definitions and functions are displayed in Table 19. The Type definitions are **Static** and **Dynamic**: Static bits update only after an external Reset and first chip select (first command write cycle). Dynamic bits can be updated at any time.

TABLE 19: LCD CONTROLLER CONTROL REGISTER BIT FUNCTIONS

ADDRESS	BIT	NAME	UPDATE	FUNCTION	SETTINGS	
C800H	0-1 (0-LSB)	M0 and M1	After Reset Only	Bits 0 (M0) and 1 (M1) set the multiplex drive ratio.	**00** = Static (5 seven-segment digits) **01** = 1:2 (10 seven-segment digits) **10** = 1:3 (15 seven-segment digits) **11** = 1:4 (20 seven-segment digits)	
	2	B	After Reset Only	Sets the bias voltage.	**0** = 1/2 **1** = 1/3	
	3	E	Anytime	Sets LCD display operation.	**0** = Disable **1** = Enable	
	4-6	X0 (LSB), X1 and X2	After Reset Only	Bits 4 (X0), 5 (X1) and 6 (X2) set the refresh clock frequency.	**000** = 52 Hz **001** = 104 Hz **010** = 156 Hz **011** = 208 Hz	**100** = 62 Hz **101** = 125 Hz **110** = 178 Hz **111** = 250 Hz
	7	C	Anytime	Sets the command operating mode.	**0** = Continuous Data Reading **1**= Command Only	

Data Registers

LCD display data is stored in a 20-byte × 8-bit RAM. The number of registers used depends on the number of digits displayed, 5, 10, 15 or 20. The data register bit definitions for a 20-digit display, for which the entire RAM is used, are shown in Table 20.

TABLE 20: LCD CONTROLLER DATA REGISTER BIT DEFINITIONS – 20-DIGIT DISPLAY

Byte #	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	C801H	DP	g	f	e	d	c	b	a
2	C802H	DP	g	f	e	d	c	b	a
…	…	…	…	…	…	…	…	…	…
20	C814H	DP	g	f	e	d	c	b	a

For other displays, Data Registers utilization is as follows:

- For 15-digit command, write data to C801H to C80FH
- For 10-digit command, write data to C801H to C80AH
- For 5-digit command, write data to C801H to C805H

Each byte in the register defines a seven-segment digit and decimal point (DP). Each bit of a register address corresponds to a segment of each digit, as shown in Figure 19. When the bit is set to **1**, it is on. When it is set to **0**, it is off. Figure 19 also shows the backplane outputs per LCD digit for each multiplex drive ratio.

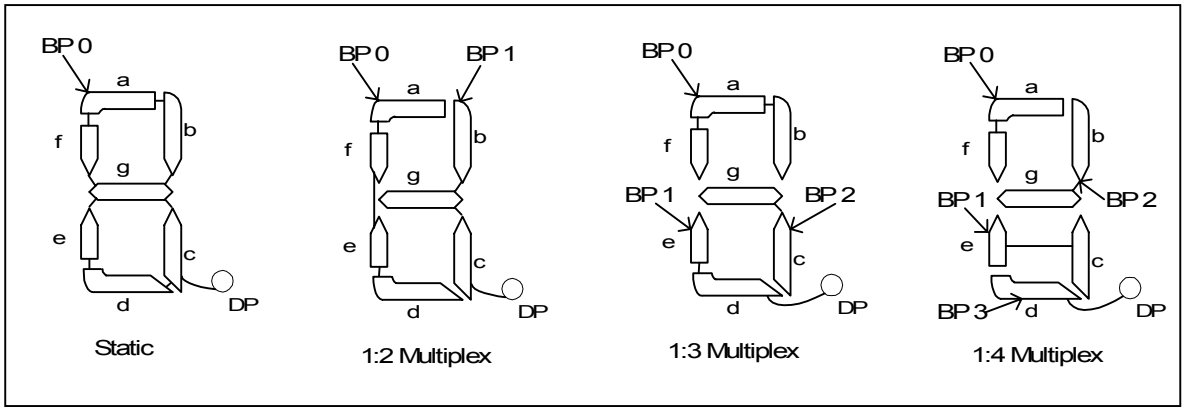

FIGURE 19: BACKPLANE OUTPUTS PER LCD DIGIT

Operation

Initialization:

At power on, the LCD controller performs the following operations:

1. Resets its backplane and segment outputs to V_{DD}.
   After power on, the actual operating LCD voltage V_{OPER} is set according to the multiplexing drive mode and the bias generator.
2. After reset, the LCD pins are routed to the Output function.

To enable the LCD controller:

1. Enable the LCD controller clock source in Clock Enable register **C200H**:
   Set C200H, Bit 0 to **1**.
2. Reset the LCD controller:
   Write **FF** to register **C401H**.
3. Set CFR addresses for LCD controller function:
   CFR addresses **C101H** to **C10BH** = **00H** (Table 32, page 62).
   This enables LCD controller output pins (**18** to **61**) (Table 32, page 62; Table 1, page 9).

Normal Operation:

4. Write data to LCD data registers **C801H** to **C814H**.
5. Set Write command in LCD control register **C800H**.
6. Repeat steps 4 and 5 for new data.

The trigger for sending the data out to the display interface is:

Programming the control register at address C800H **AND** writing data to the LCD data registers (C801H to C814H).

LED PARALLEL DISPLAY CONTROLLER

Features

- Supports up to 21 digits (7 segments + Decimal Point)
- Power-save by LED refresh mechanism
- Programmable-display data registers
- Supports common-anode, seven-segment LED

Functional Description

The LED display block diagram showing the relationship between the 21-digit LED display, the SOC-3000 LED controller and the data register is given in Figure 20.

The LED Controller timing diagram is shown in Figure 21.

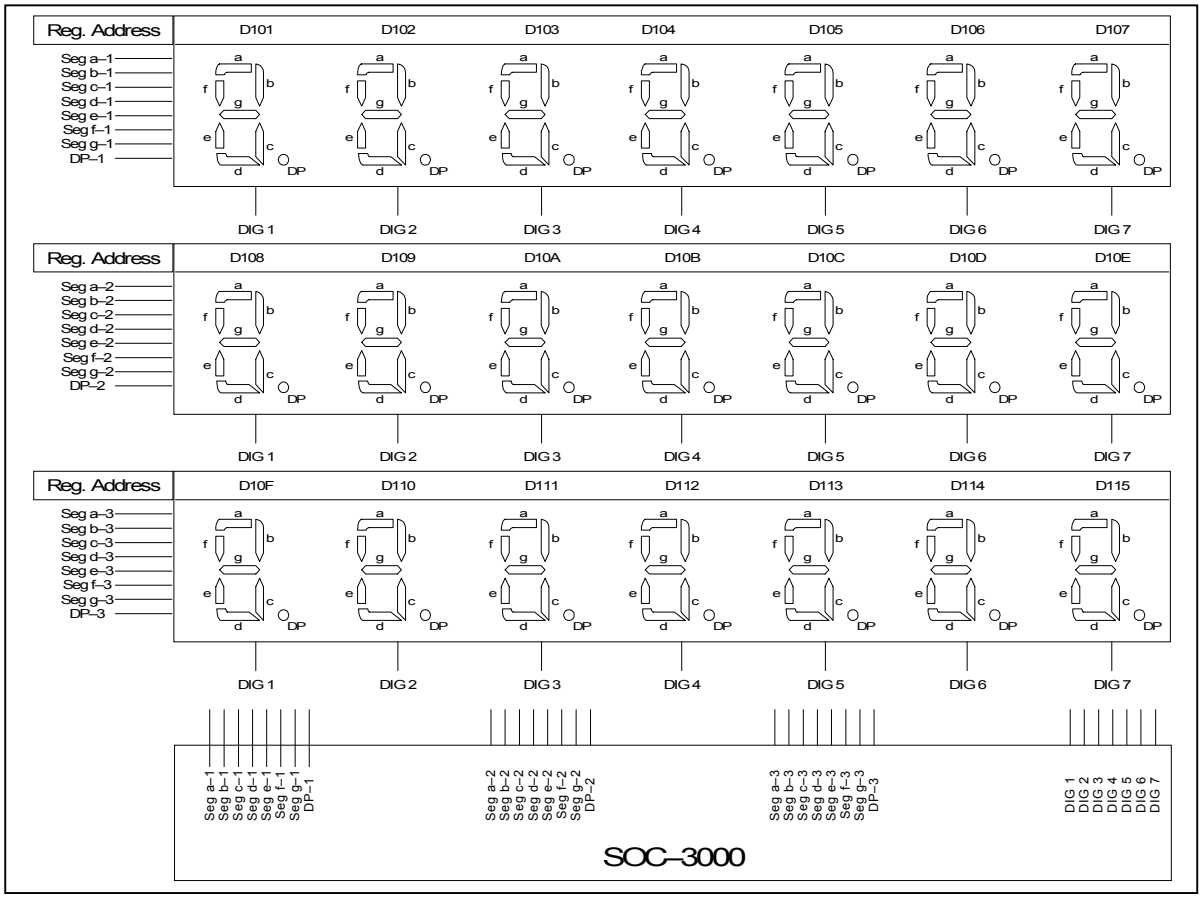

FIGURE 20: LED PARALLEL DISPLAY CONTROLLER BLOCK DIAGRAM

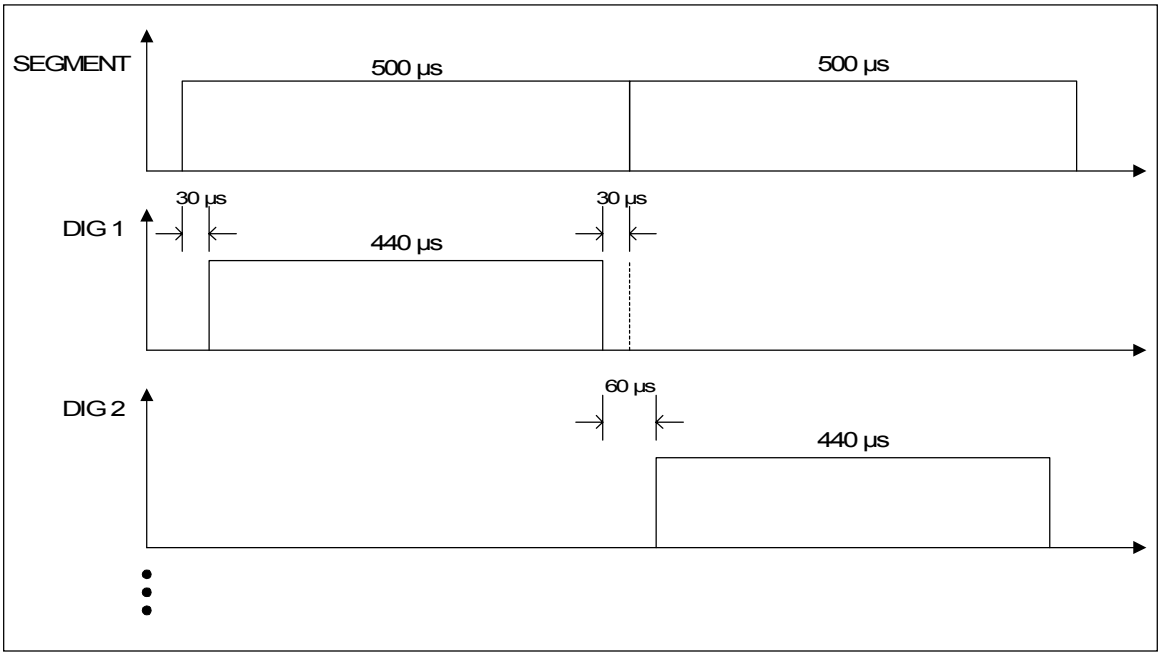

FIGURE 21: LED PARALLEL DISPLAY CONTROLLER TIMING DIAGRAM

Registers Description

The LED controller registers are defined in Table 21.

TABLE 21: LED PARALLEL DISPLAY CONTROLLER DRIVER REGISTERS DESCRIPTION

FUNCTION	ADDRESS	BIT	REMARK
Controller Clock Enable	C200H	1	1= Enable 0= Disable
Controller RESET	C402H	All	0xFF = Reset
Semaphore Bit	D100H	0	Read only
Data Registers	D101H to D115H	All	Write only

LED display data is stored in a 21-byte × 8-bit static display RAM. The display RAM has one Read-only semaphore register containing the semaphore byte and 21 Write-only data registers.

All 22 bytes (one semaphore byte and 21 data bytes) must be written before any new data is applied.

Semaphore Register

The Semaphore register bit definitions are shown in Table 22.

TABLE 22: LED PARALLEL DISPLAY CONTROLLER SEMAPHORE REGISTER BIT DEFINITIONS

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
D100H	X	X	X	X	X	X	X	E

Only Bit 0, the Semaphore bit, is active in the LED Controller control register (Table 23). The semaphore is used to synchronize the access to the control registers.

TABLE 23: LED PARALLEL DISPLAY CONTROLLER SEMAPHORE REGISTER BIT FUNCTIONS

BIT	NAME	TYPE	FUNCTION	SETTINGS
0	E	Read-only	Semaphore bit	0 = Ready 1 = Busy

Data Registers

LED data is stored in a 21-byte × 8-bit RAM.

The data is organized in three groups of seven digits, as follows:

- Group 1: **D101H** to **D107H** - multiplexed on SEC A1 to DP1 Pins.
- Group 2: **D108H** to **D10EH** - multiplexed on SEC A2 to DP2 Pins.
- Group 3: **D10FH** to **D115H** - multiplexed on SEC A3 to DP3 Pins.

The data register bit definitions for a 21-digit display are shown in Table 24.

TABLE 24: LED PARALLEL CONTROLLER DATA REGISTER BIT DEFINITIONS

GROUP	BYTE #	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	1	D101H	DP	g	f	e	d	c	b	a
	2	D102H	DP	g	f	e	d	c	b	a
	3 to 7	D103H to D107H	DP	g	f	e	d	c	b	a
2	8	D108H	DP	g	f	e	d	c	b	a
	9	D109H	DP	g	f	e	d	c	b	a
	10 to 14	D10AH to D10EH	DP	g	f	e	d	c	b	a
3	15	D10FH	DP	g	f	e	d	c	b	a
	16	D110H	DP	g	f	e	d	c	b	a
	17 to 21	D111H to D115H	DP	g	f	e	d	c	b	a

Note:

The trigger for sending the data to the display hardware is writing data to address D115H.

Operation

At power-on or reset the LED Parallel display controller is disabled.

Initialization:

To enable the LED Parallel display controller:

1. Enable the controller clock source in Clock Enable register **C200H**:
   Set C200H, Bit 1 to **1**.
2. Reset the controller:
   Write **FF** to register **C402H**.
3. Set CFR addresses for LED Parallel display controller function:
   CFR addresses **C103H** to **C109H** = **55H**,
   CFR address **C10A** = **15H** (Table 32, page 62).
   These result in the following operations:
   - Enable LED parallel display controller output pins (**22** to **52**) (Table 32, page 62; Table 2, page 12).
   - Check semaphore bit in LED parallel display controller semaphore register at address **D100H**.

Normal Operation:

4. If semaphore bit is Ready (Bit 0 set to **0**), write data to Data register addresses **D101H** to **D115H**.
5. Set Write command:
   Write **01H** to **D100H**.

The trigger for sending the data out to the display serial interface is:

- Programming the semaphore register at address D100H **AND** writing data to the 21 data registers (D101H to D115H).

OR

- Programming the semaphore register at D100H **AND** writing data to the last data register at D115H.

As soon as the controller starts to send the data, it sets the semaphore bit to **1**, indicating that it is busy.

When the controller finishes data output, it resets the semaphore bit to **0**, indicating that it is available for a new operation.

LED SERIAL INTERFACE DISPLAY CONTROLLER

Features

- Supports up to 24 digits
- Serial interface
- Programmable control-signal polarity
- Programmable data registers
- Supports common-anode, seven-segment LED

Functional Description

The LED Serial Interface display comprises three groups of eight digits. The controller diagram showing the division of the 24-byte register into three eight-byte groups and the operation cycle is given in Figure 22.

The LED Serial Interface Display Controller timing diagram is shown in Figure 23. The clock rate is 2 MHz.

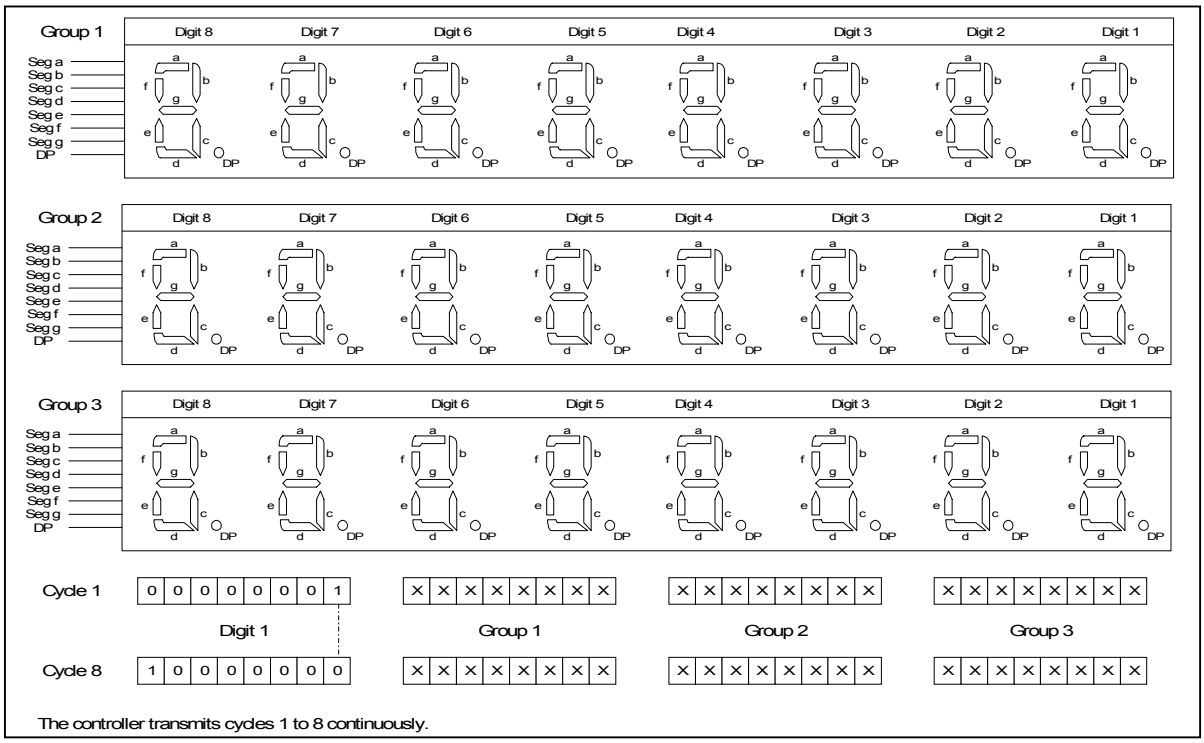

FIGURE 22: LED SERIAL INTERFACE DISPLAY BLOCK DIAGRAM

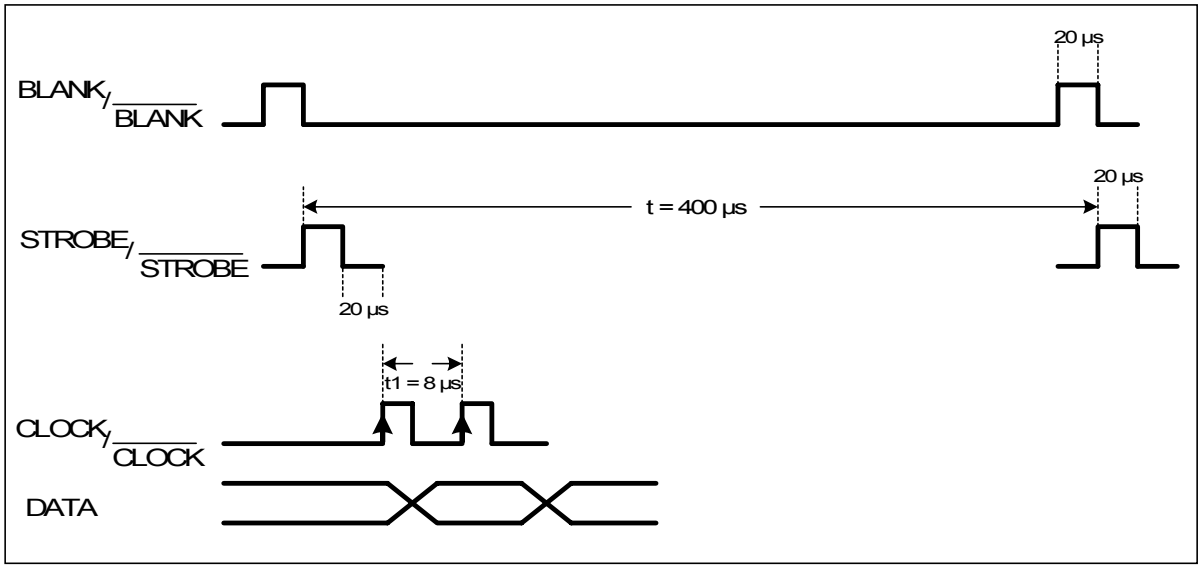

FIGURE 23: LED SERIAL INTERFACE CONTROLLER TIMING DIAGRAM

Registers Description

The LED Serial controller registers description is given in Table 25.

TABLE 25: LED SERIAL CONTROLLER DRIVER REGISTERS DESCRIPTION

FUNCTION	ADDRESS	BIT	REMARKS
Controller Clock Enable	C200H	5	1= Enable 0= Disable
Controller RESET	C403H	All	0xFF = Reset
Semaphore register	D201H		Read only
Data Registers Group 1 Group 2 Group 3	 D201H to D208H D209H to D210H D211H to D218H		 Write Only Write Only Write Only
Control Register	D200H		Read/Write

LED data is stored in a 24-byte × 8-bit static display RAM. The data registers are divided into three groups, each group containing eight bytes with the segment data for eight digits. Thus, the LED display can be formatted to display eight, 16 or 24 digits.

The display RAM has one Read/Write control register containing the Command byte and a Read-only semaphore byte that informs the system if the display is Busy or Ready to initiate writing of LED data. The semaphore byte address also serves as first address of the Write-only data register.

The trigger for sending the data out to the display serial interface is programming the control register at address D200H. As soon as the controller starts to send data, it sets the semaphore byte to **FFH**, indicating that it is busy.

The data is sent serially, Group 1 Digit 8 (left-most digit of the first group) most-significant bit (MSB) first, and continuously until Group 3 Digit 1 least-significant bit (LSB) last.

When the controller has finished data output, it resets the semaphore byte to **0**, indicating that it is available for a new operation.

Control Register

The definitions and functions of the control-register Command-byte bits are displayed in Table 26.

TABLE 26: LED SERIAL INTERFACE DISPLAY CONTROL REGISTER BIT FUNCTIONS

ADDRESS	BIT	NAME	FUNCTION	SETTINGS
D200H	0 (LSB)	C	Command bit	**0** = Command Only **1** = Command + Data
	1	X	N/A	Don't Care
	2	Blank Polarity	Sets the Blank polarity.	**0** = Negative Logic **1** = Positive Logic
	3	Strobe Polarity	Sets the Strobe polarity.	**0** = Negative Logic **1** = Positive Logic
	4	Clock Polarity	Sets the Clock polarity.	**0** = Negative Logic **1** = Positive Logic
	5	E	Enables and disables the display.	**0** = Disable Display **1** = Enable Display
	6	Block	Opens communication or blocks the hardware communication lines.	**0** = Close communication **1** = Open communication
	7	N/A	N/A	Don't Care

Semaphore Register

The semaphore byte is located at address **D201H**, which is the first address of the Write-only data register. This address is Read-only for the semaphore byte. The semaphore byte bit definitions are identical. The settings are:

- Controller is **Busy**: Bits 0 to 7 set to **1 (FFH)**.
- Controller is **Ready**: Bits 0 to 7 set to **0 (00H)**.

Data Registers

The display data is stored in a 24-byte × 8-bit RAM area.

The data register bit definitions for a 21-digit display are shown in Table 27. The registers are Write-only.

TABLE 27: LED SERIAL INTERFACE DISPLAY DATA REGISTER BIT DEFINITIONS

GROUP #	DIGIT #	BYTE #	ADDRESS	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	8	1	D201H	DP	g	f	e	d	c	b	a
	7	2	D202H	DP	g	f	e	d	c	b	a
	6	3	D203H	DP	g	f	e	d	c	b	a
	5	4	D204H	DP	g	f	e	d	c	b	a
	4	5	D205H	DP	g	f	e	d	c	b	a
	3	6	D206H	DP	g	f	e	d	c	b	a
	2	7	D207H	DP	g	f	e	d	c	b	a
	1	8	D208H	DP	g	f	e	d	c	b	a
2	8	9	D209H	DP	g	f	e	d	c	b	a
	7	10	D20AH	DP	g	f	e	d	c	b	a
	6	11	D20BH	DP	g	f	e	d	c	b	a
	5	12	D20CH	DP	g	f	e	d	c	b	a
	4	13	D20DH	DP	g	f	e	d	c	b	a
	3	14	D20EH	DP	g	f	e	d	c	b	a
	2	15	D20FH	DP	g	f	e	d	c	b	a
	1	16	D210H	DP	g	f	e	d	c	b	a
3	8	17	D211H	DP	g	f	e	d	c	b	A
	8	18	D212H	DP	g	f	e	d	c	b	a
	8	19	D213H	DP	g	f	e	d	c	b	a
	8	20	D214H	DP	g	f	e	d	c	b	a
	8	21	D215H	DP	g	f	e	d	c	b	a
	8	22	D216H	DP	g	f	e	d	c	b	a
	8	23	D217H	DP	g	f	e	d	c	b	a
	8	24	D218H	DP	g	f	e	d	c	b	a

Operation

At power-on or reset the LED Serial Interface display controller is disabled.

Initialization:

To enable the LED Serial Interface display controller:

1. Enable the controller clock source in Clock Enable register **C200H**:
   Set C200H, Bit 5 to **1**.
2. Reset the controller:
   Write **FF** to register **C403H**.
3. Check CFR address for LED serial Interface display controller function:
   CFR address **C101H** = **AA** (Table 32, page 62).
   This results in the following operations:
   - Enables serial controller output pins (**58** to **61)** (Table 32, page 62)
   - Check semaphore byte at address **D201H**.

Normal Operation:

4. If semaphore byte is Ready (Bits 0 to 7 set to **0**), write data to Data register addresses **D201H** to **D218H**.
5. Set Write command at the controller Control register address D200H.
6. Repeat steps 4 and 5 for new data.

PROGRAMMABLE FREQUENCY CONTROLLER

Features

- Programmable CPU clock frequency: 16, 8, 4, 2, 1 or 0.5 MHz
- Driven by a 16-MHz resonator or crystal oscillator

Functions

- Generates independent clocks for the CPU and controllers (ADC converter, display, keyboard, watchdog timer, etc.)

Clock Generator Block Diagram

The clock generator block diagram is presented in Figure 24.

Functional Description

Dividing the 16-MHz frequency source according to the control register setting generates the CPU clock frequency.

The CPU clock can be set to 16, 8, 4, 2, 1 or 0.5 MHz.

Switching CPU frequency:

- To switch from the 16-MHz frequency to any other frequency, program the frequency-controller control register as shown in Table 28.
- To switch from any frequency (other than 16 MHz) to another frequency, first switch to 16 MHz and then switch to the desired frequency.

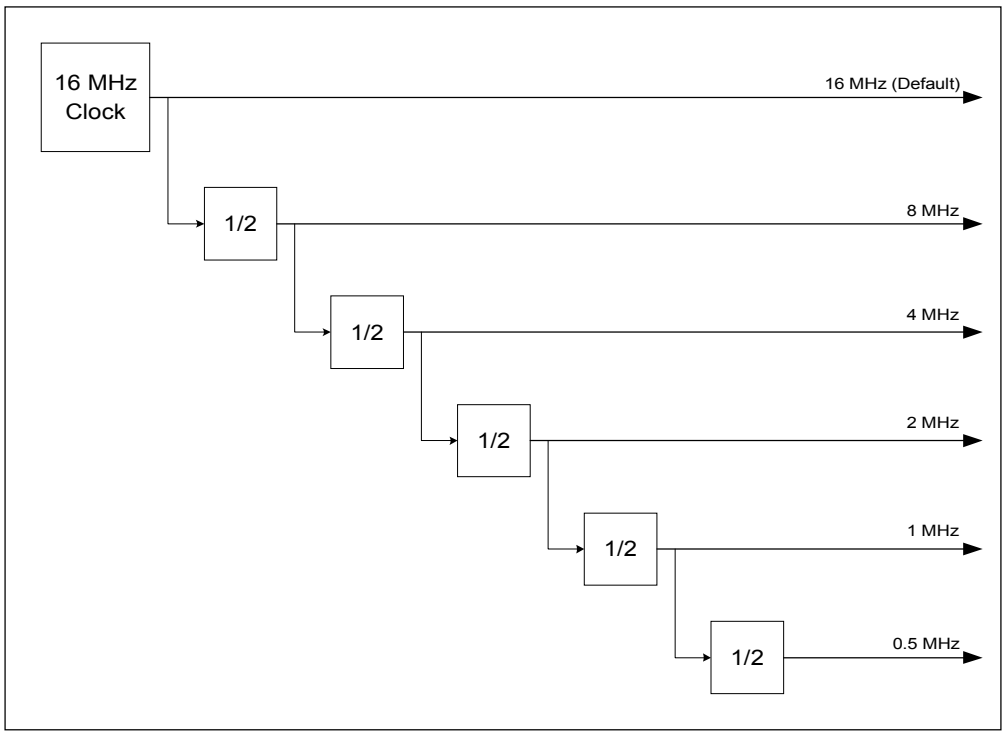

FIGURE 24: CLOCK GENERATOR BLOCK DIAGRAM

Operation

At Power on or Reset, the CPU frequency clock output is set to 16 MHz.

The clocks for the controllers is fixed and derived directly from the external frequency source.

The Frequency controller setting derives the CPU clock, as defined in Table 28.

Control Registers Description

The clock frequency is programmed from a single 8-bit control register.

The address of the clock frequency control register is **E800H**.

The bit settings at **E800H** that define the clock frequency are given in Table 28.

TABLE 28: CLOCK FREQUENCY CONTROL REGISTER BIT SETTINGS

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	CPU CLOCK
E800H	Don't Care					0	0	0	16 MHz
						0	0	1	8 MHz
						0	1	0	4 MHz
						0	1	1	2 MHz
						1	0	0	1 MHz
						1	0	1	0.5 MHz

WATCHDOG TIMER

Functions

The purpose of the watchdog timer is to generate a CPU reset at specified intervals. If the SOC-3000 software does not interrupt the watchdog cycle and instead enters an erroneous state, the watchdog time carries out its CPU reset one second after the software was supposed to make its interrupt. The erroneous state may be due to a programming error. The watchdog may be disabled or re-triggered via its control register.

Functional Description

The operating parameters of the watchdog timer are presented in Table 29.

TABLE 29: WATCHDOG TIMER OPERATING PARAMETERS

PARAMETER	VALUE
Time Constant	1 second
Trigger	By the control register (WDI)
Enable/Disable	By the control register (ENWD)
Power Up Mode	Disabled

Operation

The application software controls the watchdog operation. It is automatically disabled in the In-circuit Emulator (ICE) mode and after power-up or reset.

The application software should activate the watchdog as soon as it starts normal operation after power-on or reset conditions.

The watchdog timer should be periodically re-triggered during normal operation, before the timer expires. Expiration of the watchdog timer resets the CPU.

If required, disabling the watchdog timer clock input can disable the watchdog.

Table 30 describes the operation of the watchdog timer.

TABLE 30: WATCHDOG TIMER COMMAND SEQUENCE

#	COMMAND	ADDRESS	BIT	SETTING
1	Enable Watchdog	C200H	3	1= Enable 0= Disable
2	Re-trigger Timer	F800H	all	FFH
3	Disable Watchdog	C200H	3	0

Control Registers Description

Setting the Clock Enable register (C200H), bit 3 to **1** enables the watchdog timer.
Setting the Clock Enable register (C200H), bit 3 to **0** disables the watchdog timer.
Writing **FFH** to address F800H re-triggers the watchdog.

LOW VOLTAGE DETECTOR

The low voltage detector is a supervisory circuit in which the Power Fail Input (V_{det}) is compared to an internal 2.23 V reference (Figure 25). The comparator output goes low when the voltage at V_{det} is less than or equal to 2.23 V and **Bit 1** of register **E400H** equals **0**.

V_{det} is usually driven by an external voltage divider, which senses the unregulated DC input to the system 5V regulator. The voltage divider ratio can be chosen such that the voltage at V_{det} falls below 2.23 V several milliseconds before the +5V supply falls below 4.75V. INT0 is normally used to interrupt the microprocessor so that data can be stored in non-volatile memory before V_{CC} falls below 4.75 V and the RESET output goes low. The Power Fail Comparator output returns to High when Vdet>2.27V.

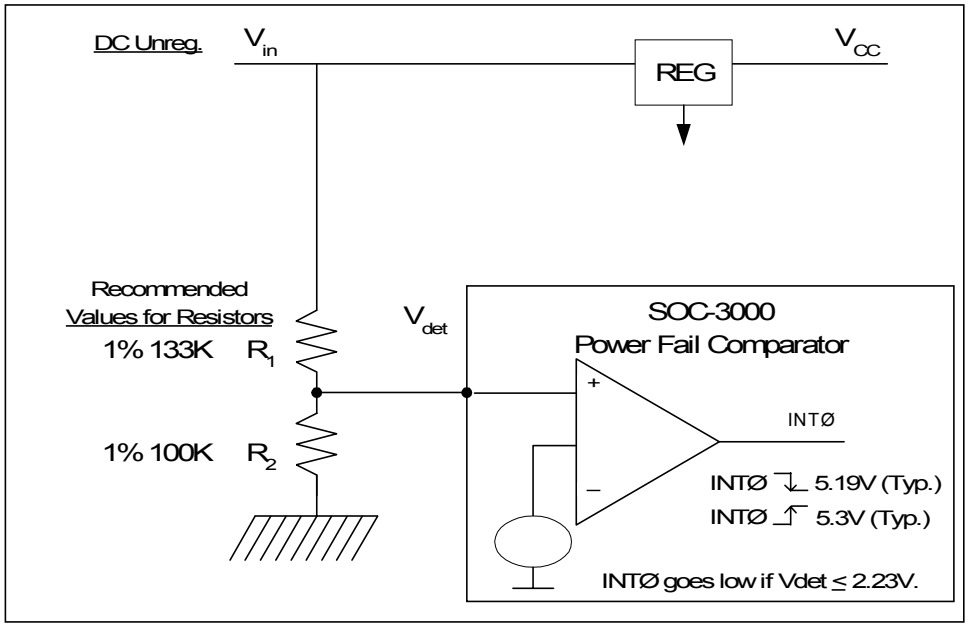

FIGURE 25: LOW VOLTAGE DETECTOR

Interrupt Register

The address of the power-supply interrupt register is **E400H** (Read/Write).

The bit settings at **E400H** that define the power failure interrupt and flag are given in Table 31.

TABLE 31: POWER-FAILURE INTERRUPT REGISTER BIT SETTINGS

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1 POWER FAIL FLAG	BIT 0 (LSB) INTERRUPT ENABLE
E400H	Don't Care						**0** = If $V_{DET} \leq V_{REF}$ **1** = Normal	**0** = Enabled **1** = Disabled

CONFIGURATION REGISTERS (CFR)

Programming the configuration registers (CFR) in the CPU sets the SOC-3000 pin functions. The CFR registers include control and configuration registers that provide the interface between the CPU and the other on-chip peripherals, such as the keyboard, LED and LCD controllers and input/output ports. Each peripheral operates as designated in the CFR registers, where each register may be programmed to perform alternative functions. (See "Examples of Pin Configuration Programming", on page 85).

The complete CFR-register bit assignment for all peripherals and input/output and corresponding PLCC-84 pins are given on the following pages in Table 32.

TABLE 32: CFR BIT ASSIGNMENT

PLCC-84 PIN	REG ADD.	BIT	BIT SETTINGS PER FUNCTION				NOTES
61	C101H	7-6	00=LCD Display S40		10=LED-SI-BLANK	11=OUT 13.3	SI = Serial Interface
60		5-4	00=LCD Display S39		10=LED-SI- STROBE	11=OUT 13.2	
59		3-2	00=LCD Display S38		10=LED-SI- STROBE	11=OUT 13.1	
58		1-0	00=LCD Display S37		10=LED-SI- CLK	11=OUT 13.0	CLK = Clock
57	C102H	7	0=LCD Display S36	1=OUT 12.4			
56		6	0=LCD Display S35	1=OUT 12.3			
55		5-4	00=LCD Display S34		10=OUT 12.2		
54		3-2	00=LCD Display S33		10=OUT 12.1		
53		1-0	00=LCD Display S32		10=OUT 12.0		
52	C103H	7-6	00=LCD Display S31	01=LED Display DIG 7	10=OUT 11.3		DIG = Digit
51		5-4	00=LCD Display S30	01=LED Display DIG 6	10=OUT 11.2		
50		3-2	00=LCD Display S29	01=LED Display DIG 5	10=OUT 11.1		
49		1-0	00=LCD Display S28	01=LED Display DIG 4	10=OUT 11.0		
48	C104H	7-6	00=LCD Display S27	01=LED Display DIG 3	10=OUT 10.0		
47		5-4	00=LCD Display S26	01=LED Display DIG 2			
46		3-2	00=LCD Display S25	01=LED Display DIG 1			SEG = Segment
45		1-0	00=LCD Display S24	01=LED Display SEG DP3			DP = Decimal Point
44	C105H	7-6	00=LCD Display S23	01=LED Display SEG G3			
43		5-4	00=LCD Display S22	01=LED Display SEG F3			
42		3-2	00=LCD Display S21	01=LED Display SEG E3			
41		1-0	00=LCD Display S20	01=LED Display SEG D3			
40	C106H	7-6	00=LCD Display S19	01=LED Display SEG C3			
39		5-4	00=LCD Display S18	01=LED Display SEG B3	10=OUT 9.2		

PLCC-84 PIN	REG ADD.	BIT	BIT SETTINGS PER FUNCTION				NOTES
38		3-2	00=LCD Display S17	01=LED Display SEG A3	10=OUT 9.1		
37		1-0	00=LCD Display S16	01=LED Display SEG DP2	10=OUT 9.0		
36	C107H	7-6	00=LCD Display S15	01=LED Display SEG G2		11=OUT 8.3	
35		5-4	00=LCD Display S14	01=LED Display SEG F2		11=OUT 8.2	
34		3-2	00=LCD Display S13	01=LED Display SEG E2	10=OUT 8.1		
33		1-0	00=LCD Display S12	01=LED Display SEG D2		11=OUT 8.0	
32	C108H	7-6	00=LCD Display S11	01=LED Display SEG C2		11=OUT 7.3	
31		5-4	00=LCD Display S10	01=LED Display SEG B2		11=OUT 7.2	
30		3-2	00=LCD Display S9	01=LED Display SEG A2		11=OUT 7.1	
29		1-0	00=LCD Display S8	01=LED Display SEG DP1		11=OUT 7.0	
28	C109H	7-6	00=LCD Display S7	01=LED Display SEG G1		11=OUT 6.3	
27		5-4	00=LCD Display S6	01=LED Display SEG F1	10=OUT 6.2		
26		3-2	00=LCD Display S5	01=LED Display SEG E1	10=OUT 6.1		
25		1-0	00=LCD Display S4	01=LED Display SEG D1	10=OUT 6.0		
24	C10AH	5-4	00=LCD Display S3	01=LED Display SEG C1	10=OUT 5.2		
23		3-2	00=LCD Display S2	01=LED Display SEG B1	10=OUT 5.1		
22		1-0	00=LCD Display S1	01=LED Display SEG A1	10=OUT 5.0		

PLCC-84 PIN	REG ADD.	BIT	BIT SETTINGS PER FUNCTION				NOTES
21	C10BH	6-5	00=BP4		10=OUT 4.3		BP = Backplane
20		4-3	00=BP3	01=VPP	10=OUT 4.2		
19		2	0=BP2	1=OUT 4.1			
18		1-0	00=BP1		10=OUT 4.0		
-	C10CH	7-0	FFH				Must be always 0xFF
5	C10DH	7	0=I.O 15.7	1=KIN0			KIN = Keyboard In
4		6	0=I.O 15.6	1=KIN1			I.O = Input/Output
3		5	0=I.O 15.5	1=KIN2			
2		4	0=I.O 15.4	1=KIN3			
1		3	0=I.O 15.3	1=KIN4			
84		2	0=I.O 15.2	1=KIN5			
83		1	0=I.O 15.1	1=KIN6			
82		0	0=I.O 15.0	1=KIN7			
81	C10EH	7	0=I.O 14.7	1=KOUT0			KOUT = Keyboard Out
80		6	0=I.O 14.6	1=KOUT1			
79		5	0=I.O 14.5	1=KOUT2			
78		4	0=I.O 14.4	1=KOUT3			
77		3	0=I.O 14.3	1=KOUT4			
76		2	0=I.O 14.2	1=KOUT5			
75		1	0=I.O 14.1	1=KOUT6			
74		0	0=I.O 14.0	1=KOUT7			

SPECIAL FUNCTION REGISTERS (SFR)

The SOC-3000/i includes Special Function Registers (SFR) that enable the device hardware controllers and reset them. Each controller description details its specific SFR operation. This section details all the SFR registers and functions. All these registers are mapped as XDATA memory area.

Global Configuration Register

Register 0C100H is used as a general enable/disable of pin allocation to all the hardware controllers in the SOC-3000/i. Upon power-up or reset this register is cleared, disabling all the hardware controllers. Writing 0xFF to the register activates the allocation of pins to hardware controller, as defined by programming the CFR registers.

TABLE 33: GLOBAL CFR REGISTER

ADDRESS	FUNCTION	REMARKS
C100H	Enable / Disable pin allocation	0x00 – Enable 0xFF - Disable

Operation

1. Upon power-up or reset, the Global CFR register is set, disabling all pin allocation to the hardware controllers.
2. Initialize the CFR registers according to the required hardware configuration as described in section “

Configuration Registers (CFR)" page 61.

3. Initialize the hardware controllers.
4. Enable the Global CFR Register: Write 0x00 to address C100H.

Controllers Clock Enable Register

Register C200H controls the clock source to the hardware controllers in the SOC-3000/i. Each controller operation may be disabled by inhibiting its clock.

TABLE 34: CLOCK ENABLE REGISTER

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
C200H	ADC	0	SLED	0	WDT	KBD	PLED	LCD

TABLE 35: CONTROLLERS CLOCK ENABLE REGISTER BIT FUNCTIONS

BIT	NAME	TYPE	FUNCTION	SETTINGS
0 (LSB)	LCD	Read-Write	Enable LCD display controller clock	0 = Disable 1 = Enable
1	PLED	Read-Write	Enable parallel LED display controller clock	0 = Disable 1 = Enable
2	KBD	Read-Write	Enable keyboard controller clock	0 = Disable 1 = Enable
3	WDT	Read-Write	Enable watch-dog timer clock	0 = Disable 1 = Enable
4	-	Read-Write	None. Set always to 0.	Always 0.
5	SLED	Read-Write	Enables serial LED display controller	0 = Disable 1 = Enable
6	-	Read-Write	None. Set always to 0.	Always 0.
7	AD	Read-Write	Enables ADC controller clock	0 = Disable 1 = Enable

Controllers RESET Registers

The SFRs listed in Table 36 provides the mechanism to reset the hardware controllers of the SOC-3000/i.

TABLE 36: CONTROLLERS RESET REGISTER

ADDRESS	TYPE	FUNCTION	SETTINGS
C400H	Write only	Keyboard controller reset	0xFF = Reset
C401H	Write only	LCD display controller reset	0xFF = Reset
C402H	Write only	Parallel LED display controller reset	0xFF = Reset
C403H	Write only	Serial LED display controller reset	0xFF = Reset
C406H	Write only	ADC controller reset	0xFF = Reset

I/O OPERATION

I/O operation is determined by the configuration registers (CFR) programming. The I/O ports are composed of two groups:

- Byte-Oriented Output Ports –

  Data written to the port is byte oriented (writing **FFH** to the port will set it to HIGH, and writing **00H** to the port will set it to LOW).

- Bit-Oriented Input/Output (I/O) Ports –

  Data written to the port is byte oriented (FFH–to set the port, 00H–to reset the port). Data read from the port is bit-oriented (only the port allocated bit is set/reset).

Table 44, the I/O ports groups, addresses and corresponding PLCC-84 pins are described in Table 37 and Table 38.

TABLE 37: BIT-ORIENTED I/O PORTS ADDRESSES, PIN AND BIT ASSIGNMENT

PLCC-84 PIN	I/O PORT NAME	PORT ADDRESS	BIT ASSIGNMENT (LSB)							
5	I.O 15.7	F22A	0	0	0	0	0	0	0	**x**
4	I.O 15.6	F22B	0	0	0	0	0	0	**x**	0
3	I.O 15.5	F22C	0	0	0	0	0	**x**	0	0
2	I.O 15.4	F22D	0	0	0	0	**x**	0	0	0
1	I.O 15.3	F22E	0	0	0	**x**	0	0	0	0
84	I.O 15.2	F22F	0	0	**x**	0	0	0	0	0
83	I.O 15.1	F230	0	**x**	0	0	0	0	0	0
82	I.O 15.0	F231	**x**	0	0	0	0	0	0	0
81	I.O 14.7	F232	0	0	0	0	0	0	0	**x**
80	I.O 14.6	F233	0	0	0	0	0	0	**x**	0
79	I.O 14.5	F234	0	0	0	0	0	**x**	0	0
78	I.O 14.4	F235	0	0	0	0	**x**	0	0	0
77	I.O 14.3	F236	0	0	0	**x**	0	0	0	0
76	I.O 14.2	F237	0	0	**x**	0	0	0	0	0
75	I.O 14.1	F238	0	**x**	0	0	0	0	0	0
74	I.O 14.0	F239	**x**	0	0	0	0	0	0	0

TABLE 38: BYTE-ORIENTED OUTPUT PORTS ADDRESSES AND PIN ASSIGNMENT

PLCC-84 PIN	I/O FUNCTION	PORT ADDRESS
61	OUT 13.3	F205
60	OUT 13.2	F206
59	OUT 13.1	F207

PLCC-84 PIN	I/O FUNCTION	PORT ADDRESS
58	OUT 13.0	F208
57	OUT 12.4	F209
56	OUT 12.3	F20A
55	OUT 12.2	F20B
54	OUT 12.1	F20C
53	OUT 12.0	F20D
52	OUT 11.3	F20E
51	OUT 11.2	F20F
50	OUT 11.1	F210
49	OUT 11.0	F211
48	OUT 10.0	F212
39	OUT 9.2	F213
38	OUT 9.1	F214
37	OUT 9.0	F215
36	OUT 8.3	F216
35	OUT 8.2	F217
34	OUT 8.1	F218
33	OUT 8.0	F219
32	OUT 7.3	F21A
31	OUT 7.2	F21B
30	OUT 7.1	F21C
29	OUT 7.0	F21D
28	OUT 6.3	F21E
27	OUT 6.2	F21F
26	OUT 6.1	F220
25	OUT 6.0	F221
24	OUT 5.2	F222
23	OUT 5.1	F223
22	OUT 5.0	F224
21	OUT 4.3	F225
20	OUT 4.2	F226
19	OUT 4.1	F227
18	OUT 4.0	F228

8051-COMPATIBLE ON-CHIP PERIPHERALS

This section describes the standard 8051 peripheral devices available to the user. These functions are fully compatible with the standard 8051 CPUs and are controlled via the standard 8051 Special Function Registers (SFRs).

Parallel I/O Ports

Some of the parallel I/O ports of the 80C51TBO core are available on the SOC-3000 pins.

Most of the ports are already allocated to specific functions. However, the application design may require allocating different functions to these pins. Table 39 list the available pins, 80C51 I/O port, default function and special precaution needed when changing the function of the pin.

TABLE 39: AVAILABLE PINS ON THE 80C51 I/O PORT

PIN #	80C51 PORT	DEFAULT FUNCTION	SPECIAL PRECAUTIONS
7	P1.7	Buzzer	After power-up the SOC-3000 asserts 3 pulses on this pin
8	P1.5	None	
9	P1.4	None	
14	P3.4 / Timer 0	None	Used in CybraTech application for power-off control in low-power applications
15	P3.5 / Timer 1	None	Used in CybraTech application for detecting power source (AC/Battery)
16	P1.6	None	Used in CybraTech application to control LCD electro-luminescent backlight operation

The I/O ports are controlled and accessible using the 80C51TBO Special Function Registers as described in its device specification.

Timers/Counters

The 80C51 Timers/Counters external inputs are available for use on SOC-3000 pin #14 (Timer 0) and pin #15 (Timer 1). Using the timers is via the 80C51 Special Function Registers (SFRs) as described in the 80C51TBO specification.

SOC-3000 INITIALIZATION

At power-up or after RESET the SOC-3000 performs the following procedures:

- Disabling all the peripheral controllers of the ASIC.
- Setting the CFR and control registers to their default values.
- Start the boot program (ROM mask in the chip) that checks if the chip is programmed or not. If the chip is programmed it starts running the program starting at address **1000H**. Otherwise, it toggles the buzzer signal (pin 7) HIGH/LOW three times to signal that the chip is erased and waits for software download via the serial communication port.

To initialize the SOC-3000:

1. Program the SOC-3000 pin configuration in the CFR registers.
   - For general pin configuration for an LCD display, refer to Table 1, page 9. For a quick reference, refer to Table 4, page 18.
   - For general pin configuration for a LED display, refer to Table 2, page 12. For a quick reference, refer to Table 5, page 19.
   - For CFR bit assignment, refer to Table 32, page 62.

   For examples of CFR bit assignment, refer to "Example of Pin Configuration Programming", on page 85.
2. Initialize the peripheral controllers used by the application.
3. Write 0x00 to the global CFR register at address **C100H**.
   This activates all CFR registers and completes SOC-3000 initialization.

SOC-3000 HARDWARE DESIGN CONSIDERATIONS AND PERIPHERAL INTERFACE CONNECTIONS

Load Cell Interface

The SOC-3000 supports a wide range of load-cell connection configurations, each based on various combinations of the following connection options:

- 4-wire or 6-wire interface
- Up to eight load cells connected in parallel
- Load cell impedance range of 350 to 1000 ohms

Individually and in combination, these connection options enable the SOC-3000 to function on a wide range of application platforms, each having different power consumption and system configuration requirements, while using the same electronic hardware.

4-Wire and 6-Wire Interfaces

The SOC-3000 interface to the load cell carries the following electrical signals:

- SIG + (Signal Input +)
- SIG – (Signal Input –)
- SEN + (Excitation voltage / Sense input +)
- SEN – (Excitation voltage / Sense input –)

A typical 4-wire load-cell connection, in which the distance between the load cells and the SOC-3000 chip is small, as in a standard retail scale, is shown in Figure 26.

However, in platforms requiring long wires between the load cell and the electronic hardware, such as weighing bridges, the voltage drop over the cables is significant and affects accuracy.

The 6-wire interface eliminates this error factor by using the sense wires, as shown in Figure 27. The sense wires serve as a reference for the ADC converter, thus eliminating the voltage drop over the long excitation-voltage wires.

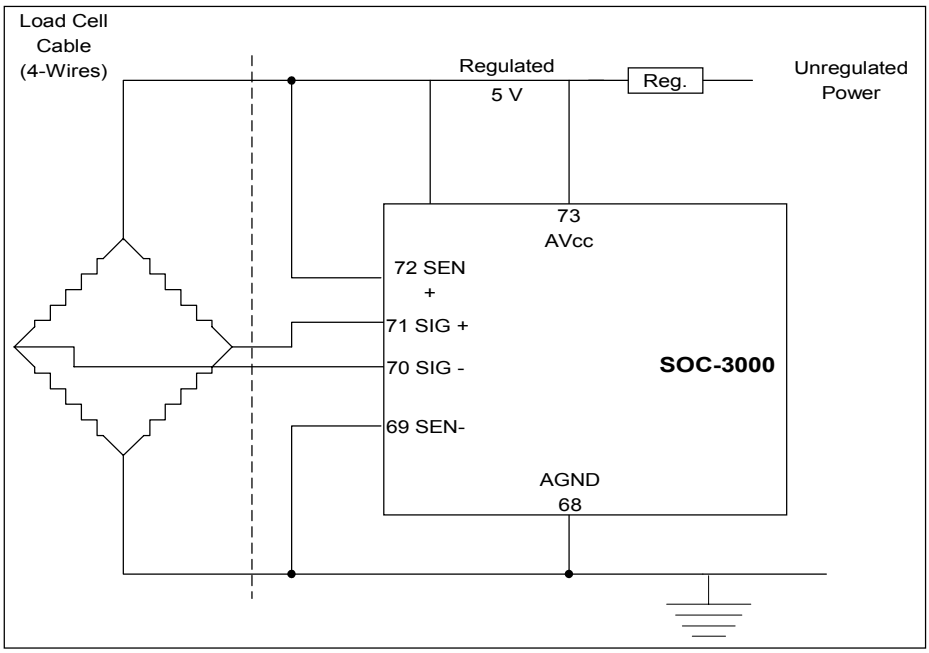

FIGURE 26: 4-WIRE LOAD-CELL CONNECTION

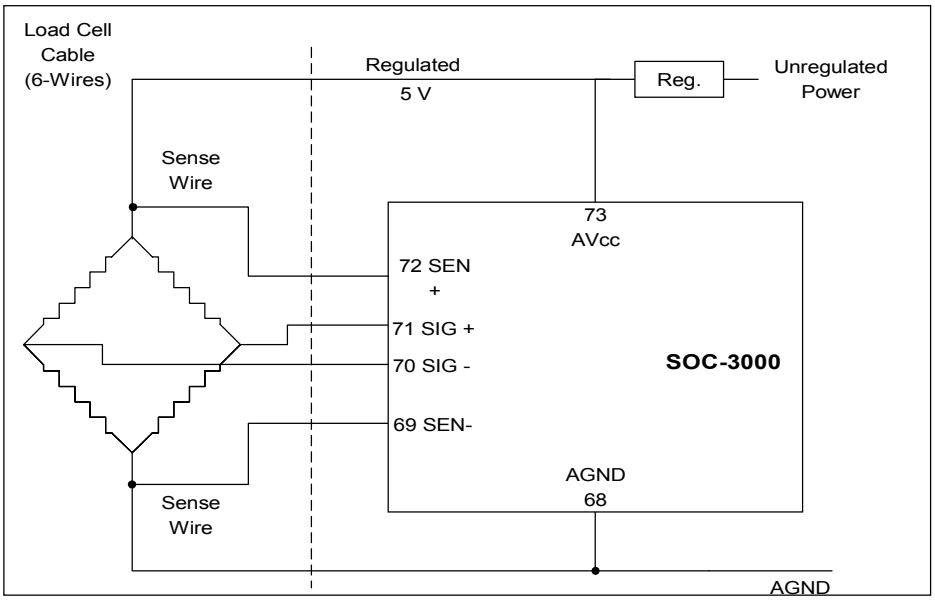

FIGURE 27: 6-WIRE LOAD-CELL CONNECTION

Load Cells Connected in Parallel

The SOC-3000 may be connected to up to eight load cells connected in parallel. Multiple load cells are required in heavy load applications, such as weigh bridges, that require from two to eight load cells.

Load cells connected in parallel typically result in lower output impedance, which decreases in direct proportion to the number of load cells. This results in a higher excitation current and higher sensitivity to factors that throw load cells out of balance.

The SOC-3000 eliminates this problem with its high Common Mode Rejection Ratio (CMRR), which allows the connection of a large number of load cells (up to eight) without losing measurement accuracy. The multiple load-cell connection is shown in Figure 28.

IMPORTANT

The load cells should be matched before connecting them to the SOC-3000 to ensure the same initial offset, span and impedance. This will eliminate error factors that are beyond the control of SOC-3000 electronics.

NOTE

These large weighing platforms may also require a 6-wire interface connection, as described above, on page 75.

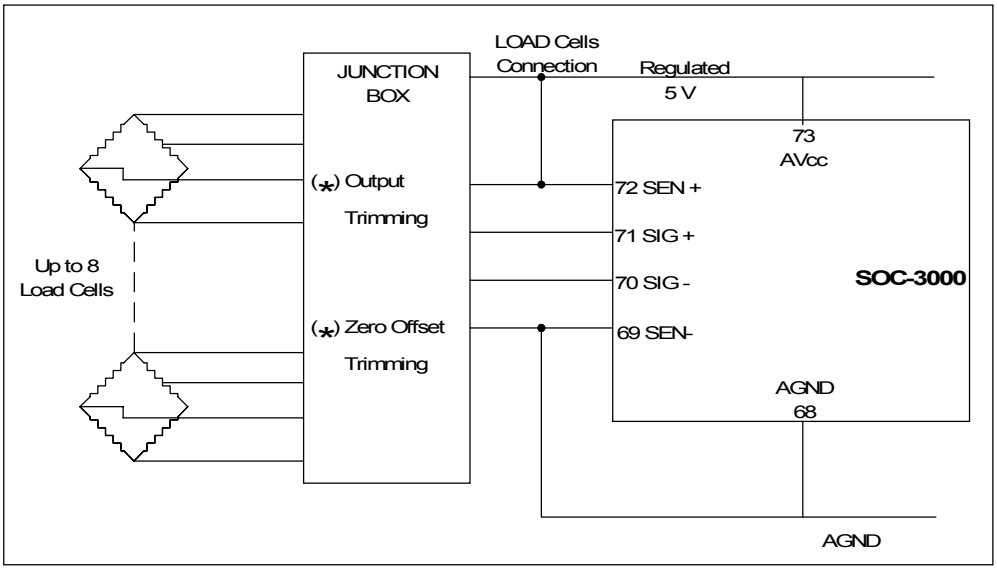

FIGURE 28: MULTIPLE LOAD-CELL CONNECTION

Load Cell Impedance

Most load cells have output impedance of 350 ohms. However, in power-restricted applications, load cells of higher impedance, typically a 1000-ohm bridge, are used to reduce the cell's power consumption.

The SOC-3000 CMRR minimizes the error resulting from this high bridge impedance and ensures full and accurate performance under this limiting condition.

The result is economical power consumption without sacrificing weighing accuracy.

Keyboard Interface

The SOC-3000 supports direct connection of a keyboard of up to 64 keys arranged in an 8 × 8 matrix. The hardware interface with an example of a scale keyboard is shown in Figure 29.

The keyboard controller ("Keyboard Controller", page 31) automatically scans the matrix by asserting a high signal on the output lines (KOUT 0 to 7) and reading the input lines (KIN 0 to 7). The key hardware code, which is the code returned by the keyboard controller when the key is pressed, is shown in Figure 12, page 31.

The keyboard controller has a programmable anti-bounce mechanism, in which different delays can be programmed to avoid erroneous key activation due to bouncing of the keys. The delay can be set to a discrete value from 4 to 18 milliseconds, in two-millisecond increments. For programming the anti-bounce mechanism, see Table 14, page 32.

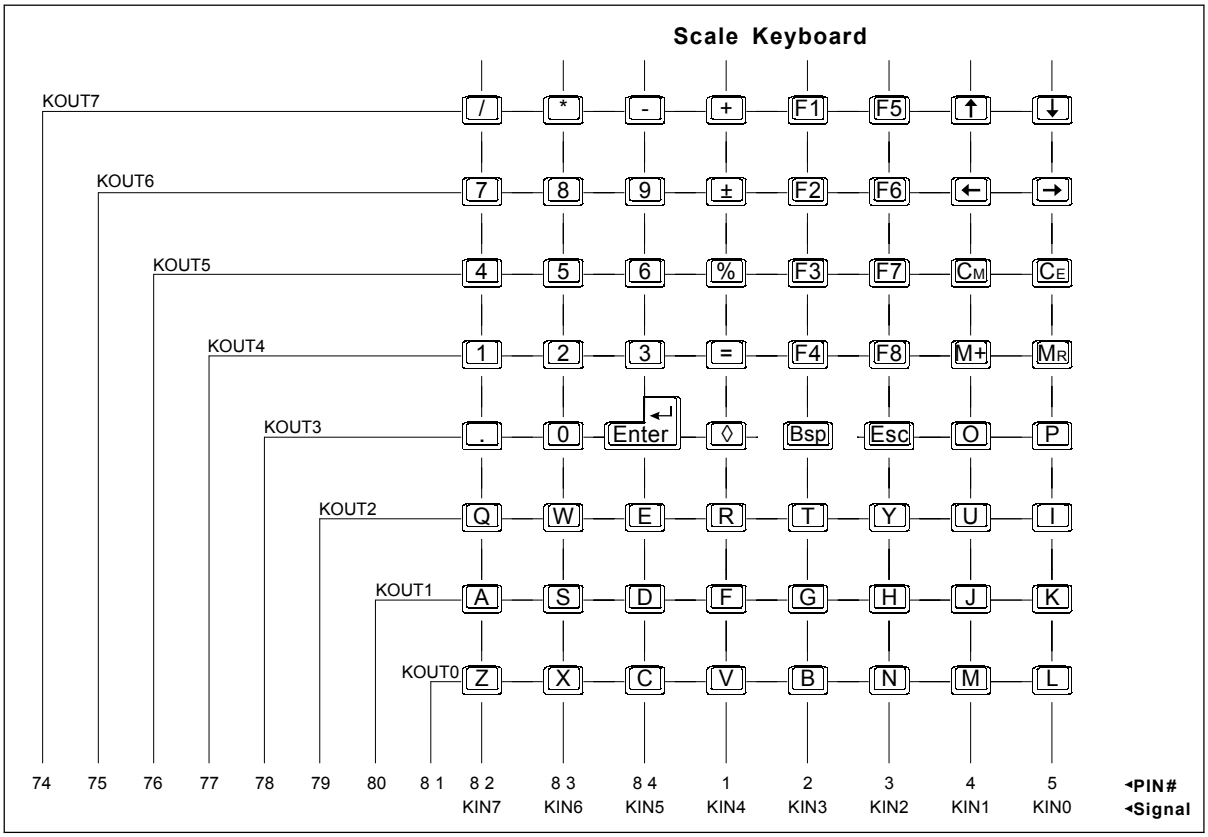

FIGURE 29: KEYBOARD INTERFACE

LCD Display Interface

The SOC-3000 interface supports LCD displays as follows:

- Up to four backplanes, each driving 40 LCD segments
- Static, 1/2-bias and 1/3-bias display options
- Electro-luminescent (EL) lighting control

The hardware interface is shown in Figure 30.

The SOC-3000 is equipped with bias generators with voltage-followers buffers that generate the LCD bias voltages and backplane multiplexing signals. Thus, LCD displays can be directly connected to the SOC-3000 without any external component.

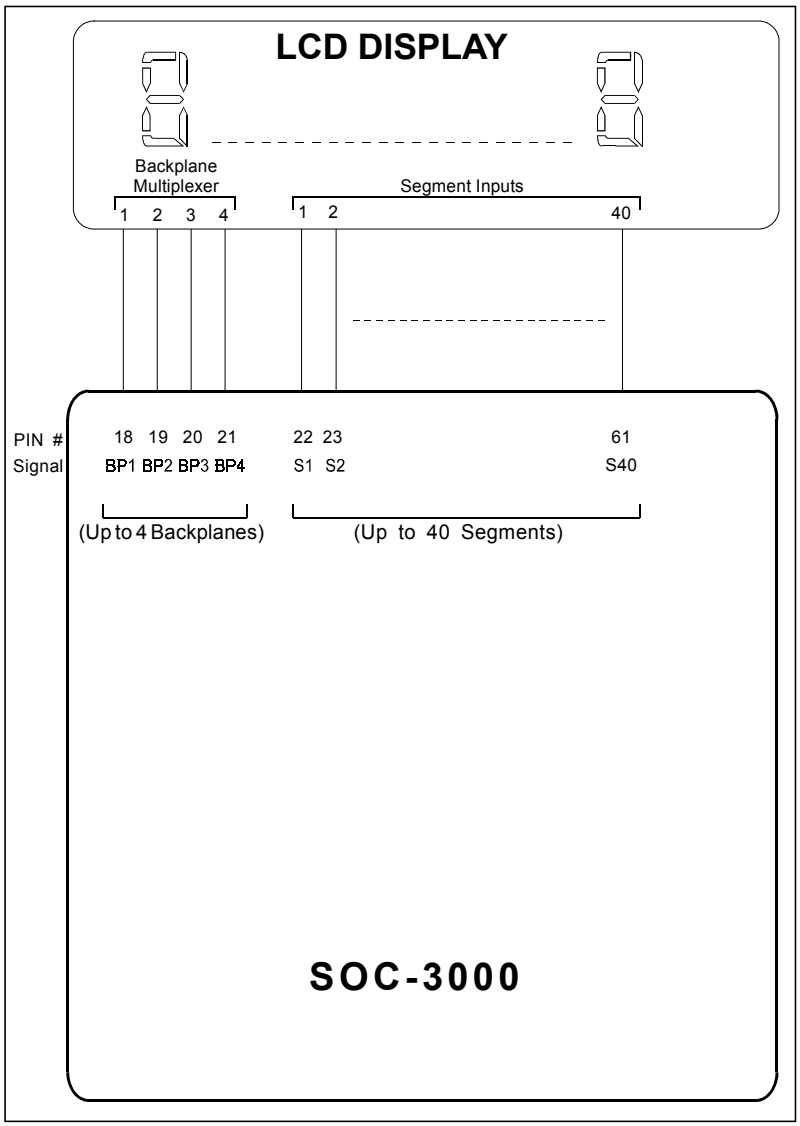

FIGURE 30: LCD DISPLAY INTERFACE

LED Display Interface

The SOC-3000 interface supports LED displays as follows:

- Up to 21 digits each comprising eight segments–seven-segment digit plus Decimal Point (DP)
- Three digit groups, **Weight**, **Price,** and **Total**
- Automatic hardware refresh mechanism to reduce power consumption

The hardware interface is shown in Figure 31.

The LED display is directly connected to the SOC-3000 with the addition of only the LED display drivers.

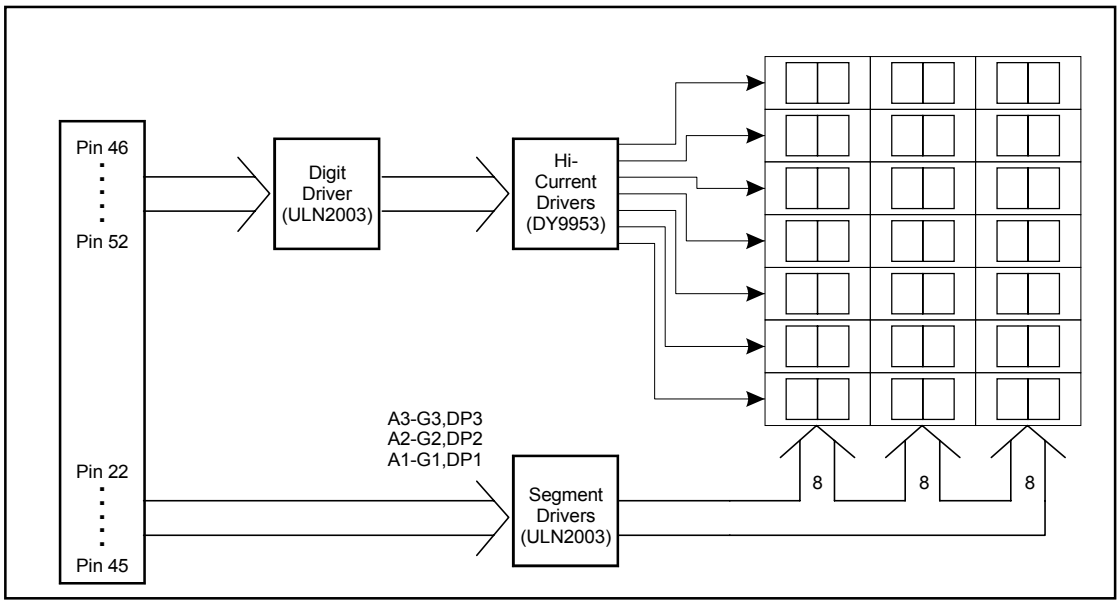

FIGURE 31: LED PARALLEL DISPLAY INTERFACE

External Interrupt Sources

External interrupt sources may be connected to the SOC-3000 using the following pins:

a. Vdet / INT0~.
b. P3.4 / Timer-counter 0 input.
c. P3.5 / Timer-counter 1 input.

Using the Vdet input:

The Vdet input is connected to INT0 of the 80C51TBO core. In battery-operated equipment this input is connected to the battery voltage divider and used to detect low battery voltage.

Other interrupt sources may be connected to this input using open-collector drivers operating in negative logic mode ('0' is active interrupt). A low voltage input triggers the INT0. The application software applies a mechanism to determine whether the interrupt was generated by low battery voltage or by other interrupt source.

Using Timer0 and Timer1 inputs:

SOC-3000 pin #14 is connected to the 80C51 Timer 0 input and pin #15 is connected to Timer1 input.

These inputs may be used for counting or timer operations, or as additional interrupt inputs to the device.

Using these inputs as interrupt inputs requires that the appropriate timer be set to 0xFE. The next event causes the counter to increase to 0xFF and triggers the Timer 0 (or timer 1) interrupt.

I^2C-Compatible Interface

The SOC-3000 may supports a 2-wire I^2C compatible serial interface. The I^2C-compatible interface shares its pins with the CPU I/O pins (P1.4, P1.5) and is implemented in software. Table 40 provides the hardware interface information:

TABLE 40: I^2C-COMPATIBLE INTERFACE HARDWARE INTERFACE

PIN#	NAME	DESCRIPTION
8	SDATA	Serial Data I/O pin
9	SCLOCK	Serial Clock pin

Power Saving Schemes

SOC-3000/i provides several means for power saving for battery-operated systems:

a. Set the CPU to IDLE or POWERDOWN operating modes – see detailed description in the M8051TBO Technical Specification, Power Management section.

b. Disable unused hardware controllers – by disabling the controller clock via the "Controllers Clock Enable Register (C200H)", see tables 33 and 34.

c. Reduce the CPU frequency to minimum while idle by using the Frequency Controller. The CPU frequency may be increased on the fly to 16MHz when an interrupt or an event occurred.

d. Switch the power to the load cell using the I/O pins of the SOC and an external switch.

Grounding and Board Layout Recommendations

As with all high-resolution data converters, special attention must be paid to grounding and to the PCB layout of SOC-3000 based designs in order to achieve optimum performance from the Analog-To-Digital Converter.

Four-layer boards are recommended where the outer layers are ground layers covering the whole surface, and the inner layers are used for routing the signal lines. The same ground plane should be used for both the digital and analog grounds.

Keep all ground connection as short as possible. Make sure that the return paths of the signals are as close as possible to the paths that the currents took to reach their destinations.

Avoid digital signals flowing under the analog components area.

Wherever possible, avoid large discontinuities in the ground plane, since they force the return signals to travel on a longer path. An example of correct implementation is routing all signals through the inner layers and keeping the outer layers for ground.

If you plans to connect fast logic signals (rise/fall time < 5ns) to any of the SOC-3000 digital inputs, add a series resistor to each relevant line in order to keep rise and fall times longer than 5ns at the SOC-3000 input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high-speed signals from capacitive coupling into the SOC-3000 and affecting the accuracy of the ADC.

IN-CIRCUIT EMULATOR (ICE) SYSTEM

The In-Circuit Emulator (ICE-3000) system provides full emulation of the SOC-3000 device. It includes a plug-in pod that replaces the SOC-3000 device thus enabling full emulation of the device in the target board. It emulates the SOC-3000 device in real-time simplifying the hardware-software integration process.

The ICE-3000 is composed of 3 elements:

a. DS-51 emulator.

b. SOC-3000 Personality Probe.

c. Windows-based software debugger.

The system enables you to access all SOC-3000 device registers and memory locations and debug the application using free run or breakpoints and single step execution control.

EXAMPLES OF PIN CONFIGURATION PROGRAMMING

The following pages show examples of pin configuration programming, as follows:

- Example 1 shows a 20-digit LCD display and an 8×8 keyboard.
- Example 2 shows a 16-digit LCD display, an 8×4 keyboard, 8 output ports and 4 I/O ports.
- Example 3 shows a 21-digit LED Parallel display, an 8×8 keyboard and 13 output ports.
- Example 4 shows the pin programming for all output and I/O ports.

Example 1: Configuring a 20-digit LCD Display and an 8x8 Keyboard

- 20-digit LCD display support implies allocation of the whole LCD driver output pins to the LCD display, using 4 backplanes and 40 segments. Thus, pins 18-61 should be assigned to the LCD controller/driver.
- 8x8 keyboard support implies allocation of the whole keyboard I/O pins to the keyboard controller. Thus, pins 1-5 and 74-84 should be assigned to the keyboard controller.

Table 41 lists the CFR registers affected and their required values.

TABLE 41: EXAMPLE 1: 20-DIGIT LCD DISPLAY, 8×8 KEYBOARD

FUNCTION	CFR REGISTER ADDRESS & VALUE	PORT / SEGMENT	AFFECTED PINS
LCD Display	C101H = 00H	S37 – S40	58 – 61
	C102H = 00H	S32 – S36	53 – 57
	C103H = 00H	S28 – S31	49 – 52
	C104H = 00H	S24 – S27	45 – 48
	C105H = 00H	S20 – S23	41 – 44
	C106H = 00H	S16 – S19	37 – 40
	C107H = 00H	S12 – S15	33 – 36
	C108H = 00H	S8 – S11	29 – 32
	C109H = 00H	S4 – S7	25 – 28
	C10AH = 00H	S1 – S3	22 – 24
	C10BH = 00H	BP1 – BP4	18 – 21
Keyboard Matrix	C10DH = FFH	KIN0 – KIN7	1 – 5; 82 – 84
	C10EH = FFH	KOUT0 – KOUT7	74 – 81

Example 2: Configuring a 16-digit LCD Display, an 8x4 Keyboard, 8 Output and 4 I/O Ports

- 16-digit LCD display support implies partial allocation of the LCD driver output pins to the LCD display, using 4 backplanes and 32 segments. Thus, pins 18-52 should be assigned to the LCD controller/driver.
- 8x4 keyboard support implies partial allocation of the keyboard I/O pins to the keyboard controller. Thus, pins 1-5 and 78-84 should be assigned to the keyboard controller.
- 8 output ports will be implemented using the 8 pins of the LCD driver that are not used for the display. Thus, pins 53-61 should be assigned as Output ports.
- 4 I/O ports will be implemented using the 4 pins of the keyboard input matrix that are not used by the keyboard. Thus, pins 74-77 should be assigned as I/O ports.

Table 42 lists the CFR registers affected and their required values.

TABLE 42: EXAMPLE 2: 16-DIGIT LCD DISPLAY, 8×4 KEYBOARD, 8 OUTPUT, 4 I/O

FUNCTION	CFR REGISTER ADDRESS & VALUE	PORT / SEGMENT	AFFECTED PINS
LCD Display	C102H = E8H	S32	53
	C103H = 00H	S28 – S31	49 – 52
	C104H = 00H	S24 – S27	45 – 48
	C105H = 00H	S20 – S23	41 – 44
	C106H = 00H	S16 – S19	37 – 40
	C107H = 00H	S12 – S15	33 – 36
	C108H = 00H	S8 – S11	29 – 32
	C109H = 00H	S4 – S7	25 – 28
	C10AH = 00H	S1 – S3	22 – 24
	C10BH = 00H	BP1 – BP4	18 – 21
Keyboard Matrix	C10DH = FFH	KIN0 – KIN7	1 – 5; 82 – 84
	C10EH = F0H	KOUT4 – KOUT7	78 – 81
Output Ports	C101H = FFH	P13.0 – P13.3	58 –61
	C102H = E8H	P12.1 – P12.4	54 – 57
I/O Ports	C10E = F0H	KOUT4 – KOUT7	78 – 81
		P14.0 – P14.3	74 – 77

Example 3: Configuring a 21-digit LED Parallel Display, an 8x8 Keyboard and 13 Output Ports

- 21-digit LED parallel display support implies full allocation of the LED parallel display controller output pins to the LED parallel display. Thus, pins 22-52 should be assigned to the LED parallel display controller.
- 8x8 keyboard support implies full allocation of the keyboard I/O pins to the keyboard controller. Thus, pins 1-5 and 74-84 should be assigned to the keyboard controller.
- 13 output ports will be implemented using the available OUTPUT ports available in the ASIC. Thus, pins 53-61 should be assigned as Output ports.

Table 43 lists the CFR registers affected and their required values.

TABLE 43: EXAMPLE 3: 21-DIGIT LED DISPLAY, 8×8 KEYBOARD, 13 OUTPUT

FUNCTION	CFR REGISTER ADDRESS & VALUE	PORT / SEGMENT	AFFECTED PINS
LED Display	C103H = 55H	DIG4 – 7	49 – 52
	C104H = 55H	SEG DP3; DIG1 - 3	45 – 48
	C105H = 55H	SEG D3 – G3	41 – 44
	C106H = 55H	SEG DP2; A3 – C3	37 – 40
	C107H = 55H	SEG D2 – G2	33 – 36
	C108H = 55H	SEG DP1; A2 – C2	29 – 32
	C109H = 55H	SEG D1 – G1	25 – 28
	C10AH = 15H	SEG A1 – C1	22 – 24
Keyboard Matrix	C10DH = FFH	KIN0 – KIN7	1 – 5; 82 – 84
	C10EH = FFH	KOUT0 – KOUT7	74 – 81
Output Ports	C101H = FFH	P13.0 – P13.3	58 –61
	C102H = EAH	P12.0 – P12.4	53 – 57
	C10BH = 56H	P4.0 – P4.3	18 – 21

Example 4: Outputs and I/O Ports Programming

- Output ports support implies full allocation of the LCD display controller output pins to the OUTPUT function. Thus, pins 18-61 should be assigned to the OUTPUT controller.
- I/O ports support implies full assignment of the Keyboard controller pins to the I/O ports. Thus, pins 1 – 5 and 74 – 84 should be assigned to the I/O controller.

TABLE 44: OUTPUT AND I/O PORTS PROGRAMMING

FUNCTION	CFR REGISTER ADDRESS & VALUE	PORT / SEGMENT	AFFECTED PINS
OUTPUT ports	C101H = FFH	P13.0 – P13.4	58 – 61
	C102H = EAH	P12.0 – P12.4	53 - 57
	C103H = AAH	P11.0 – P11.3	49 – 52
	C104H = 80H	P10.0	48
	C106H = 2AH	P9.0 – P9.2	37 – 39
	C107H = FCH	P8.0 – P8.3	33 – 36
	C108H = FFH	P7.0 – P7.3	29 – 32
	C109H = EAH	P6.0 – P6.3	25 – 28
	C10AH = 2AH	P5.0 – P5.2	22 – 24
	C10BH = 56H	P4.0 – P4.3	18 - 21
I/O Ports	C10DH = 00H	P15.0 – P15.7	1 – 5; 82 - 84
	C10EH = 00H	P14.0 – P14.7	74 - 81

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