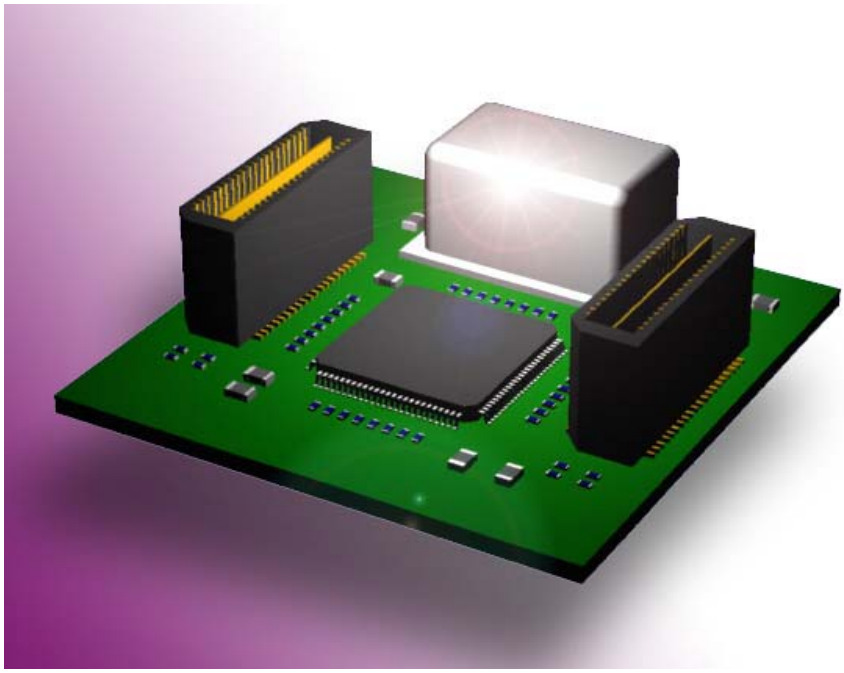
STS-100 Synchronous Timing Module

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com



Features

- Suitable for Stratum 3 and 4 SONET or SDH Equipment Clocks (SEC) applications
- Supports 14 individual inputs (LVDS, LVPECL, TTL) at Nx8 kHz multiples up to 155.52 MHz
- 11 output reference clocks: 7xSEC(1.544MHz, 2.048MHz, 6.48 to 155.52MHz), 1BITS(1.544MHZ, 2.048MHZ), 64kHz/8kHz composite clock, 8 kHz frame sync, 2 kHz multi-frame sync.
- Supports Free Run, Lock and Hold Over modes of operation.
- Robust monitoring on all input clock sources
- Automatic “hitless” switchover on loss of input.
- Phase build-out for output clock phase continuity during input switch over or mode transitions.
- Supports Microprocessor interface – Intel, Motorola, Multiplexed, Serial and EEPROM
- Programmable wander/jitter tracking/attenuation 0.1Hz to 20Hz
- Supports master/Slave configuration and hot/standby redundancy.
- 3.3V Operation
- Meets Telcordia specifications
- ROHS-5 Compliant

RoHS-5/6 COMPLIANT

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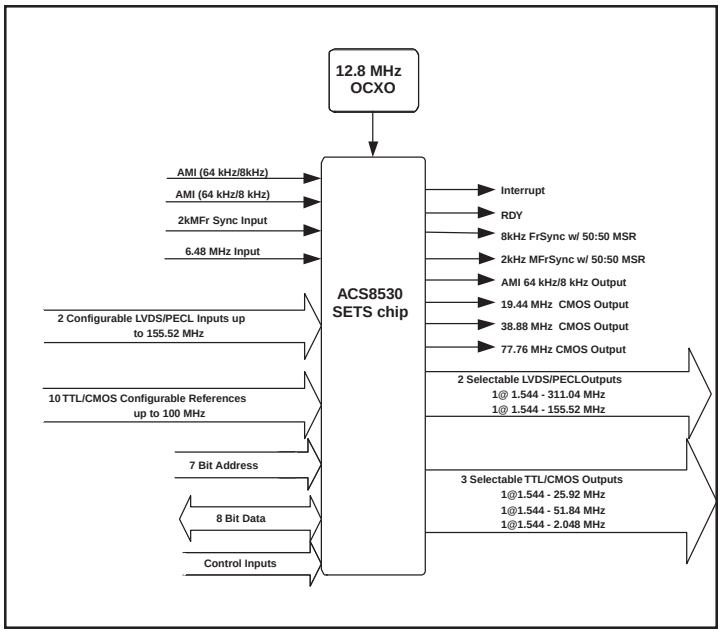
Application

The STS-100 module provides Synchronous Equipment Timing Source (SETS) function in a SONET/SDH network element. It generates SONET/SDH equipment clocks (SEC) and frame synchronization clocks. The module supports Free run, Locked and Holdover modes of operations. The module supports 14 input clocks and generates 11 different outputs. The module also supports master/slave configuration, which provides protection against single STS-100 failure. This module is incorporated with a microprocessor port, which provides access to the internal registers.

The STS-100 module is a platform that is designed to support easy installation and upgrade paths of the ACS8530 SETS chip from Semtech. For timing diagrams and additional details, please refer to the ACS8530 data sheet. For register assignments, please refer to the ACS8530 data sheet.

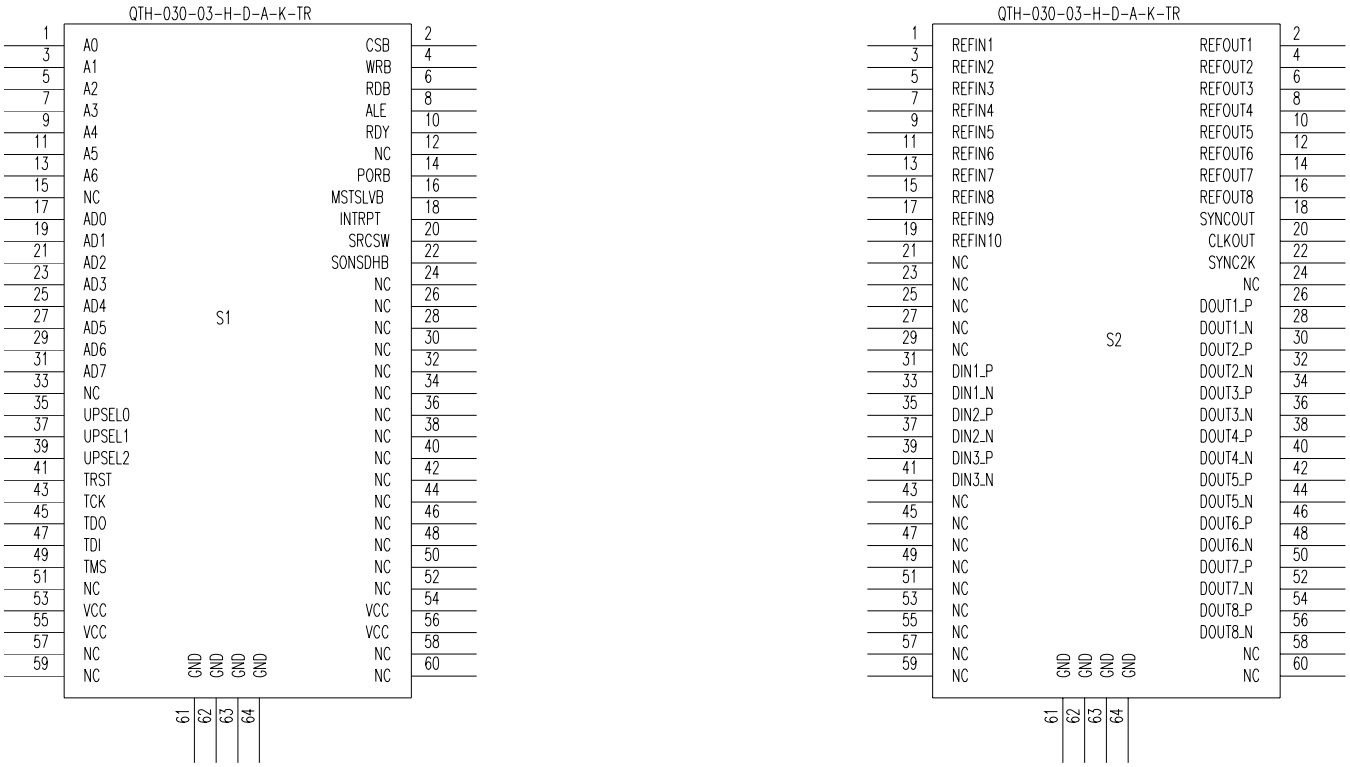
This product is ROHS-5 compliant. ROHS-5 indicates that this product is ROHS compliant except for lead from those manufacturers wishing to take the lead exemption.

Functional Block Diagram



Pin Outs

Figure 2



Two QTH-030-03-H-D-A-K-TR connectors from SAMTEC® are used on the STS-100 Module. The mating Part# is QSH-030-01-H-D-A-K-TR.

Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5		3.6	Volts	
V_I	Input Voltage			3.6	Volts	
V_O	Output Voltage			3.6	Volts	
T_s	Storage Temperature	-40		85	°C	

Recommended Operating Conditions

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.0	3.3	3.6	Volts	
I_{IN}	Power Supply Current (Power-up) (Typical)		650 450	750 550	mA mA	
T_{OP}	Operating Temperature	0		70	°C	
V_{IH}	High level input voltage - TTL/CMOS	Refer to Semtech's data sheet for ACS8530 SETS				
V_{IL}	Low level input voltage - TTL/CMOS	Refer to Semtech's data sheet for ACS8530 SETS				
V_{IH}	High level input voltage - AMI	Refer to Semtech's data sheet for ACS8530 SETS				
V_{IL}	Low level input voltage - AMI	Refer to Semtech's data sheet for ACS8530 SETS				
V_{IH}	High level input voltage - LVPECL/LVDS	Refer to Semtech's data sheet for ACS8530 SETS				
V_{IL}	Low level input voltage - LVPECL/LVDS	Refer to Semtech's data sheet for ACS8530 SETS				

DC Characteristics - Outputs

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{OH}	High level output voltage, TTL/CMOS	Refer to Semtech's data sheet for ACS8530 SETS				
V_{OL}	Low level output voltage, TTL/CMOS	Refer to Semtech's data sheet for ACS8530 SETS				
V_{OH}	High level output voltage, AMI	Refer to Semtech's data sheet for ACS8530 SETS				
V_{OL}	Low level output voltage, AMI	Refer to Semtech's data sheet for ACS8530 SETS				
V_{OH}	High level output voltage, LVPECL/LVDS	Refer to Semtech's data sheet for ACS8530 SETS				
V_{OL}	Low level output voltage, LVPECL/LVDS	Refer to Semtech's data sheet for ACS8530 SETS				

Specifications

Table 4

Parameter	Specifications	Notes
Input Frequency Range	2kHz,8kHz,64kHz,1.544MHz, 2.048MHz, 6.48MHz-155.52MHz	
Output Frequency Range	2kHz,8kHz,64kHz,1.544MHz, 2.048MHz, 6.48MHz-311.04MHz	
Timing Reference Inputs	GR-1244-CORE 3.2.1	
Jitter, Wander and Phase Transient Tolerances	GR-1244-CORE 4.2-4.4, GR-253-CORE 5.4.4.3.6	
Wander Generation	GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	
Wander Transfer	GR-1244-CORE 5.4	
Jitter Generation	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3	
Jitter Transfer	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1	
Phase Transients	GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3	
Free Run Accuracy	±4.6 ppm	
Pull-in/ Hold-in Range	±17 ppm from Free Run frequency	

Connector S1
Table 5

PIN	SYMBOL	I/O	DESCRIPTION
1,3,5,7, 9,11,13	A[0:6]	I	Address bus for microprocessor interface, A[0} is SDI in serial interface mode
2	CSB	I	Chip Select (Active Low)
4	WRB	I	Write (Active Low)
6	RDB	I	Read (Active Low)
8	ALE	I	Address latch enable. This pin acts as SCLK in serial mode.
10	RDY	O	Ready/Data acknowledge
14	PORB	I	Power on Reset (Active Low)
17,19,21 23,25,27 29,31	AD[0:7]		Address/Data multiplexed address/data depending on microprocessor mode selection. AD[0] is SDO in serial mode
16	MSTSLVB	I	Master/Slave select. Sets initial power up state
18	INTRPT	O	Active high software interrupt
20	SRCSW	I	Source switching. Force fast source switching.
22	SONSDHB	I	SONET/SDH frequency select. Sets initial power up state
35, 37, 39	UPSEL[0:2]	I	Configures the input for a particular microprocessor type.
41	TRST	I	Tri-State input
43	TCK	I	JTAG TCK input
45	TDO	O	JTAG TDO output
47	TDI	I	JTAG TDI input
49	TMS	I	JTAG TMS output
53, 54, 55, 56	Vcc		3.3V Input
61, 62, 63, 64	GND		Ground
12, 15, 24, 26, 28, 30, 32, 33, 34, 36, 38, 40, 42, 44, 46, 48, 50, 51, 52, 57, 58, 59, 60	NC		No Connect

Connector S2
Table 6

PIN	SYMBOL	I/O	IO Type	DESCRIPTION	
1	REFIN1	I	TTL/CMOS	Input Reference	(I3 input on ACS8530 SETS)
2	REFOUT1	O	TTL/CMOS	Output Reference	(TO1 output on ACS8530 SETS)
3	REFIN2	I	TTL/CMOS	Input Reference	(I4 input on ACS8530 SETS)
4	REFOUT2	O	TTL/CMOS	Output Reference	(TO2 output on ACS8530 SETS)
5	REFIN3	I	TTL/CMOS	Input Reference	(I7 input on ACS8530 SETS)
6	REFOUT3	O	TTL/CMOS	Output Reference	(TO3 output on ACS8530 SETS)
7	REFIN4	I	TTL/CMOS	Input Reference	(I8 input on ACS8530 SETS)
8	REFOUT4	O	TTL/CMOS	Output Reference	(TO4 output on ACS8530 SETS)
9	REFIN5	I	TTL/CMOS	Input Reference	(I9 input on ACS8530 SETS)
10	REFOUT5	O	TTL/CMOS	Output Reference	(TO5 output on ACS8530 SETS)
11	REFIN6	I	TTL/CMOS	Input Reference	(I10 input on ACS8530 SETS)
12	REFOUT6	O	TTL/CMOS	Output Reference	(TO9 output on ACS8530 SETS)
13	REFIN7	I	TTL/CMOS	Input Reference	(I11 input on ACS8530 SETS)
14	REFOUT7	O	TTL/CMOS	8 kHZ Frame SYNC output	
15	REFIN8	I	TTL/CMOS	Input Reference	(I13 input on ACS8530 SETS)
16	REFOUT8	O	TTL/CMOS	2 kHz Multi-Frame SYNC output	
17	REFIN9	I	TTL/CMOS	Input Reference	(I14 input on ACS8530 SETS)
18	SYNCOUT	0	TTL/CMOS	No Connect	
19	REFIN10	I	TTL/CMOS	Input Reference	
20	CLKOUT	O	TTL/CMOS	Onboard oscillator output	
22	SYNC2K	I	TTL/CMOS	Sychronized to a 2 kHz multi-frame signal from partner STS-100A in a rededundancy system	
26	DOUT1_P	O	AMI	AMI Output	
28	DOUT1_N	O	AMI	AMI Output	
30	DOUT2_P	O	LVPECL/LVDS	Differential Output	(TO6 pins on ACS8530 SETS)
32	DOUT2_N	O	LVPECL/LVDS	Differential Ouput	(TO6 pins on ACS8530 SETS)
34	DOUT3_P	O	LVPECL/LVDS	Differential Ouput	(TO7 pins on ACS8530 SETS)
36	DOUT3_N	O	LVPECL/LVDS	Differential Ouput	(TO7 pins on ACS8530 SETS)
38	DOUT4_P			No Connect	
40	DOUT4_N			No Connect	
42	DOUT5_P			No Connect	
44	DOUT5_N			No Connect	
46	DOUT6_P			No Connect	
48	DOUT6_N			No Connect	
50	DOUT7_P			No Connect	
52	DOUT7_N			No Connect	
54	DOUT8_P			No Connect	
56	DOUT8_N			No Connect	
31	DIN1_P	I	AMI	AMI Input	(I1 input on ACS8530 SETS)
33	DIN1_N	I	AMI	AMI Input	(I2 input on ACS8530 SETS)
35	DIN2_P	I	LVPECL/LVDS	Differential Input	(I5 pins on ACS8530 SETS)
37	DIN2_N	I	LVPECL/LVDS	Differential Input	(I5 pins on ACS8530 SETS)
39	DIN3_P	I	LVPECL/LVDS	Differential Input	(I6 pins on ACS8530 SETS)
41	DIN3_N	I	LVPECL/LVDS	Differential Input	(I6 pins on ACS8530 SETS)
21, 23, 25, 27, 29, 43, 45, 47, 49, 51, 53, 55, 57, 58, 59, 60	NC			No Connect	

Microprocessor Interface

The STS-100 has a microprocessor interface incorporated into the module. The module can be configured to function in the modes listed in Table 2. The module is configured by using pins UPSEL[2:0].

Table 7

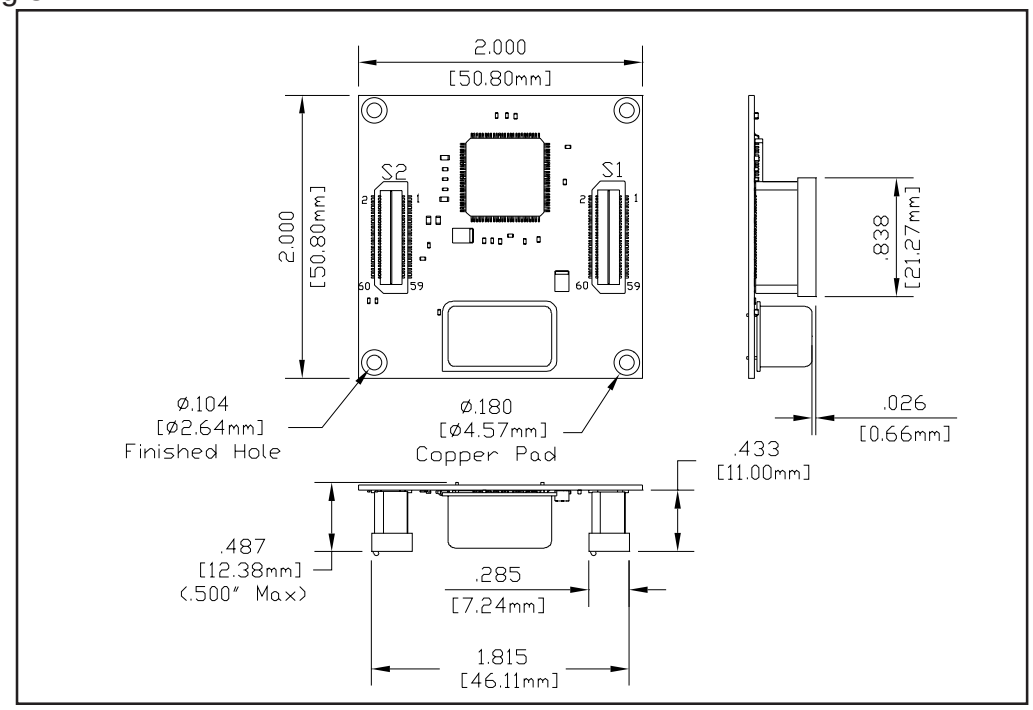
UPSEL[2:0]	MODE
000	Off
001	EEPROM
010	Multiplexed
011	INTEL
100	MOTOROLA
101	Serial
110	Off
111	Off

MOTOROLA mode: Parallel data + address. Compatible with 68x0 type bus.
INTEL mode: Parallel data + address. Compatible with 80x86 type bus.
Multiplexed mode: Data/address. Mode is suitable for microprocessors, which share bus signals between data and address.
Serial mode: Compatible with serial interface.
EEPROM mode: This mode is suitable for use with an EEPROM, in which configuration information is stored (one way communication- status information not accessible).
Note: For timing diagrams and additional details, please refer to the ACS8530 data sheet.

Package Dimensions

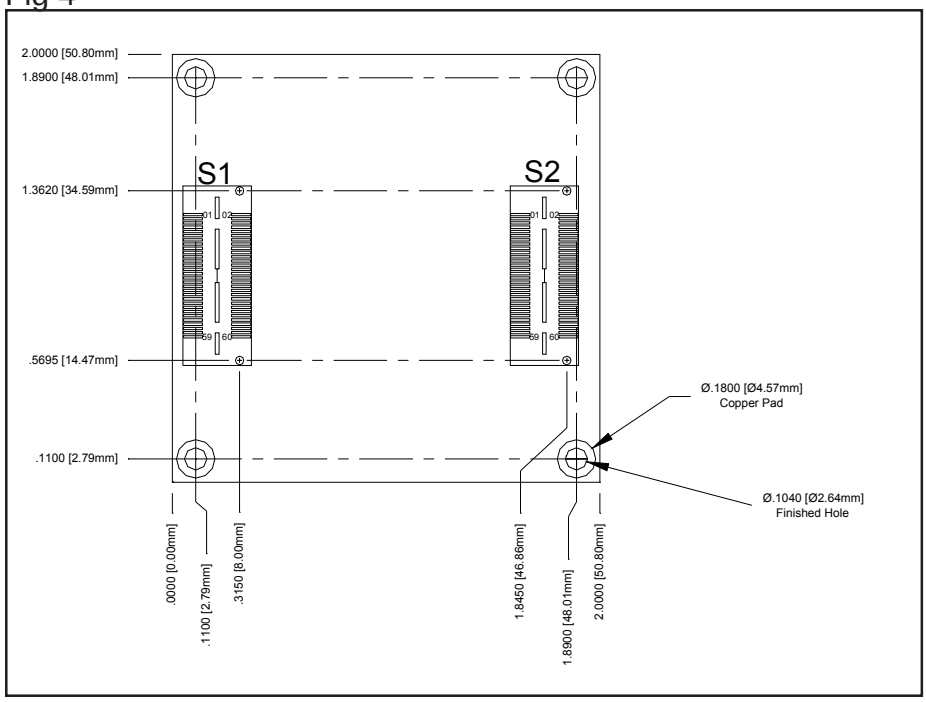
Maximum Board Dimension: L x W x H = 2” x 2” x 0.5”

Fig 3



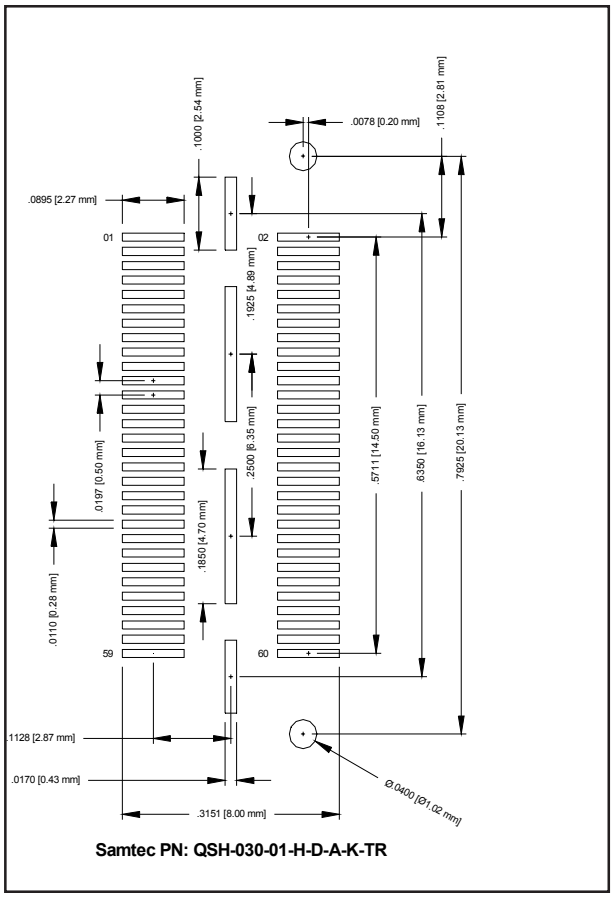
Recommended Connector Placement and Component Keep Out Area

Fig 4



Recommended Connector Footprint Dimensions

Fig 5



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Revision	Revision Date	Note
P00	8/27/01	Preliminary Product Release
P01	8/9/02	Updated current specs & SETS PN
P02	10/10/02	Added millimeter dimensions to mechancial drawings.
P03	4/25/06	Added ROHS-5/6 Compliance