

# M62362P/FP

## 1280 Resolution 3ch Multiplying D/A Converter

REJ03D0873-0201  
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### Description

The M62362P is an integrated circuit semiconductor of CMOS structured with 3 channels of built-in 1280 step resolution (equivalent 10.3-bit) multiplication type D/A converters.

The 3-wire serial interface method and it is able to cascading serial use with  $D_0$  terminal.

The device is suited for use in high accuracy automatic adjustment combination with microcomputer.

### Features

- Digital data transfer method: 3-wire serial data transfer method
- High resolution  
Resolution is more over 10-bit and error is less than  $\pm 1$  LSB
- Capable of 4 quadrant multiplication
- Short setting time
- With reset terminal

### Recommended Operating Condition

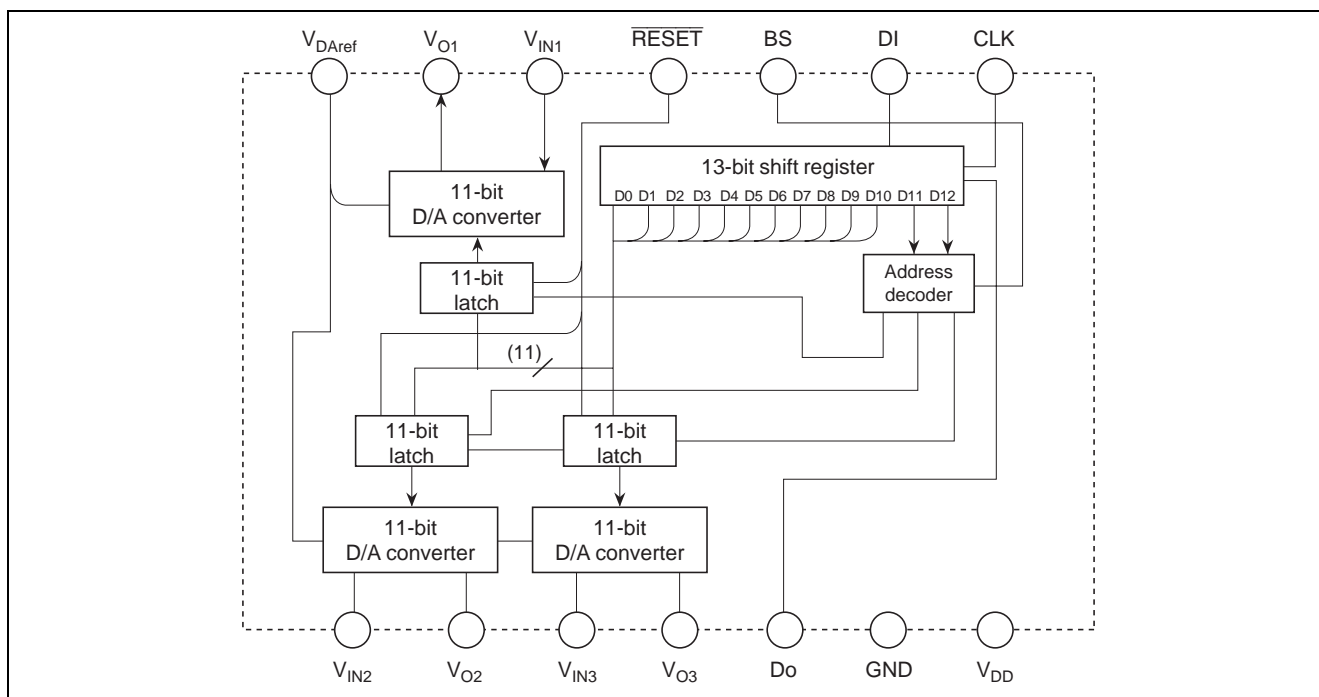
Digital section supply voltage:  $V_{DD} = 5\text{ V} \pm 10\%$

### Application

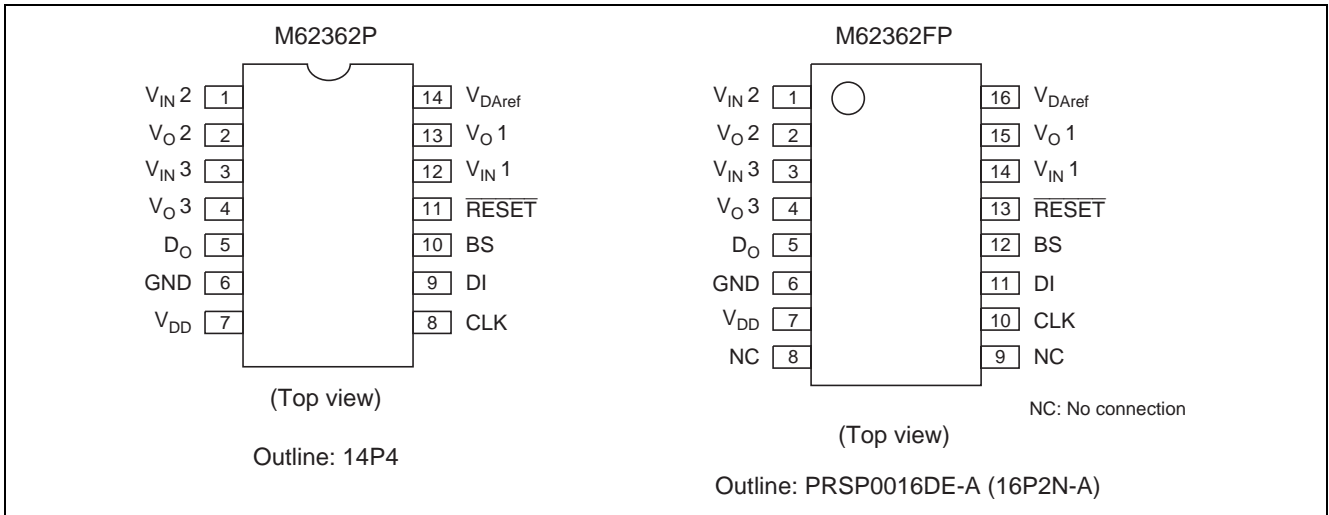
Signal gain control of display-monitor or CTV. Conversion from digital control data to analog control data for home-use and industrial equipment.

Automatic adjustment by combination with EEPROM and microcomputer. (Replacement of conventional half-fixed)

### Block Diagram



## Pin Arrangement

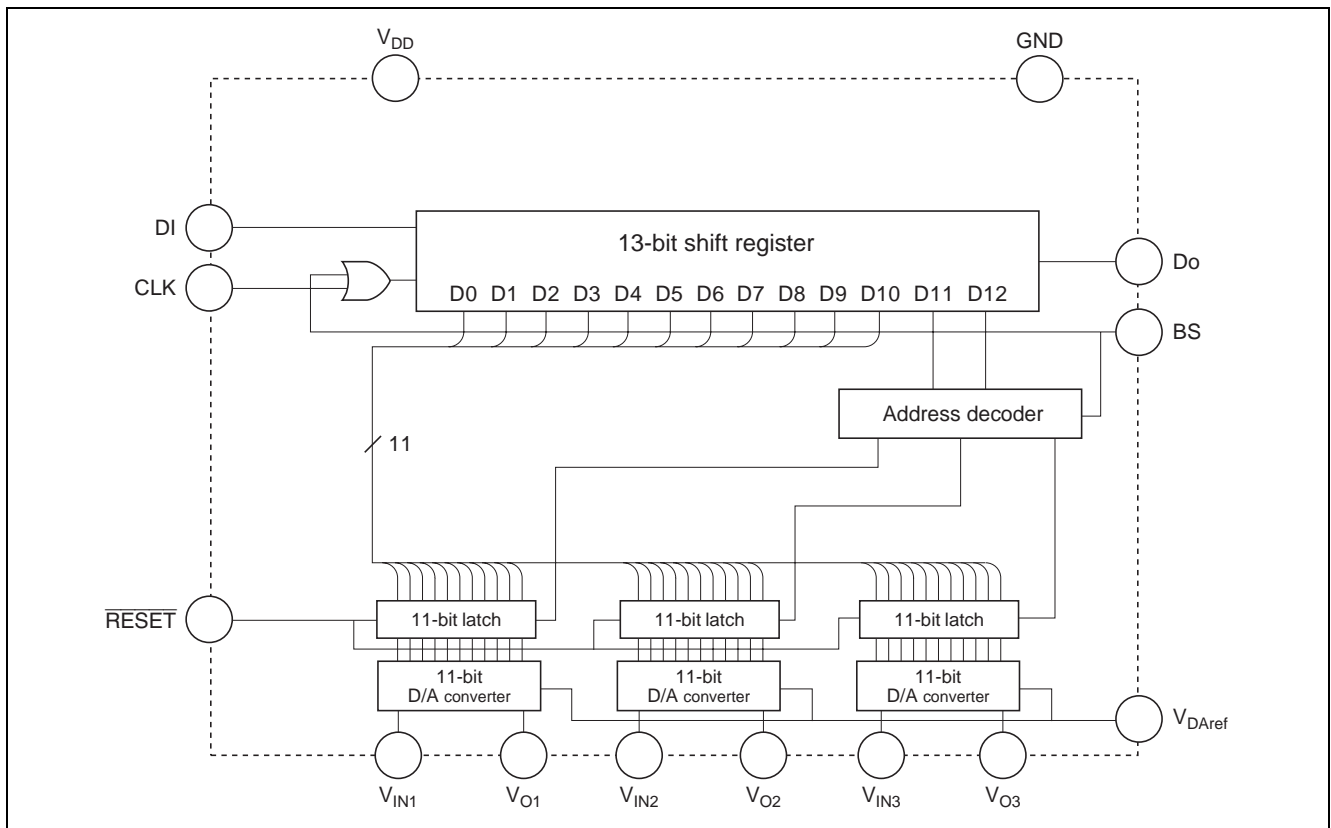


## Pin Description

Pin No.	Pin Name	Function
9 (11)	DI	Serial data input terminal
5	D <sub>O</sub>	Serial data output terminal
8 (10)	CLK	Serial clock input terminal
10 (12)	BS	When BS terminal level is "H" latch circuit data is load
11 (13)	RESET	When RESET terminal level is "L", all D/A output terminal became "L"
13 (15)	V <sub>O1</sub>	1280 resolution D/A output
2	V <sub>O2</sub>	
4	V <sub>O3</sub>	
7	V <sub>DD</sub>	Power supply terminal
6	GND	GND terminal
1	V <sub>IN2</sub>	D/A converter input terminal
3	V <sub>IN3</sub>	
12 (14)	V <sub>IN1</sub>	
14 (16)	V <sub>DAref</sub>	D/A converter reference voltage input terminal

Note: ( ) : M62362FP

## Block Diagram for Explanation of Terminals



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{DD}$	-0.3 to +7.0	V
Digital input voltage (DI, CLK, BS)	$V_{IND}$	-0.3 to +7.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$	-0.3 to $V_{DD} + 0.3$	V
D/A reference voltage	$V_{DAref}$	-0.3 to $V_{DD} + 0.3$	V
Operating temperature	$T_{opr}$	-20 to +85	°C
Storage temperature	$T_{stg}$	-40 to +125	°C

## Electrical Characteristics

### <Digital Part>

( $V_{DD}$ ,  $V_{IN} = +5\text{ V} \pm 10\%$ ,  $V_{DD} \geq V_{IN}$ ,  $GND = V_{DAREF} = 0\text{ V}$ ,  $T_a = -20$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	$V_{DD}$	4.5	5.0	5.5	V	
Input leak current	$I_{ILK}$	-10	—	10	$\mu\text{A}$	$V_{IN} = 0$ to $V_{DD}$
Input low voltage	$V_{IL}$	—	—	$0.2 V_{DD}$	V	
Input high voltage	$V_{IH}$	$0.8 V_{DD}$	—	—	V	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.5\text{ mA}$
Output high voltage	$V_{OH}$	$V_{DD} - 0.4$	—	—	V	$I_{OH} = -400\ \mu\text{A}$

### <Analog Part>

( $V_{DD}$ ,  $V_{IN} = +5\text{ V} \pm 10\%$ ,  $V_{DD} \geq V_{IN}$ ,  $GND = V_{DAREF} = 0\text{ V}$ ,  $T_a = -20$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions	
		Min	Typ	Max			
Input voltage	$V_{IN}$	0	—	$V_{DD}$	V		
Output voltage	$V_O$	0	—	$V_{DD}$	V	$V_{IN} = 0$ to $V_{DD}$	
Input current	$I_{IN}$	—	0.75	1.5	mA	$V_{IN} = 5\text{ V}$ , $V_{DAREF} = 0\text{ V}$ Proportional to $(V_{IN} - V_{DAREF})$	
D/A reference source current	$I_{DAREF}$	-4.5	-2.25	—	mA	$V_{IN1} = V_{IN2} = V_{IN3} = 5\text{ V}$ , $V_{DAREF} = 0\text{ V}$ Proportional to $(V_{IN} - V_{DAREF})$	
D/A output sink or source current	$I_O$	-1.0	—	1.0	$\mu\text{A}/\text{LSB}$		
Output impedance	$R_O$	—	1.8	3.6	$\text{k}\Omega$	Constant for all D/A output mode	
Resolution	RES	—	1280	—	STEP		
Accuracy	Differential nonlinearity	DNL	-1	—	1	LSB	
	Nonlinearity	NL	-0.6	—	0.6	%FS	
	Nonlinearity for channels	$\Delta\text{NL}$	-0.4	—	0.4	%FS	

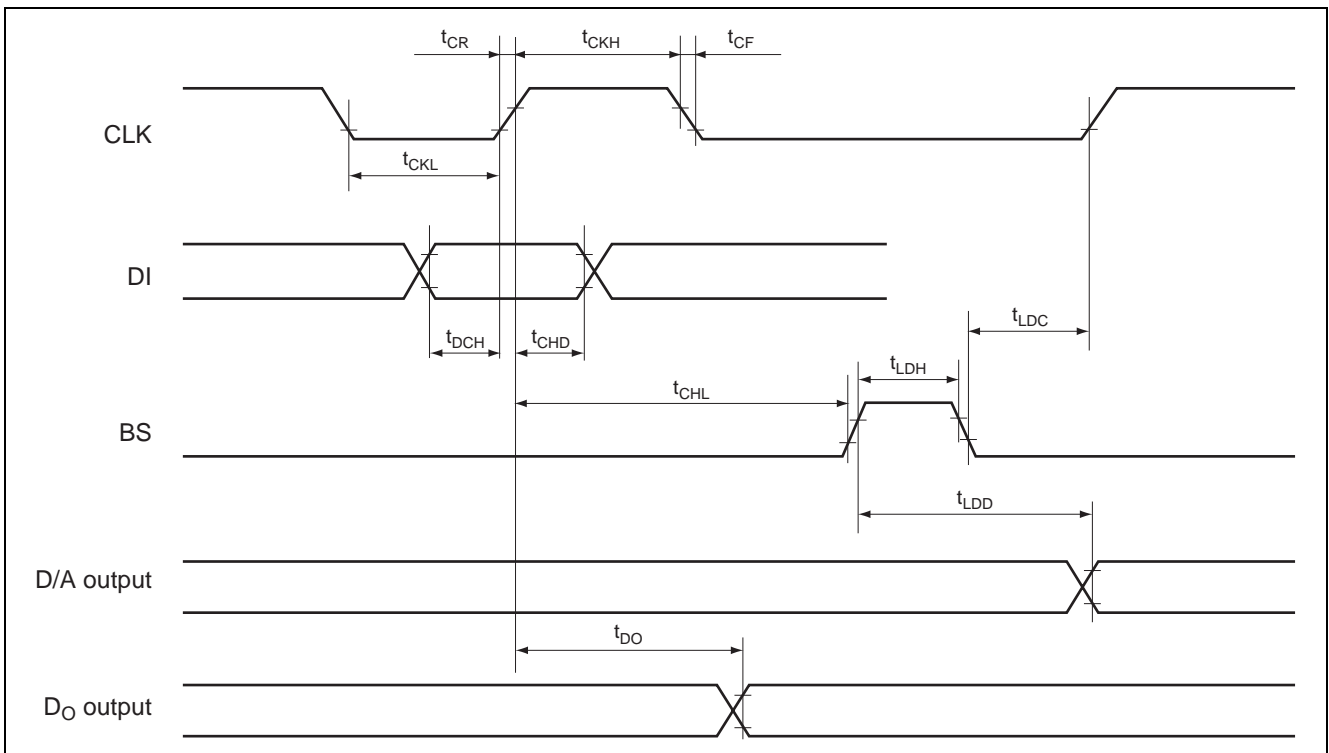
Note: Polarity of current, (+) is sink into IC and (-) is source from IC.

## AC Characteristics

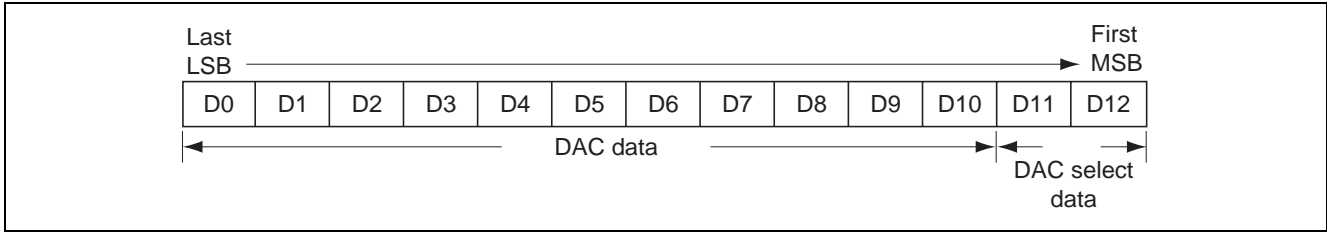
( $V_{DD}$ ,  $V_{IN} = +5\text{ V} \pm 10\%$ ,  $V_{DD} \geq V_{IN}$ ,  $GND = V_{Dref} = 0\text{ V}$ ,  $T_a = -20\text{ to }+85^\circ\text{C}$ )

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	$t_{CKL}$	200	—	—	ns	
Clock "H" pulse width	$t_{CKH}$	200	—	—	ns	
Clock rise time	$t_{CR}$	—	—	200	ns	
Clock fall time	$t_{CF}$	—	—	200	ns	
Data setup time	$t_{DCH}$	60	—	—	ns	
Data hold time	$t_{CHD}$	100	—	—	ns	
LD setup time	$t_{CHL}$	200	—	—	ns	
LD hold time	$t_{LDC}$	100	—	—	ns	
LD "H" pulse width	$t_{LDH}$	100	—	—	ns	
Data output delay time	$t_{DO}$	70	—	350	ns	$C_L \leq 100\text{ pF}$
Data output setting time	$t_{LDD}$	—	—	20	$\mu\text{s}$	No load
Input/output response time		—	—	5		$f = 10\text{ kHz}$

## Timing Chart



## Digital Data Format



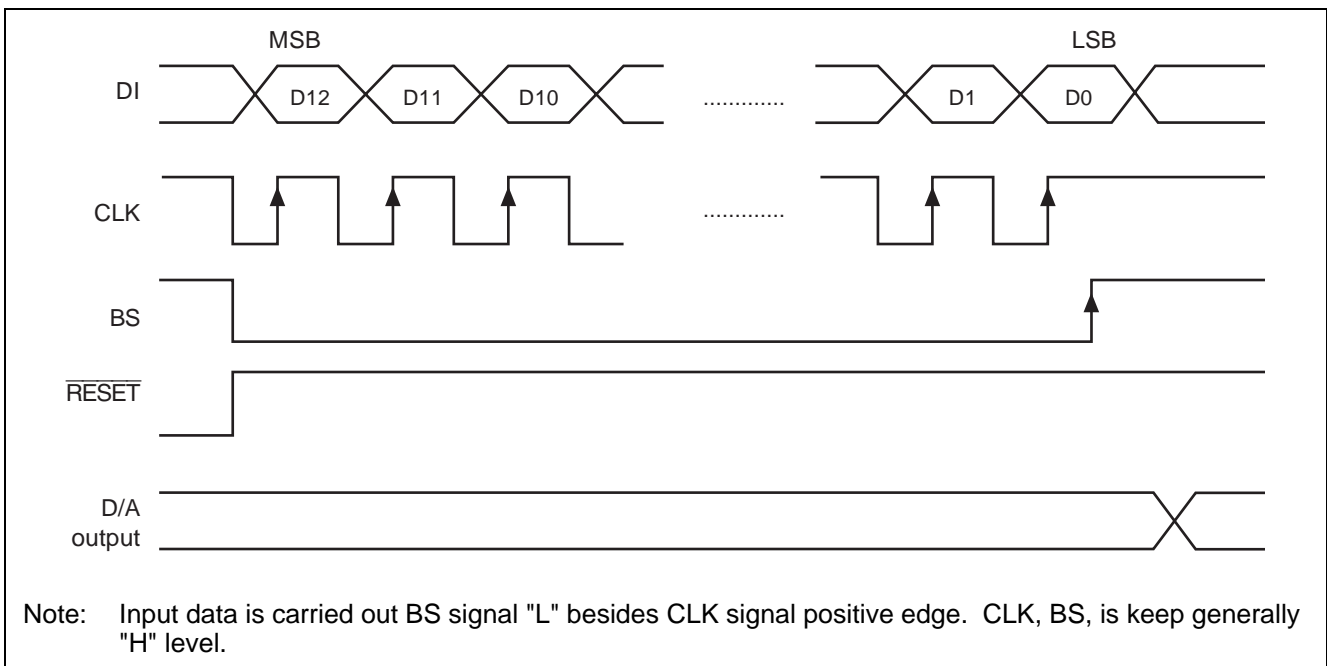
### DAC Data

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D/A Output
0	0	0	0	0	0	0	0	0	0	0	$V_{DAref}$
1	0	0	0	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 1280 \times 1 + V_{DAref}$
0	1	0	0	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 1280 \times 2 + V_{DAref}$
1	1	0	0	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 1280 \times 3 + V_{DAref}$
:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	0	0	1	$(V_{IN} - V_{DAref}) / 1280 \times 1279 + V_{DAref}$
0	0	0	0	0	0	0	0	1	0	1	$V_{IN}$
:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	1	$V_{IN}$

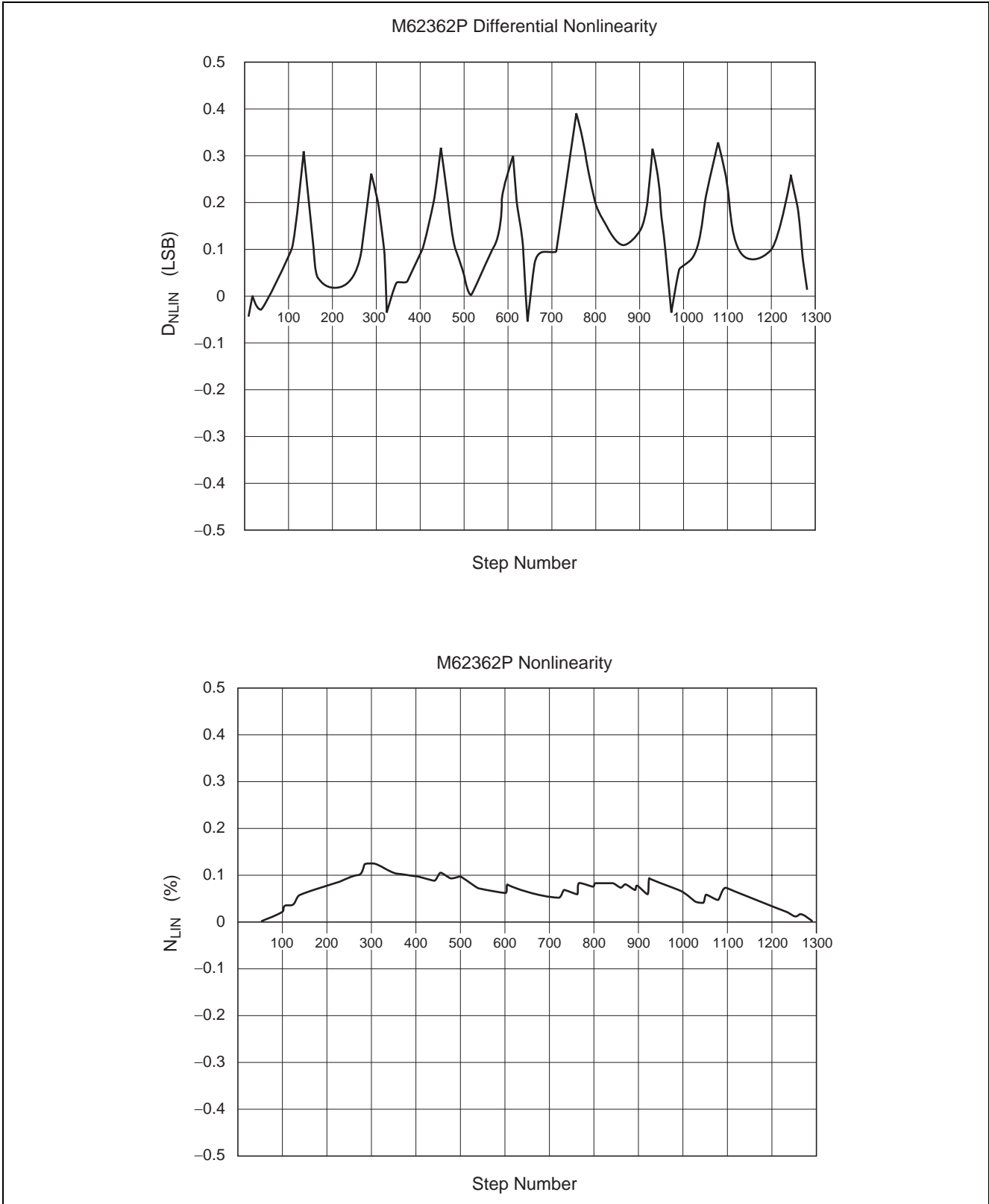
### DAC Select Data

D11	D12	DAC Selection
0	0	Don't care
0	1	ch1
1	0	ch2
1	1	ch3

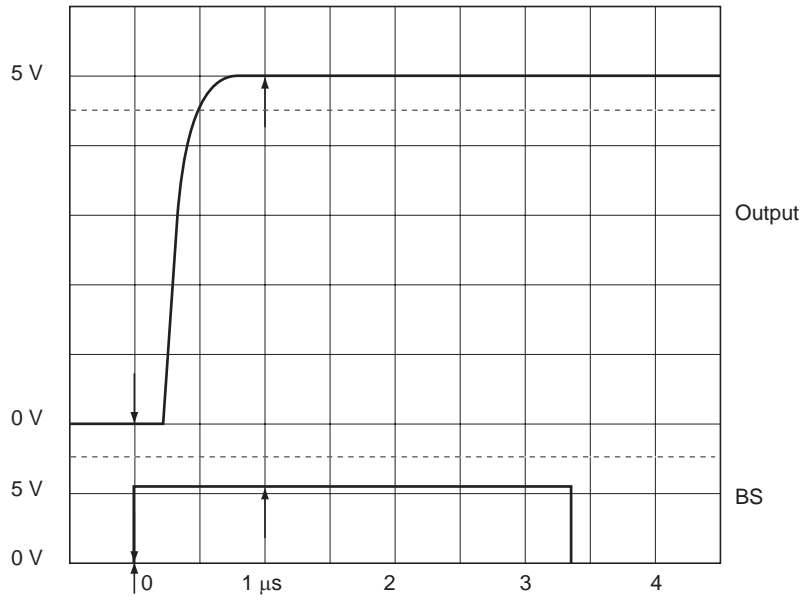
### Timing Chart (Model)



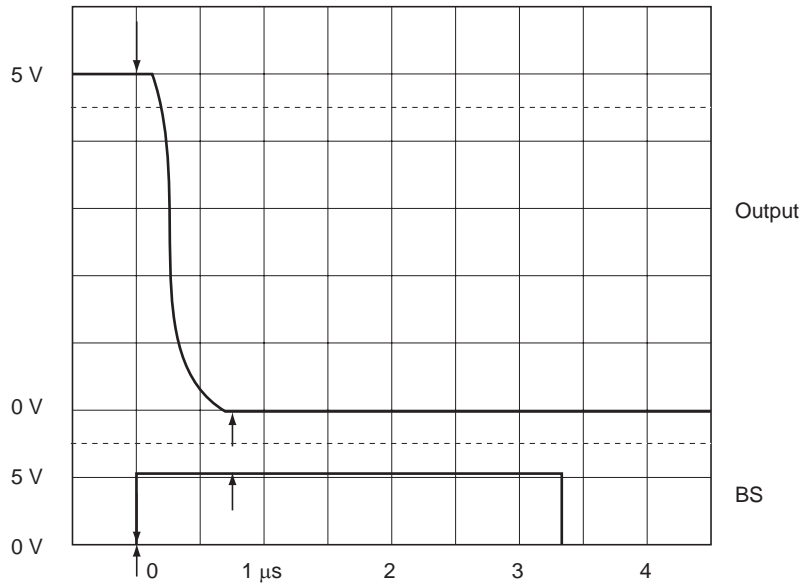
### Typical Characteristics



M62362P Output Rise Characteristics (Setting Time)



M62362P Output Fall Characteristics (Setting Time)

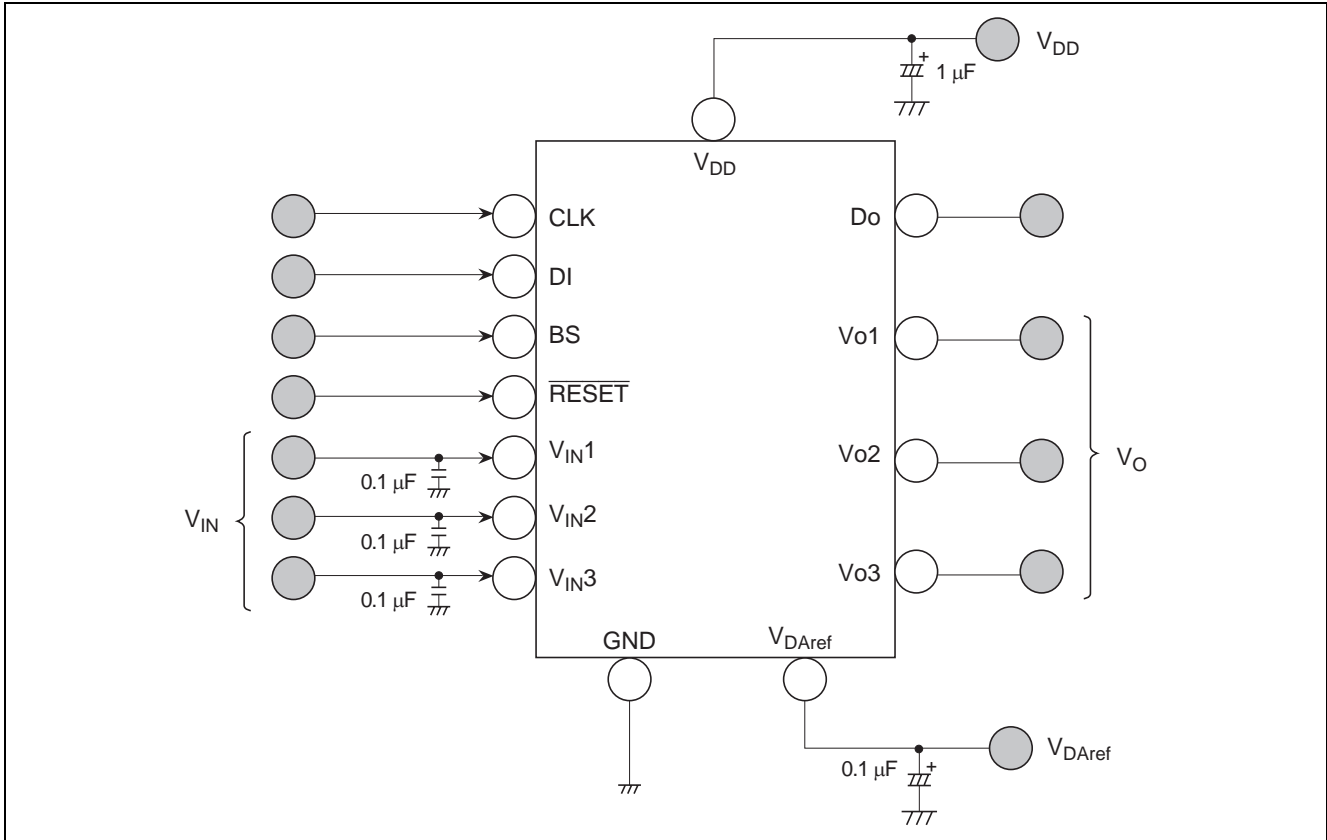




### Precaution for Use

M62362 have 5 terminals these are input free voltage at use. ( $V_{DD}$ ,  $V_{IN1}$ ,  $V_{IN2}$ ,  $V_{IN3}$ ,  $V_{DAref}$ ) If ripple and spike is input to these terminals, accuracy of conversion is down. So, when use this device, please connect capacitor among to each terminals and GND for stable operation.

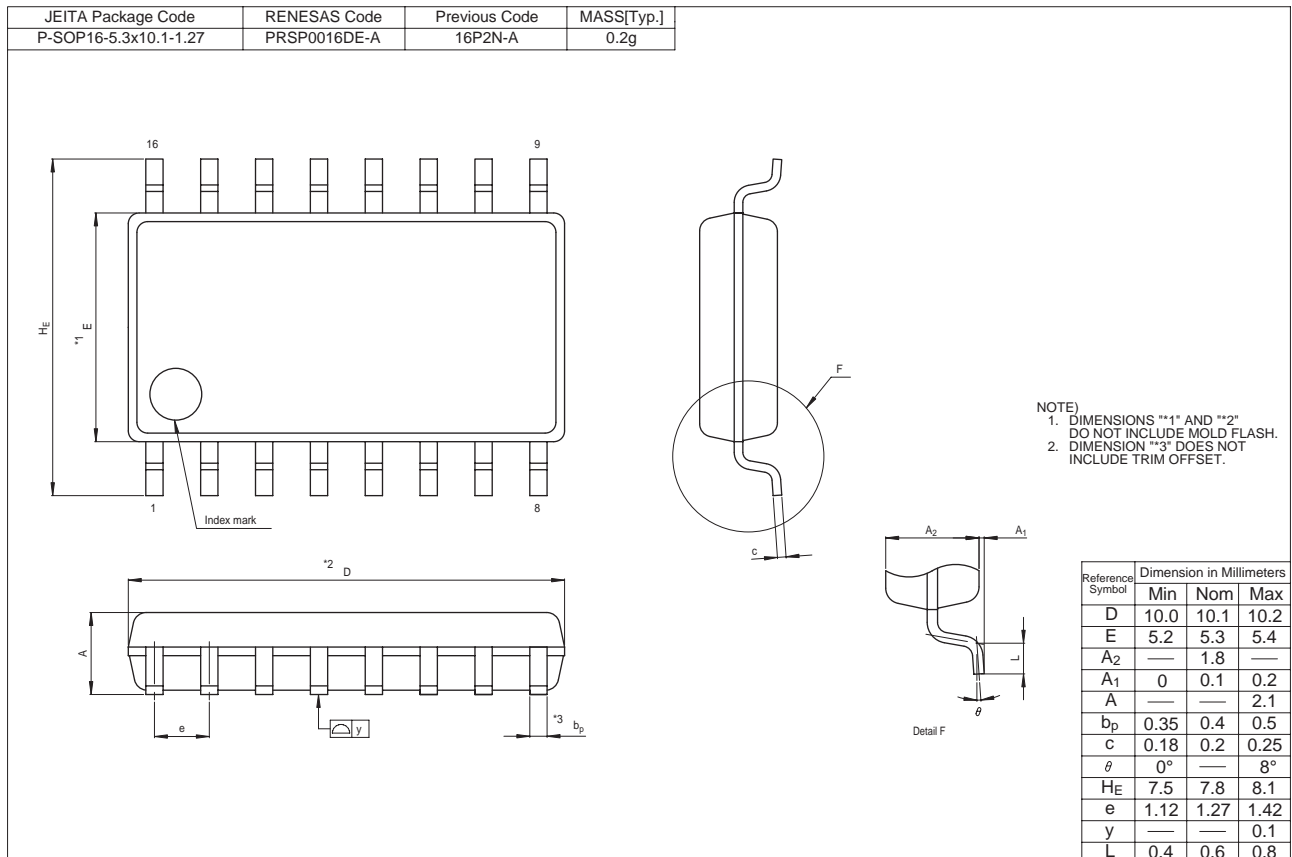
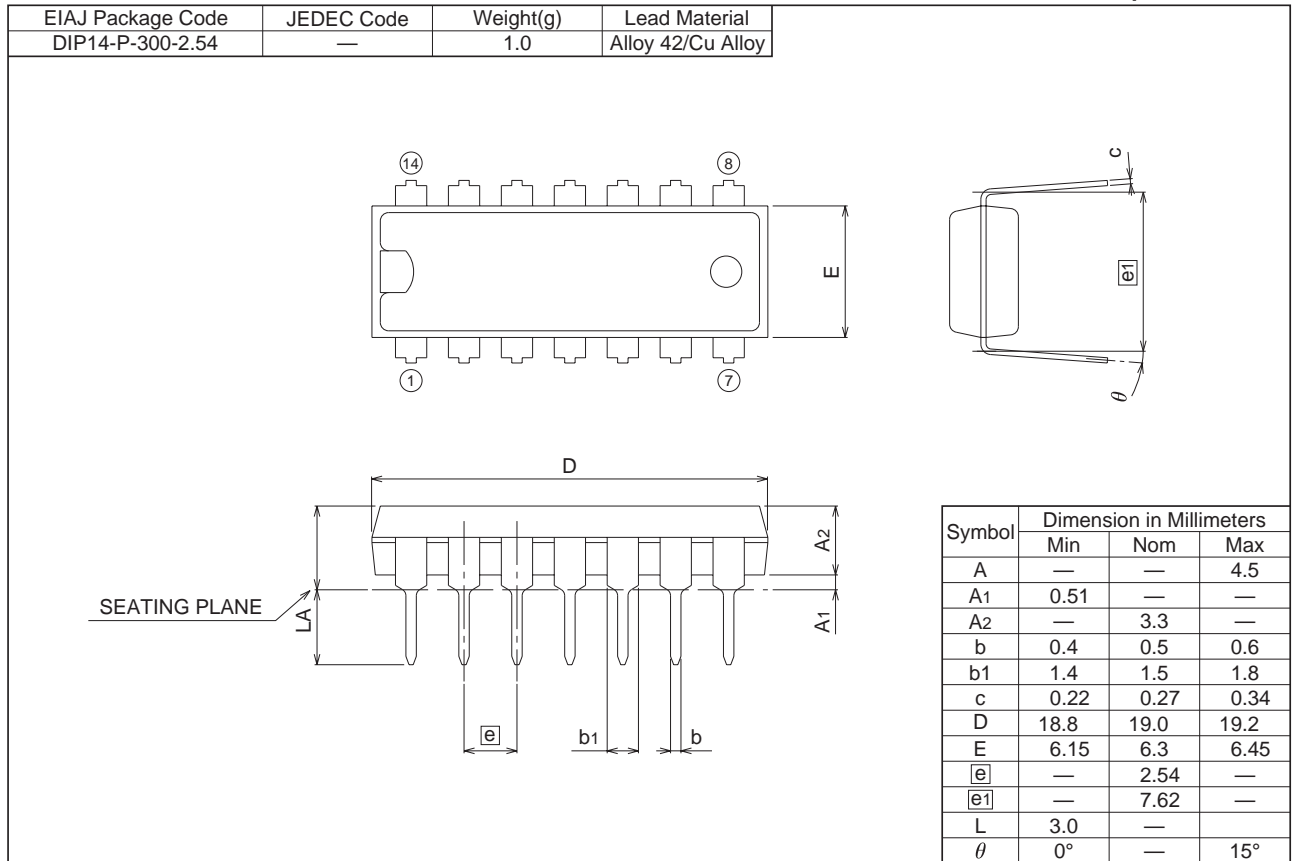
### Application Example



### Package Dimensions

#### 14P4

Plastic 14pin 300mil DIP



Notes:

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