SIRENZA 2.4GHz to 5.8GHz Frequency Translator ADVANCED Datasheet

GENERAL DESCRIPTION

The ML5825 is a high integration 2.4GHz - 5.8GHz frequency translator (transverter). It upconverts 2.4GHz signals to 5.8GHz and downconverts received 5.8GHz signals to 2.4GHz. Transmit and receive utilize the same low noise fixed local oscillator (LO). It is intended to be used in conjunction with a 2.4GHz transceiver-based solution to quickly and easily develop a 5.8GHz solution while fully leveraging previous development.

The ML5825 receive chain contains a Low Noise Amplifier (LNA), bandpass filter and image reject down conversion mixer. A digitally controlled 18dB gain step in the receive chain provides an innovative solution for optimizing IIP3 (low gain mode) and Noise Figure (high gain mode). On the transmit side, the ML5825 buffers and upconverts a differential 2.4GHz signal to 5.8GHz, where it is filtered and amplified.

The ML5825's PLL accepts two industry-standard input clock frequencies. The ML5825's low STANDBY MODE current maximizes battery life. Power supply regulation is included in the ML5825, providing circuit isolation and consistent performance over supply voltages between 2.8V-3.6V.

PIN CONFIGURATION



ORDERING INFORMATION

PART NUMBER	TEMP RANGE	PACKAGE	PACK (QTY)
ML5825DM	-10°C to +60°C	28QFN 4x5x0.9 mm	Antistatic Tray (490)
ML5825DM-T	-10°C to +60°C	28QFN 4x5x0.9 mm	Tape & Reel (2500)

FEATURES

- High Integration 2.4GHz to 5.8GHz Transverter
 - Receive LNA, Image Reject Filter & Mixer
 - Transmit Pre-Driver, Filters & Mixers
 - Fully Integrated PLL-Based Synthesizer
- Selectable Receive Gain Optimizes NF and IIP3
- Interfaces Directly with Many 2.4GHz Transceivers
- 4dB (typ. High Gain Mode) Noise Figure
- -14dBm Input IP3 (Low Gain Mode)
- Selectable Transmit Output Power
- 10µA Standby Mode
- Space-saving 28 pin QFN package

APPLICATIONS

- 5.8GHz Digital Cordless Telephones
- 5.8GHz Streaming Audio & Video
- Upconverted 2.4GHz Standards
 - o Bluetooth
 - o Zigbee/802.15.4

BLOCK DIAGRAM



SIRENZA MICRODEVICES

ML5825

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SIMPLIFIED APPLICATIONS DIAGRAM



Figure 1: ML5825 Typical Application Schematic



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. Operating the device for any length of time beyond the operating conditions may degrade device performance and/or shorten operating lifetime.

VCCA	
Maximum Receive RF Input Power	+13dBm
Maximum Transmit RF Input Power	+3dBm
Junction Temperature	150°C
Storage Temperature Range	65°C to 150°C
Lead Temperature (Soldering, 10s)	
Thermal Resistance (θ_{JA})	

OPERATING CONDITIONS

Ambient Temperature Range	10°C to 60°C
VCCA Range	

Unless otherwise specified, V_{CCA} =3.2V, T_A =-10°C to +60°C, XCEN= V_{IH} , P_{INRX} =-40dBm, P_{INTX} =-3dBm, PLL Loop Filter Bandwidth=40 KHz, and gain control in either state.

SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS
POWER S	UPPLIES					
VCCA	Analog supply voltage		2.8	3.2	3.6	V
I _{STBY}	Supply current, STANDBY mode	VCCA=3.6V, XCEN=V _{IL} , TXON= V _{IL} OR V _{IH}			10	μΑ
I _{RX}	Supply current, RECEIVE mode	TXON= V _{IL}		45	60	mA
I _{TX}	Supply current, TRANSMIT mode	TXON= V _{IH} R _{TXISET} =7.5K Ω R _{TXISET} =5.5K Ω		95 100	110 115	mA mA
SUPPLY R	EGULATION	<u>.</u>	·			
V _{R27}	Regulated Output Voltage	Pins 12, 19, 26		2.7		V
V _{R25}	Regulated Output Voltage	Pin 17		2.5		V
V_{BG}	Bandgap Voltage	Pins 18 & 25		1.25		V
SYNTHES	ZER					
f _{LO}	Local Oscillator Frequency	$F_{OUT} = F_{IN} + / - F_{LO}$		3342.336		MHz
Ι _Ρ	Charge Pump sink/source current This is a function of V_{TUNE} to compensate for the change in $K_{\rm V}$	V _{TUNE} =0.3V V _{TUNE} =1.2V V _{TUNE} =1.9V	0.49	0.90 0.60 0.38	0.71	mA mA mA
Φ _N	Phase noise at driver output f_o =10KHz offset from f_c f_o =1.2MHz offset from f_c	400mVp-p sine wave reference		-65 -115	-110	dBc/Hz dBc/Hz
Kv	VCO Tuning sensitivity		100	230	350	MHz/V
F _{PULL}	Frequency pulling	70µs after P_{IN} –50dBm to +12dBm		+/-20		KHz
F _{PTR}	Frequency pulling TX to RX and RX to TX	70µs after transition		+/-20		KHz
F _{PUSH}	Frequency pushing	Vary VCCA from 2.9V to 3.6V		<.5		MHz/V
twake	Settling time from standby	XCEN=V _{IH} , to within 10KHz			200	μS



SYMBOL	PARAMETER		CONDITIONS	MIN	ТҮР	MAX	UNITS
f _{FREF}	Reference signal f	requency	REFSEL=V _{IL} REFSEL=V _{IH}		18.432 24.576		MHz MHz
V _{FREF}	Reference signal l	evel	AC coupled	400		1200	mVp-p
RECEIVER	R					L	
F _{RXI}	Receiver Input Fre	equency Range		Ę	5.725 - 5.85	0	GHz
F _{RXO}	Receiver Output F	requency Range		2.38	2664 - 2.50	7664	GHz
Z _{RIN}	Receiver Input Imp	pedance	Over F _{RXI}		37 + j2		Ω
Z _{RXO}	Receiver Output Ir	mpedance	Differential Impedance RXON/RXOP Over F _{RXO}		100		Ω
NF	Input noise figure		High Gain Mode		4.0	7.0	dB
			Low Gain Mode		14	22	dB
G _{RX}	RX Power Gain	High Gain Mode	Pin=-50dBm	8	13		dB
		Low Gain Mode	Pin=-30dBm	05	- 8		dB
I _{IP3}	Input IP3	High Gain Mode	For Pin=-50dBm each tone spaced +/-1MHz from 5800MHz	-25			dBm
		Low Gain Mode	For Pin=-30dBm each tone spaced +/1MHz from 5800MHz		-14		dBm
P _{1dB}	RX Input 1dB com	pression	High Gain Mode		-35		dBm
			Low Gain Mode		-25		dBm
P _{RXI}	RX conducted emi port	issions from RF input	RXI terminated in 50 ohm			-50	dBm
P_{SPUR}	Out of Band Spuri	ous,					
	High Gai	n Mode	Spurs outside Receive Output Frequency Range		-25		dBc
	Low Ga			20	-5		0BC
	RX Image Rejection	n	From RXI to RXO, Pin=-50dBm, F _{RXI} = 835-965MHz	20			aв
TRANSMI	TTER						
F _{TXI}	Transmitter Input F	Frequency Range		2.382664 - 2.507664		GHz	
F _{TXO}	Transmitter Outpu	t Frequency Range		5.725-5.850		0	GHz
Z _{TXI}	Transmitter Input I	Impedance	Differential Impedance TXIN/TXIP Over F _{TXI}		100		Ω
Z _{TXO}	Transmitter Outpu	t Impedance	Over F _{TXO}		43 + j88		Ω
P _{OUT}	TX buffer output p	ower at 5.85 GHz	R_{TXISET} =7.5K Ω , Pin=-6dBm	3.5			dBm
	Matched into 50 ol	hms,	R_{TXISET} =5.5K Ω , Pin=-3dBm	5.5			dBm
R _{TXH}	Transmit harmonic	c output rejection	50 Ohm load		<-20		dBc
R _{LO}	Transmit LO feed	thru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}	-30			dBc
R _{RFIF}	Transmit IF feed th	hru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}	-30			dBc
R _{2LO}	Transmit 2xLO fee	ed thru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}		<-30		dBc
R _{3LO}	Transmit 3xLO fee	ed thru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}		<-20		dBc
R _{4LO}	Transmit 4xLO fee	ed thru	Measured at TXO port with CW signal at F_{TXI} and P_{TXI}		<-20		dBc
R _{TSB}	Transmit lower sid	leband rejection	From TXI to TXO ports at P_{TXI} for F_{TXO} = 835-960MHz	25			dBc



SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	МАХ	UNITS			
R _{MXN}	Mixer products rejection at output port	From TXI to TXO ports at P_{TXI} for F_{TXO} = 960-970MHz		>55		dBc			
INTERFAC	INTERFACE LOGIC LEVELS								
Input pins	(XCEN, TXON, RXGN, REFSEL)								
V _{IH}	Input high voltage		VCCA*0.7		VCCA+0.4	V			
VIL	Input low voltage		-0.4		VCCA*0.3	V			
I _B Input bias current		All states	-5		5	μA			
C _{IN}	Input capacitance	1MHz test frequency		4		pF			

PIN DESCRIPTIONS

PIN	NAME	I/O	FUNCTION	DIAGRAM		
POW	POWER & GROUND					
2	VSSMX	GROUND	Mixer Ground	N/A		
7	VCCA	POWER	Regulated External Supply, Requires Proper Decoupling Components	N/A		
14	VSSPLL	GROUND	PLL Ground	N/A		
15	VSSLO	GROUND	VCO and LO Ground	N/A		
24	VTXB	INPUT	TX Buffer Supply Voltage, Connect to Pin 7	N/A		
Х	VSSDB	GROUND	Exposed Paddle. Ground/Return	N/A		

SUPI	SUPPLY REGULATION					
1	VMIX	INPUT	2.7V Supply Decoupling Point, Connect to Pin 26	N/A		
12	VREG1	OUTPUT	2.7V Regulated Supply Output	N/A		
17	VREG2	OUTPUT	2.5V Regulated Supply Output	N/A		
18	VBG2	OUTPUT	1.24V Bandgap2 Supply Decoupling Point	N/A		
19	VREG3	OUTPUT	2.7V Regulated Supply Decoupling Point	N/A		
25	VBG1	OUTPUT	1.24V Bandgap1 Supply Decoupling Point	N/A		
26	VREG4	OUTPUT	2.7V Regulated Supply Output, Connect to Pins 1 and 28	N/A		
28	VLNA	INPUT	2.7V LNA Supply Decoupling Point, Connect to Pin 26	N/A		



RF T	RANSMIT/REG	CEIVE DATA		
27	RXI	I (analog)	5.8GHz RX Input. A simple matching network is required for optimum noise figure. This input connects to the base of an NPN transistor and should be AC coupled.	VLNA 28 0.7V 3.9K RXI 27 VSSDB
23	ТХО	O (analog)	5.8GHz TX Output into a matched load over the 5725 to 5850 MHz range.	VTXB 24 TXO 23 VSSDB
4 3	RXOP RXON	O (analog)	Differential 2.4GHz RX Output.	VCCA 7 56Ω RXOP 4 VSSMX VSSDB
20 21	TXIP TXIN	I (analog)	Differential 2.4GHz TX Input	VCCA TXIP 20 TXIN 21 VSSMX VSSDB



RF C	ONTROL & O	THERS		
11	XCEN	I (CMOS)	Transceiver Enable Input. Enables the bandgap reference and voltage regulators when high. Consumes only leakage current in STANDBY mode when low. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	VCCA 7 ×CEN 11 168Ω 2 VSSMX
10	TXON	I (CMOS)	TX/RX Control Input. Switches the transceiver between TRANSMIT and RECEIVE modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	VCCA 7 TXON 10 VCCA 7 168Ω 168Ω VCCA
5	RFISET	l (analog)	Connect to a 255Ω +/-1% resistor to ground.	VCCA 7 RFISET 5 2 VSSMX
6	RXGN	I (CMOS)	Gain Step Input Control. Switches the receiver between high gain (when HIGH) and low gain (when LOW). This dual-gain design allows the system designer to achieve low noise figure for low input signals while maintaining a good IIP3 under high input signal conditions. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	VCCA 7 πxgn 6 168Ω VSSMX



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13	QPO	O (analog)	Charge Pump Output. This output is connected to the external PLL loop filter. Sources current when the LO frequency is lower than desired.	VREG1 12 QPO 13 9.20 14 VSSPLL
16	VTUNE	I (analog)	VCO Tuning Voltage. This input from the PLL loop filter determines the output frequency and is very sensitive to noise coupling and leakage currents.	VREG3 19 VTUNE VTUNE VREG2 16 VREG2 17 100 VREG2 17 VREG2 VREG2 VREG2 VREG2 VREG3
22	TXISET	I (analog)	A resistor between this pin and ground establishes the PA output power compression point by setting a bias current.	TXISET Z2 VCCA TXISET Z2 VSSMX
8	FREF	I (analog)	Input Reference Frequency. Depending on the state of the REFSEL pin this input is divided by 3 or 4 to generate the PLL reference frequency.	VCCA T T FREF B VCCA T T T T T T T T T T T T T
9	REFSEL	I (CMOS)	Reference Divider Control. If REFSEL is HIGH, FREF is divided by 4, otherwise FREF is divided by 3. This is a CMOS input, and the thresholds are referenced to VCCA and VSSMX.	VCCA 7 REFSEL 9 168Ω 2 VSSMX



FUNCTIONAL DESCRIPTION

The ML5825 is a monolithic, bilateral 2.4GHz to 5.8GHz frequency translator. It provides a simple and straightforward solution for designers of 2.4GHz products who want to develop advanced products for the relatively interference-free 5.8GHz band, especially digital cordless telephones. The ML5825 can implement "dual band" solutions that use both the 2.4GHz and 5.8GHz bands as well as "hybrid" products where one link (say, basestation transmission) is at 5.8GHz, while the other link (basestation receive) is at 2.4GHz.

5.8GHz signals enter the RXI pin and then are fed to an LNA and bandpass filter. An image-reject downconvert mixer translates the signal to the 2.4GHz ISM band where it is then buffered and sent off chip differentially on RXON/RXOP. The receive signal path can be configured for either a "High Gain" mode (about 13dB) or "Low Gain" mode (-8dB). Gain mode is selected via the RXGN digital input pin. High Gain mode is used for low-level input signals to minimize Noise Figure while Low Gain mode optimizes input IP3 for stronger signals.

2.4GHz signals come into the ML5825 differentially on the TXIP/TXIN pins, where they are upconverted to 5.8GHz, bandpass filtered, and then amplified and exit via TXO. The predriver/buffer output power compression point is programmed by an external resistor that sets the preamp bias level.

A fully integrated phase locked loop (PLL) generates the fixed local oscillator (LO) at 3342.336 MHz which is used for upconverting and downconverting the RF signals. The comparison frequency of the PLL is derived from the frequency reference present on the FREF pin and the state of REFSEL as shown in Table 1. The PLL loop filter is external to the ML5825 so that lock time and in-band phase noise can be optimized for the system of interest.

REFSEL	REFERENCE DIVISION	FREF
V _{IL}	3	18.432 MHz
V _{IH}	4	24.576 MHz

Table 1: ML5825 Frequency References

The ML5825 contains two separate bandgap references and several low dropout (LDO) voltage regulators to insure consistent performance over supply voltage and minimize crosstalk on chip. The device is enabled by bringing XCEN to V_{IH} and is placed in transmit mode by setting TXON to V_{IH} . With XCEN at V_{IL} the ML5825 enters a low power standby mode.

MODES OF OPERATION

The ML5825 has three key modes of operation. The two operational modes are RECEIVE and TRANSMIT, controlled by TXON. XCEN is the chip enable/disable control pin, which sets the device in operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is summarized in Table 2.

XCEN	TXON	MODE NAME	FUNCTION
0	Х	STANDBY	Standby. All circuits powered down
1	0	RECEIVE	Receive Chain Active
1	1	TRANSMIT	Transmit Chain Active

Table 2: Modes of Operation



STANDBY MODE

In STANDBY mode, the ML5825 transverter is powered down. When exiting STANDBY mode, the transmitter is disabled for 200µs. However, the receive path is not similarly locked out and so will receive invalid data for up to 200µs. Therefore, the system should wait 200µs after exiting STANDBY mode before actively processing signals to allow the PLL to lock. A timing diagram for the ML5825 is shown in Figure 2.



Figure 2: ML5825 Control Timing Diagram, assuming a 40 KHz loop bandwidth.

RECEIVE MODE

In RECEIVE mode, the received signal at 5.8GHz is amplified, filtered, and downconverted to 2.4GHz. The receiver has two gain modes; High Gain (about 13dB) and Low Gain (about -8dB). Gain mode is set via the state of the RXGN input, with High Gain Mode corresponding to a logic "1" on RXGN.

TRANSMIT MODE

In TRANSMIT mode, the transmitted signal at 2.4GHz is upconverted, filtered, and amplified at 5.8GHz. The transmit output power compression point is programmable via an external resistor on the TXISET pin.



PHYSICAL DIMENSIONS



Figure 3: 28 Pin QFN Package Dimensions



WARRANTY

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.



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