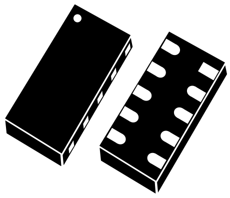
STG3689

Low Voltage 0.9Ω max dual SPDT Switch with break-before-make feature

Features

- Low quiescent supply current:
  – Max ±50µA for V_{1IN}, V_{2IN} = 1.80V at V_{CC} = 4.3V
- Ultra low power dissipation:
  – I_{CC} = 0.2µA (Max.) at T_A = 85°C, V_{IN} = 0V
- Switch S1: Low "ON" resistance V_{IN} = 0V:
  – R_{ON} = 0.7Ω (Max. T_A =25°C) at V_{CC} = 4.3V
  – R_{ON} = 0.9Ω (Max. T_A = 25°C) at V_{CC} = 3V
- Wide operating voltage range:
  – V_{CC} (OPR) = 1.65V to 4.3V single supply
- 4.3V Tolerant and 1.8V compatible threshold on digital control input at V_{CC} = 1.65 to 4.3V
- Latch-up performance exceed 300mA (JESD 17)
- ESD performance (Analog chan. Vs. GND): HBM >2kV (MIL STD 883 method 3015)



TDFN10

Description

The STG3689 is a high-speed CMOS low voltage dual analog S.P.D.T. (Single Pole Dual Throw) switch or 2:1 Multiplexer/Demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

The nIN inputs are provided to control the switches.

The switches nS1 are ON (they are connected to common Ports Dn) when the nIN input is held high and OFF (high impedance state exists between the two ports) when nIN is held low. The switches nS2 are ON (they are connected to common Ports Dn) when the nIN input is held low and OFF (high impedance state exists between the two ports) when IN is held high.

Additional key features are fast switching speed, and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Order codes

Part number	Package	Packaging
STG3689DTR	TDFN10 (2.5mm x 1.3mm)	Tape & Reel

Contents

1 Summary description

1.1 Pin connections and description

Figure 1. Pin connections (Top through view)

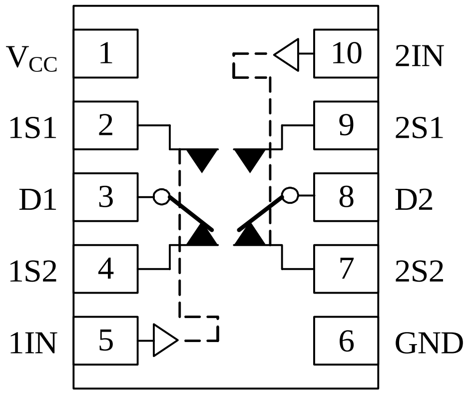
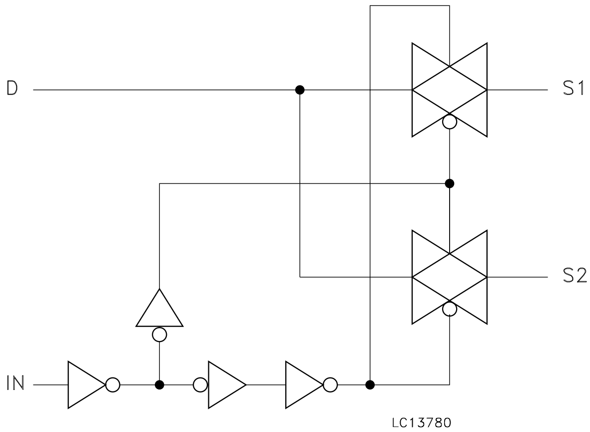


Table 1. Pin function

Pin Nº	Symbol	Name and function
5, 10	1IN, 2IN	Controls
2, 4, 9, 7	1S1, 1S2 2S1, 2S2	Independent channels
3, 8	D1, D2	Common channels
1	V_{CC}	Positive supply voltage
6	GND	Ground (0V)

1.2 Input equivalent circuit

Figure 2. Input equivalent circuit



2 Electrical ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{IN} < 0V)	-50	mA
I_{IK}	DC input diode current (V_{IN} < 0V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±200	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	±400	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70ºC (1)	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec.)	300	°C

1. Derate above 70ºC by 18.5mW/C

3 Electrical characteristics

3.1 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage [(1)]		1.4 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
d_t/d_v	Input rise and fall time control Input	V_{CC} = 1.65V to 2.7V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.3V	0 to 10	

1. Truth Table guaranteed: 1.2V to 4.3V

3.2 DC Specifications

Table 4. DC specifications

Symbol	Parameter	Test conditions		Value							Unit
		V_{CC}(V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ	Max.	Typ	Max.	Typ	Max.	
V_{IH}	High level input voltage	1.65-1.95		0.65 V_{CC}			0.65 V_{CC}		0.65 V_{CC}		V
		2.3-2.5		1.4			1.4		1.4		
		2.7-3.0		1.4			1.4		1.4		
		3.3 – 4.3		1.5			1.5		1.5		
V_{IL}	Low level input voltage	1.65-1.95				0.40		0.40		0.40	V
		2.3-2.5				0.50		0.50		0.50	
		2.7-3.0				0.50		0.50		0.50	
		3.3 – 4.3				0.50		0.50		0.50	

Table 4. DC specifications

Symbol	Parameter	Test conditions		Value							Unit
		V_{CC}(V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ	Max.	Typ	Max.	Typ	Max.	
R_{ON}	Switch ON resistance	4.3	V_S=0V to V_{CC} I_S=100 mA		0.5	0.7		1.4			Ω
		3.0			0.7	0.9		1.4			
		2.7			0.7	0.9		1.7			
		2.3			0.9	1.2		1.7			
		1.8			1.3	1.6		1.9			
		1.65			1.60	2.5		2.2			
ΔR_{ON}	ON Resistance match between channels 1Sn and 2Sn	2.7	V_S @ R_{ON} Max I_S=100 mA		0.6						Ω
R_{FLAT}	ON resistance FLATNESS (1) (2)	4.3	V_S = 0V to V_{CC} I_S=100 mA		0.18	0.21					Ω
		3.0			0.16	0.19					
		2.7			0.16	0.19					
		2.3			0.18	0.21					
		1.65			0.38	0.44					
I_{OFF}	OFF state leakage current (nSN), (Dn)	4.3	V_S = 0.3 or 4V			±10		±100			nA
I_{IN}	Input leakage current	0 – 4.3	V_{IN} = 0 to 4.3V			±0.1		±1			µA
I_{CC}	Quiescent supply current	1.65–4.3	V_{IN} = V_{CC} or GND			±0.05		±0.2		±1	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{1IN}, V_{2IN} = 1.65V		42	55					µA
			V_{1IN}, V_{2IN} = 1.80V		38	50					

1. ΔRON = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

3.3 AC electrical characteristics

Table 5. AC electrical characteristics (C_L = 35pF, R_L = 50Ω, t_r = t_f ≤5ns)

Symbol	Parameter	Test conditions		Value							Unit
		V_{CC}(V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay	1.65-1.95			0.45						ns
		2.3-2.7			0.40						
		3.0-3.3			0.30						
		3.6-4.3			0.30						
t_{ON}	TURN-ON time	1.65-1.95	V_S = 0.8V		70						ns
		2.3-2.7	V_S = 1.5V		30	60		75			
		3.0-3.3			25	50		60			
		3.6-4.3			25	50		60			
t_{OFF}	TURN-OFF time	1.65-1.95	V_S = 0.8		45						ns
		2.3-2.7	V_S = 1.5V		25	30		40			
		3.0-3.3			25	30		40			
		3.6-4.3			25	30		40			
t_D	Break before make time delay	1.65 – 1.95	C_L = 35pF R_L = 50Ω V_S = 1.5V								ns
		2.3 – 2.7		2	15						
		3.0 – 3.6		2	15						
		3.6 – 4.3		2	15						
Q	Charge Injection	1.65-1.95	C_L=100pF R_L = 1MΩ V_{GEN} = 0V R_{GEN} =0Ω		23						pC
		2.3 - 2.7			32						
		3.0 - 3.3			40						
		3.6 - 4.3			44						

3.4 Analog switch characteristics

Table 6. Analog switch characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test Conditions		Value							
		V_{CC}(V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		Unit
				Min.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
OIRR	Off Isolation (1)	1.65 - 4.3	V_S=1V_{RMS} f = 100kHz		-90						dB
Xtalk	Crosstalk	1.6 - 4.3	V_S=1V_{RMS} f = 100kHz		-76						dB
THD	Total harmonic distortion	3.0	R_L = 600Ω V_{IN} = 2V_{PP} f = 20Hz to 20 kHz		0.03						%
BW	-3dB Bandwidth	1.65 - 4.3	R_L = 50Ω		85						MHz
C_{IN}	Control pin input capacitance				7						pF
C_{Sn}	Sn port capacitance	3.3	f = 1MHz		35						pF
C_D	D port capacitance when switch is enabled	3.3	f = 1MHz		99						pF

1. Off Isolation = 20Log$_{10}$ (V_D/V_S), V_D = output, V_S = input at off switch.

3.5 Truth table

Table 7. Truth table

IN	Switch S1	Switch S2
H	ON	OFF (1)
L	OFF (1)	ON

1. High Impedance

4 Application circuits

Figure 3. ON Resistance

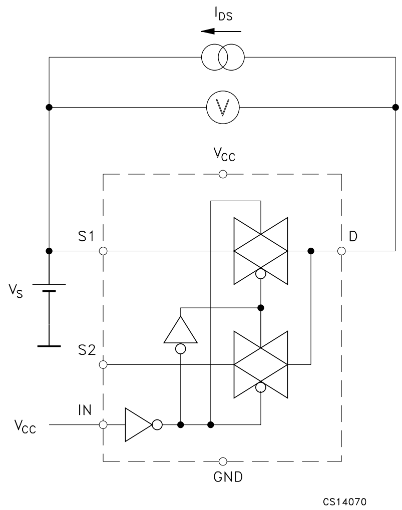


Figure 4. OFF Isolation

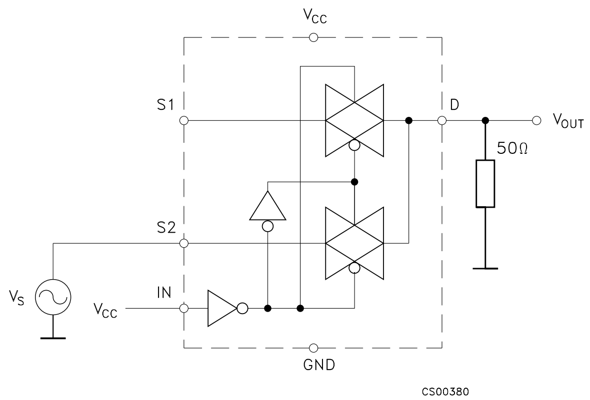


Figure 5. OFF Leakage

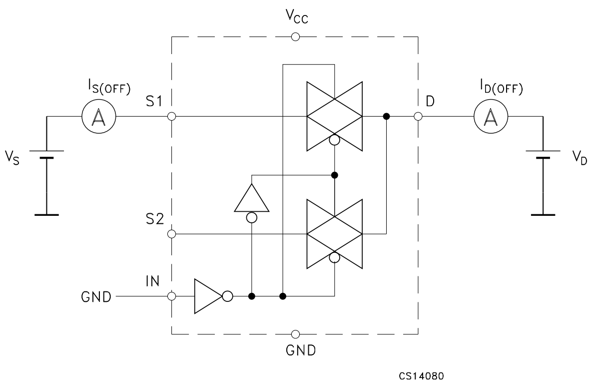


Figure 6. Bandwidth

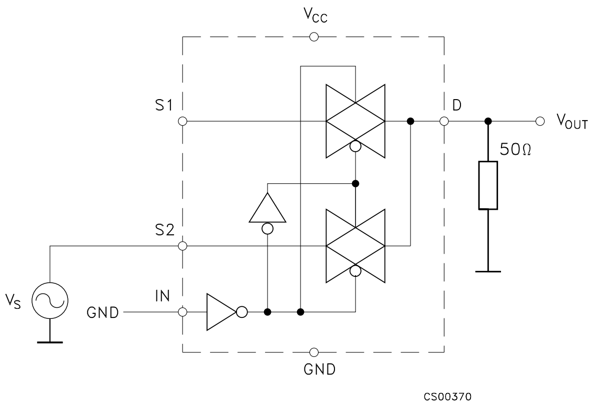


Figure 7. Channel to channel crosstalk

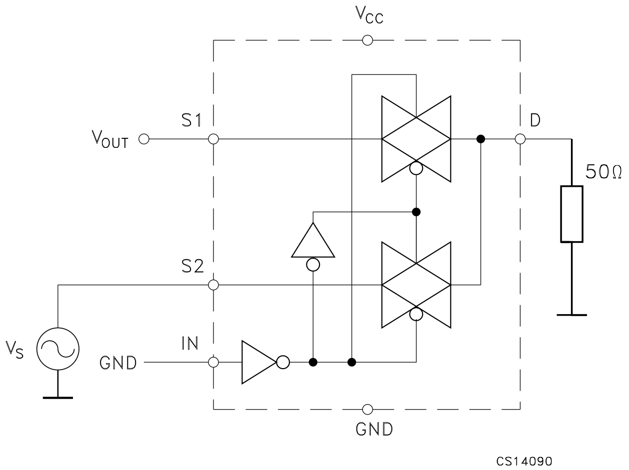
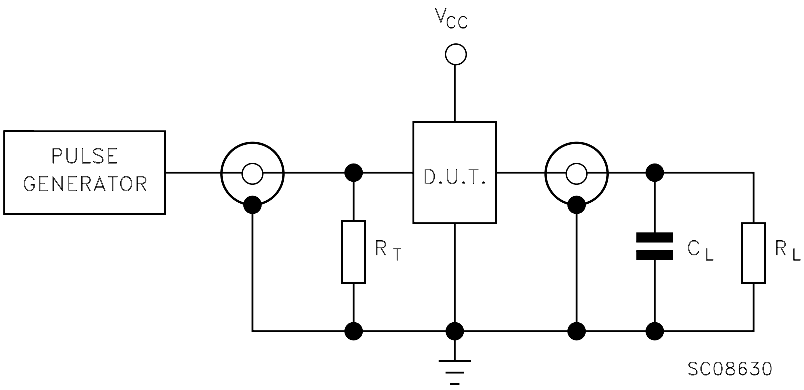


Figure 8. Test circuit



C_L = 5/35pF or equivalent (includes jig and probe capacitance)

R_L = 50Ω or equivalent

R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 9. Break-before-make time delay

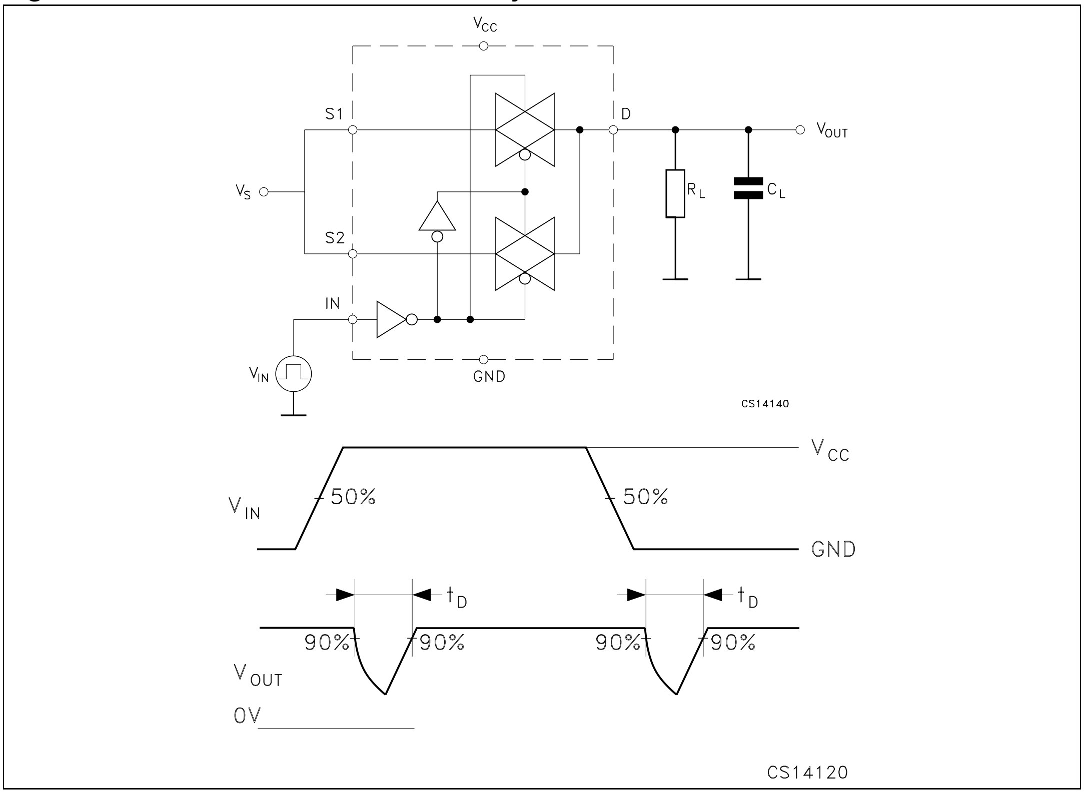


Figure 10. Switching time and charge injection
(V_{GEN} = 0V, R_{GEN} = 0Ω, R_L= 1MΩ, C_L = 100pF)

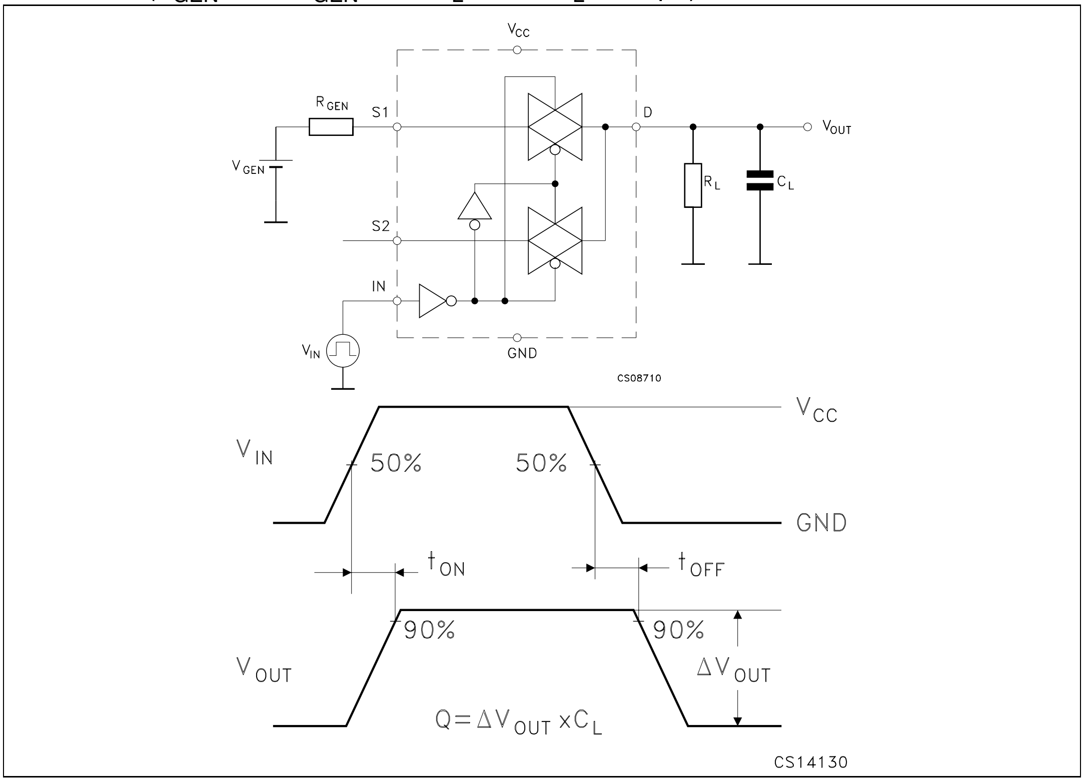
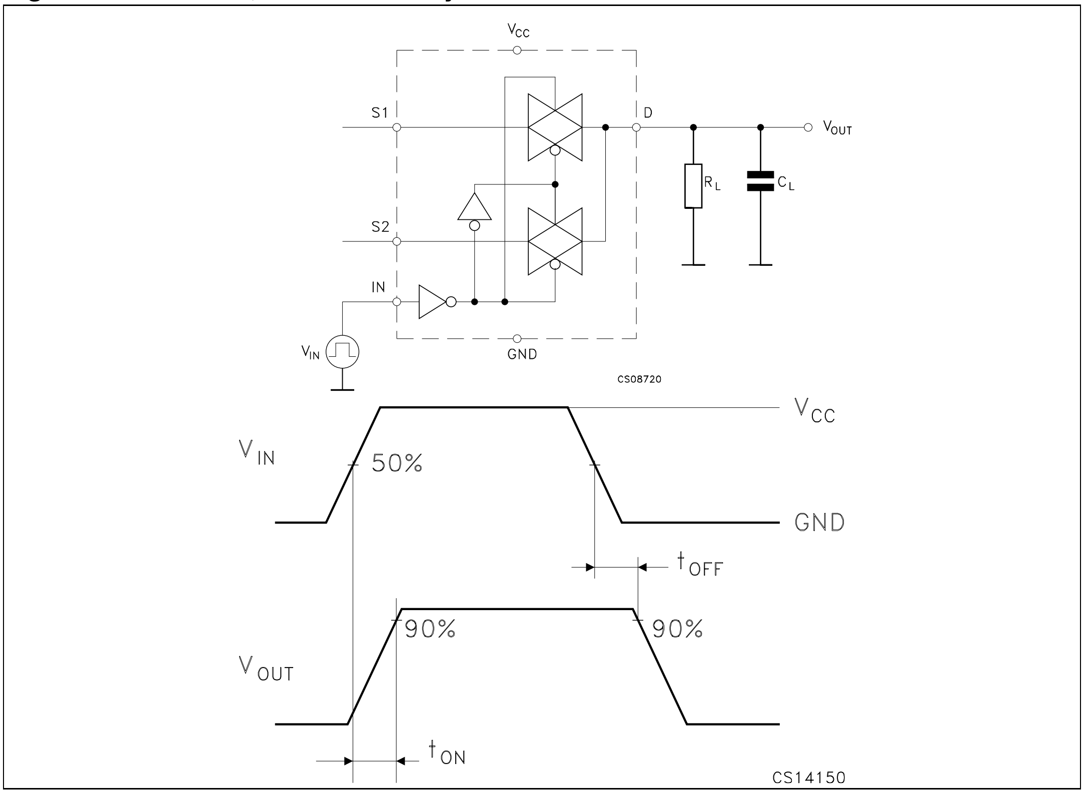


Figure 11. Turn ON, Turn OFF delay time



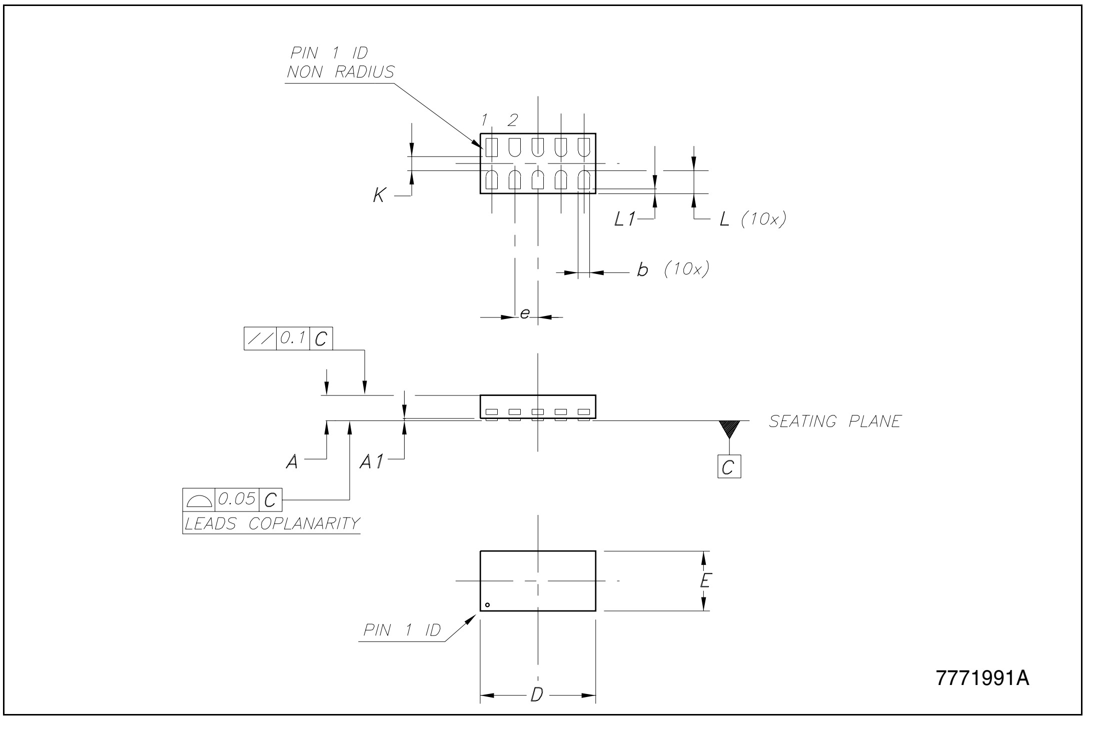
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 8. DFN10L (2.5mm x 1.3mm) Mechanical data

Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	19.7	21.7	23.6
A1	0	0.02	0.05	0	0.8	2.0
b	0.18	0.23	0.30	7.1	9.1	11.8
D	2.40	2.50	2.60	94.5	98.4	102.4
E	1.30	1.40	1.50	51.2	55.1	59.1
e		0.50			19.7	
K	0.20			7.9		
L	0.45	0.50	0.55	17.7	19.7	21.6
L1			0.15			5.9

Figure 12. Package dimensions



6 Revision history

Table 9. Revision history

Date	Revision	Changes
23-Feb-2006	1	Initial release.
01-Aug-2006	2	Final version, small text changes for entire document.