EN29PL064/032
64/32 Mbit (4/2 M x 16-Bit) CMOS 3.0 Volt- only, Simultaneous-Read/Write Flash Memory

Distinctive Characteristics

Architectural Advantages

- 64/32 Mbit Page Mode devices
- Page size of 4 words: Fast page read access from random locations within the page
- Single power supply operation
- Voltage range of 2.7V to 3.3V valid for MCP product
- Single Voltage, 2.7V to 3.6V for Read and Write operations
- Simultaneous Read/Write Operation
- Data can be continuously read from one bank while executing erase/ program functions in another bank
- Zero latency switching from write to read operations
- FlexBank Architecture(PL064/PL032)
- 4 separate banks, with up to two simultaneous operations per device
- Bank A:
  PL064 - 8 Mbit (4 Kw x 8 and 32 Kw x 15)
  PL032 - 4 Mbit (4 Kw x 8 and 32 Kw x 7)
- Bank B:
  PL064 - 24 Mbit (32 Kw x 48)
  PL032 - 12 Mbit (32 Kw x 24)
- Bank C:
  PL064 - 24 Mbit (32 Kw x 48)
  PL032 - 12 Mbit (32 Kw x 24)
- Bank D:
  PL064 - 8 Mbit (4 Kw x 8 and 32 Kw x 15)
  PL032 - 4 Mbit (4 Kw x 8 and 32 Kw x 7)
- Secured Silicon Sector region
- Up to 64 customer-lockable words
- Both top and bottom boot blocks in one device
- Data Retention: 20 years typical
- Cycling Endurance: 100K cycles per sector typical

Performance Characteristics

- High Performance
- Page access times as fast as 25 ns
- Random access times as fast as 70 ns
- 32-word/64-byte write buffer reduces overall programming time for multiple-word updates
- Power consumption (typical values at 10 MHz)
- 45 mA active read current
- 17 mA program/erase current
- 0.2 µA typical standby mode current

Software Features

- Software command-set compatible with JEDEC 42.4 standard
- CFI (Common Flash Interface) compliant
- Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend / Erase Resume
- Suspends an erase operation to allow read or program operations in other sectors of same bank
- Program Suspend / Program Resume
- Suspends a program operation to allow read operation from sectors other than the one being programmed
- Unlock Bypass Program command
- Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/Busy# pin (RY/BY#)
- Provides a hardware method of detecting program or erase cycle completion
- Hardware reset pin (RESET#)
- Hardware method to reset the device to reading array data
- WP#/ ACC (Write Protect/Acceleration) input
- At V_{IL}, hardware level protection for the first and last two 4K word sectors.
- At V_{IH}, allows removal of sector protection
- At V_{HH}, provides accelerated programming in a factory setting
- Persistent Sector Protection
- A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
- Sectors can be locked and unlocked in-system at V_{CC} level
- Package options
- 56-ball Fine Pitch BGA
- 48-ball Fine pitch BGA
- 48-pin TSOP-1

GENERAL DESCRIPTION

The PL064/PL032 is a 64/32 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 4/2 Mwords. The devices are offered in the following packages:

– 7 mm x 9 mm, 56-Ball Fine-pitch BGA standalone (PL064/PL032)
– 8 mm x 6 mm, 48-ball Fine-pitch BGA standalone (PL032)
– 48-pin TSOP (PL064/PL032)

The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 11.0 volt V_{PP} is not required for write or erase operations.

The device offers fast page access times of 25 ns, with corresponding random access times of 70 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

1. Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.
The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Bank	PL064 Sectors	PL032 Sectors
A	8 Mbit (4 Kw x 8 and 32 Kw x 15)	4 Mbit (4 Kw x 8 and 32 Kw x 7)
B	24 Mbit (32 Kw x 48)	12 Mbit (32 Kw x 24)
C	24 Mbit (32 Kw x 48)	12 Mbit (32 Kw x 24)
D	8 Mbit (4 Kw x 8 and 32 Kw x 15)	4 Mbit (4 Kw x 8 and 32 Kw x 7)

1.1 Page Mode Features

The page size is 4 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

1.2 Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **Program Suspend/Program Resume** feature enables the user to hold the program operation to read data from any sector that is not selected for programming. If a read is needed from the Secured Silicon Sector area, Persistent Protection area, or the CFI area, after a program suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

2. Ordering Information

EN29PL064 - 70 T I P

PACKAGING CONTENT
(Blank) = Conventional
P = Pb Free

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
T = 48-pin TSOP
B = 48-Ball Fine Pitch Ball Grid Array (FBGA)
0.80mm pitch, 6mm x 8mm package
C =56-Ball Fine Pitch Ball Grid Array (FBGA)
0.80mm pitch, 7mm x 9mm package

SPEED

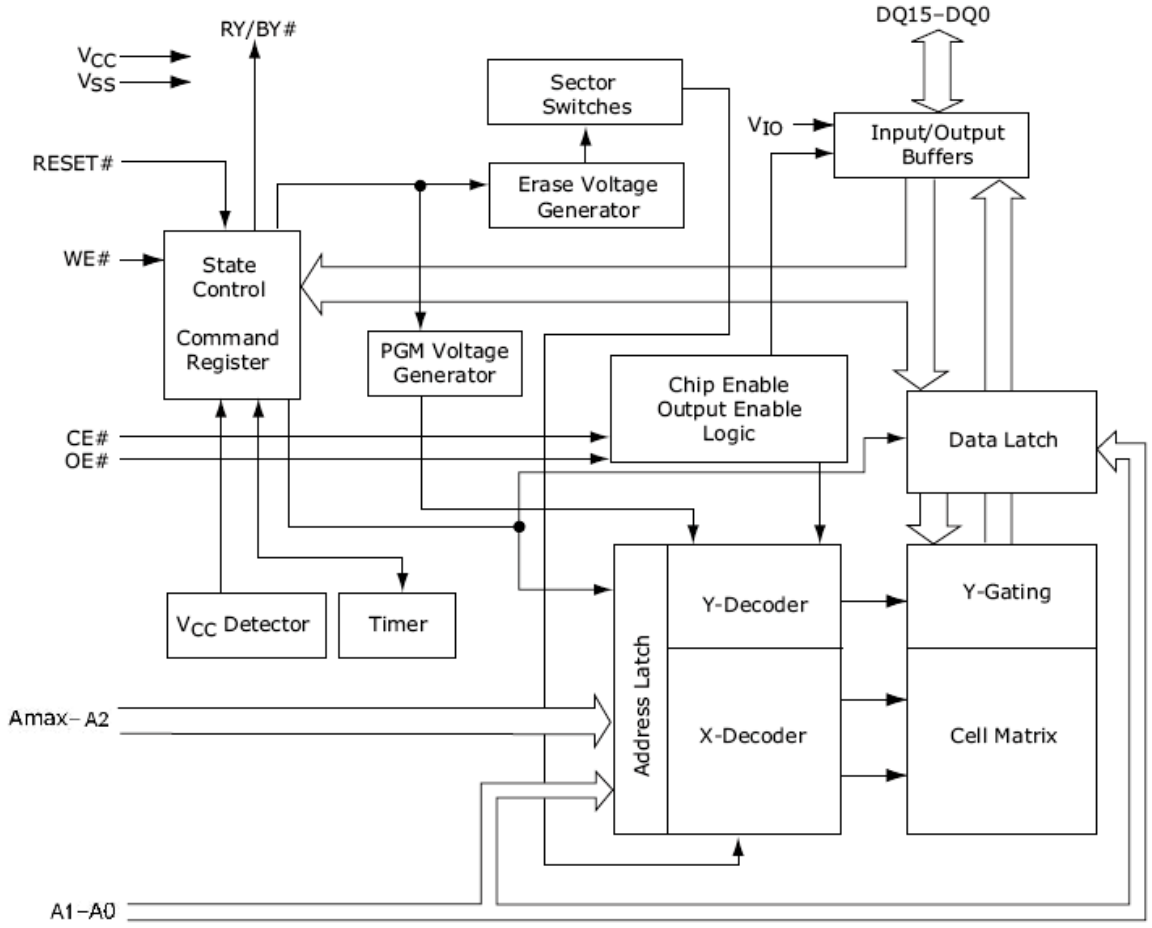
70 = 70ns

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
29PL = FLASH, 3.0V Read Program Erase,
Simultaneous-Read/Write, Page-Mode
064 = 64 Megabit (4 M x 16-Bit)
032 = 32 Megabit (2 M x 16-Bit)

3. Product Selector Guide

Part Number		EN29PL032 / EN29PL064
Speed Option	V_{CC} = 2.7 V – 3.6 V	70
Max Access Time, ns (t_{ACC})		70
Max CE# Access , ns (t_{CE})		
Max Page Access, ns (t_{PACC})		25
Max OE# Access, ns (t_{OE})		

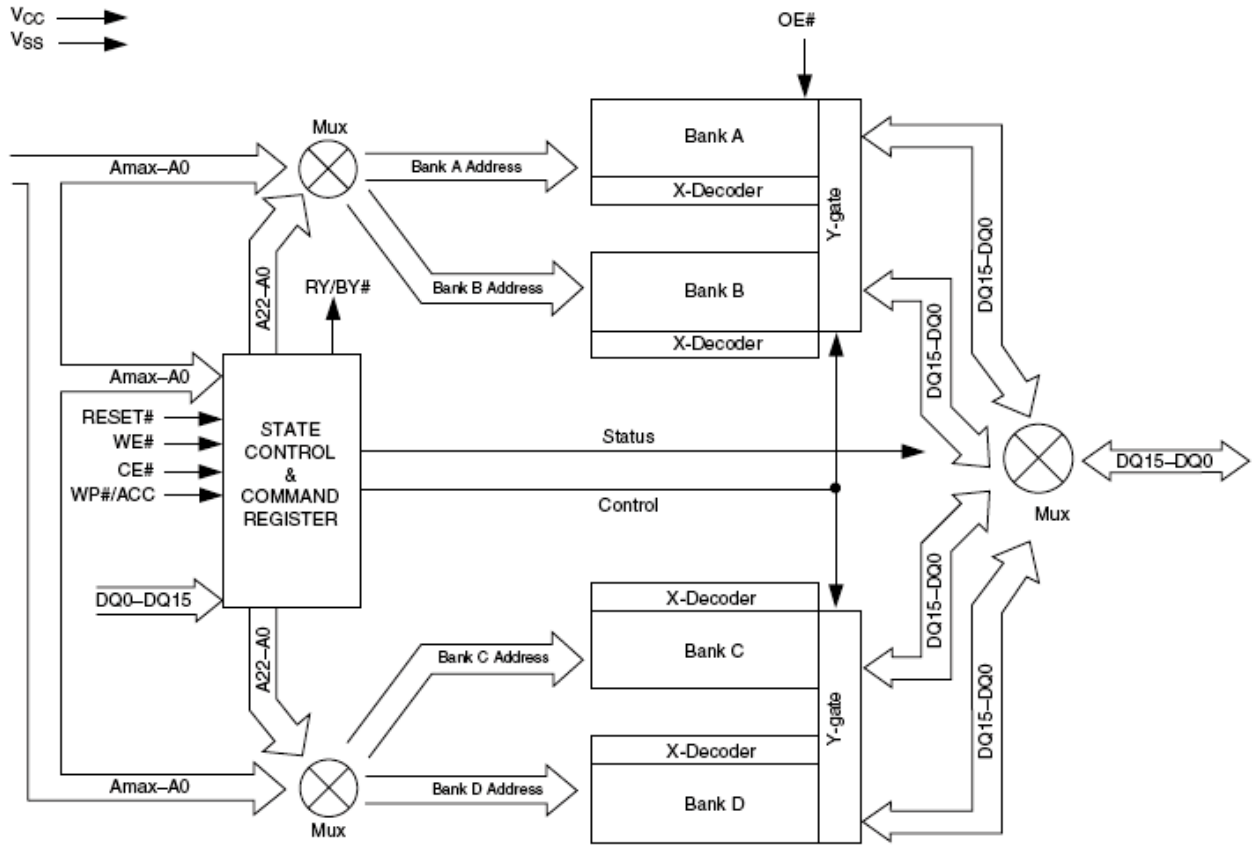
4. BLOCK DIAGRAM



Notes

1. *RY/BY# is an open drain output.*
2. *Amax = A21 (PL064), A20 (PL032)*

5. Simultaneous Read/Write Block Diagram

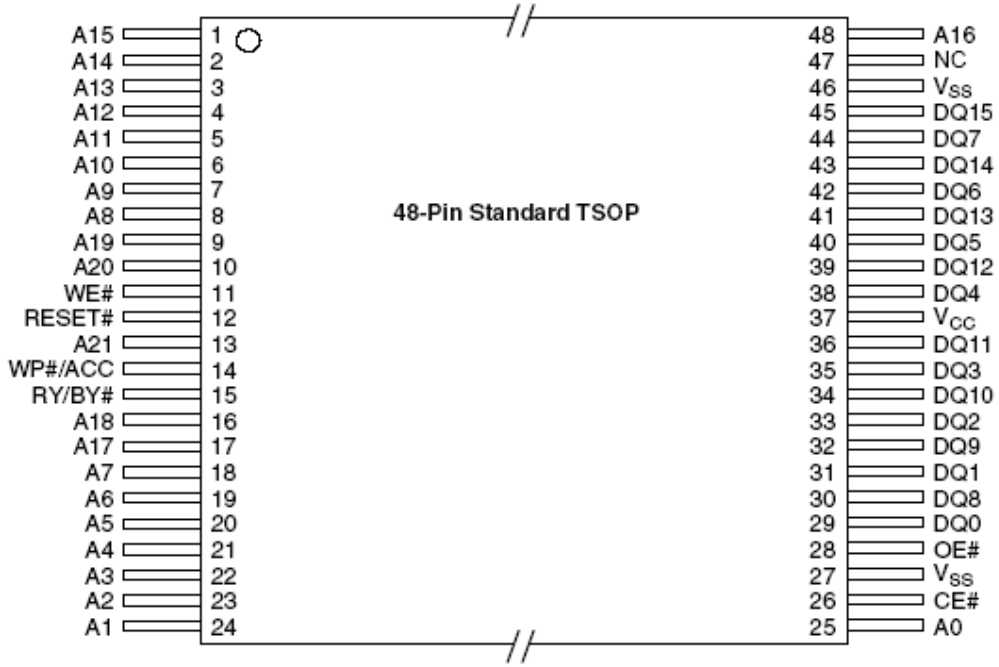


Note

Amax = A21 (PL064), A20 (PL032)

6. Connection Diagrams

Figure 6.1 48-pin TSOP



Note : PL032: pin 13 (A21) = NC

Figure 6.2 48-Ball Fine-Pitch BGA, Top View, Balls Facing Down (PL032)

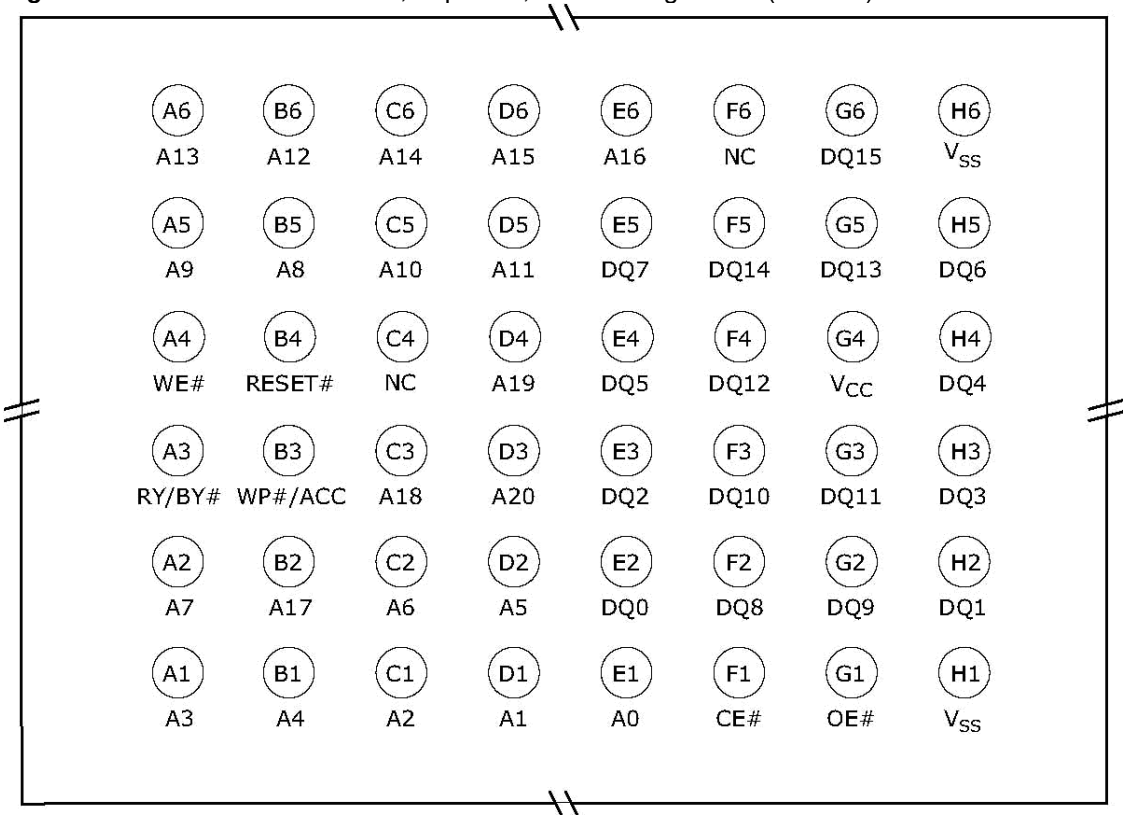
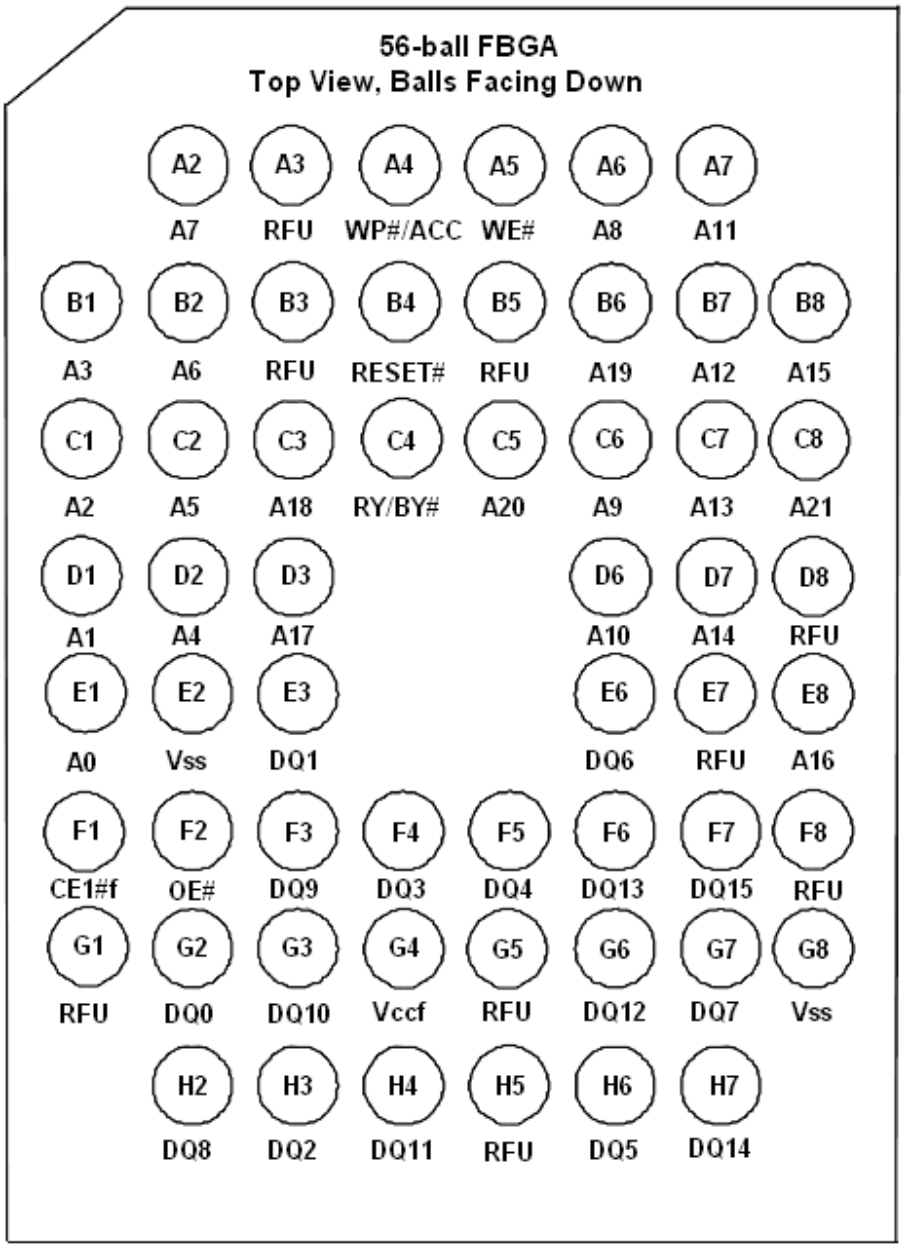


Figure 6.3 56-Ball Fine-Pitch BGA, Top View, Balls Facing Down



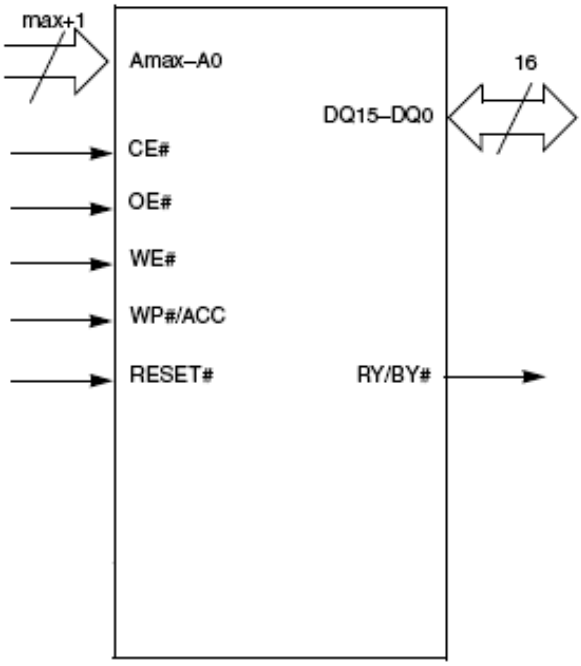
Note : PL032: C8 (A21) = NC
RFU = Reserved for Future Use

7. Pin Description

Amax–A0	Address bus
DQ15–DQ0	16-bit data inputs/outputs/float
CE#	Chip Enable Inputs
OE#	Output Enable Input
WE#	Write Enable
V_{SS}	Device Ground
NC	Pin Not Connected Internally
RY/BY#	Ready/Busy output and open drain. When RY/BY#= V_{IH}, the device is ready to accept read operations and commands. When RY/ BY#= V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
WP#/ACC	Write Protect/Acceleration Input. When WP#/ACC= V_{IL}, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP#/ACC= V_{IH}, these sector are unprotected unless the PPB is programmed. When WP#/ACC= 11V, program and erase operations are accelerated.
V_{CC}	Chip Power Supply (2.7 V to 3.6 V)
RESET#	Hardware Reset Pin

Note
Amax = A21 (PL064), A20 (PL032)

8. Logic Symbol



9. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 9.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 9.1 Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Amax–A0)	DQ15–DQ0
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write	L	H	L	H	X (Note 2)	A_{IN}	D_{IN}
Standby	Vcc±0.3 V	X	X	Vcc ±0.3 V	X (Note 2)	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 10.5–11.5 V, V_{HH} = 8.5–9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes
1. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See High Voltage Sector Protection*
2. *WP#/ACC must be high when writing to upper two and lower two sectors.*

9.1 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins. CE# is the power control. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to Table 21.3 for timing specifications and to Figure 20.3 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

9.1.1 Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

9.1.2 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A2 select a 4 word page, and address bits A1–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted (=V_{IH}), the reassertion of CE# for subsequent access has access time of t_{ACC} or t_{CE}. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping Amax–A2 constant and changing A1–A0 to select the specific word within that page.

Table 9.2 Page Select

Word	A1	A0
Word 0	0	0
Word 1	0	1
Word 2	1	0
Word 3	1	1

9.2 Simultaneous Read/Write Operation

In addition to the conventional features (read, program, erase-suspend read, erase-suspend program, and program-suspend read), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (PL064: A21–A19, PL032: A20–A18) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 9.3 Bank Select

Bank	PL064: A21–A19, PL032: A20–A18
Bank A	000
Bank B	001, 010, 011
Bank C	100, 101, 110
Bank D	111

9.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. *Word Program Command Sequence* has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector or the entire device. Table 9.3 indicates the set of address

space that each sector occupies. A “bank address” is the set of address bits required to uniquely select a bank. Similarly, a “sector address” refers to the address bits required to uniquely select a sector. *Command Definitions* has details on erasing a sector or the entire chip, or suspending / resuming the erase operation.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. See the timing specification tables and timing diagrams in section *Reset* for write operations.

9.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to V_{CC} when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

9.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Table 9.6, *Secured Silicon Sector Addresses* and *Autoselect Command Sequence* for more information.

9.4 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in *DC Characteristics* represents the CMOS standby current specification.

9.5 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. I_{CC5} in *DC Characteristics* represents the automatic sleep mode current specification.

9.6 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the tables in *AC Characteristic* for RESET# parameters and to Figure 20.5 for the timing diagram.

9.7 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

Table 9.4 PL064 Sector Architecture (Sheet 1 of 4)

Bank	Sector	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank A	SA0	0000000000	4	000000h–000FFFh
	SA1	0000000001	4	001000h–001FFFh
	SA2	0000000010	4	002000h–002FFFh
	SA3	0000000011	4	003000h–003FFFh
	SA4	0000000100	4	004000h–004FFFh
	SA5	0000000101	4	005000h–005FFFh
	SA6	0000000110	4	006000h–006FFFh
	SA7	0000000111	4	007000h–007FFFh
	SA8	0000001XXX	32	008000h–00FFFFh
	SA9	0000010XXX	32	010000h–017FFFh
	SA10	0000011XXX	32	018000h–01FFFFh
	SA11	0000100XXX	32	020000h–027FFFh
	SA12	0000101XXX	32	028000h–02FFFFh
	SA13	0000110XXX	32	030000h–037FFFh
	SA14	0000111XXX	32	038000h–03FFFFh
	SA15	0001000XXX	32	040000h–047FFFh
	SA16	0001001XXX	32	048000h–04FFFFh
	SA17	0001010XXX	32	050000h–057FFFh
	SA18	0001011XXX	32	058000h–05FFFFh
	SA19	0001100XXX	32	060000h–067FFFh
	SA20	0001101XXX	32	068000h–06FFFFh
	SA21	0001110XXX	32	070000h–077FFFh
	SA22	0001111XXX	32	078000h–07FFFFh

Table 9.4 PL064 Sector Architecture (Sheet 2 of 4)

Bank	Sector	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank B	SA23	0010000XXX	32	080000h–087FFFh
	SA24	0010001XXX	32	088000h–08FFFFh
	SA25	0010010XXX	32	090000h–097FFFh
	SA26	0010011XXX	32	098000h–09FFFFh
	SA27	0010100XXX	32	0A0000h–0A7FFFh
	SA28	0010101XXX	32	0A8000h–0AFFFFh
	SA29	0010110XXX	32	0B0000h–0B7FFFh
	SA30	0010111XXX	32	0B8000h–0BFFFFh
	SA31	0011000XXX	32	0C0000h–0C7FFFh
	SA32	0011001XXX	32	0C8000h–0CFFFFh
	SA33	0011010XXX	32	0D0000h–0D7FFFh
	SA34	0011011XXX	32	0D8000h–0DFFFFh
	SA35	0011100XXX	32	0E0000h–0E7FFFh
	SA36	0011101XXX	32	0E8000h–0EFFFFh
	SA37	0011110XXX	32	0F0000h–0F7FFFh
	SA38	0011111XXX	32	0F8000h–0FFFFFh
	SA39	0100000XXX	32	100000h–107FFFh
	SA40	0100001XXX	32	108000h–10FFFFh
	SA41	0100010XXX	32	110000h–117FFFh
	SA42	0100011XXX	32	118000h–11FFFFh
	SA43	0100100XXX	32	120000h–127FFFh
	SA44	0100101XXX	32	128000h–12FFFFh
	SA45	0100110XXX	32	130000h–137FFFh
	SA46	0100111XXX	32	138000h–13FFFFh
	SA47	0101000XXX	32	140000h–147FFFh
	SA48	0101001XXX	32	148000h–14FFFFh
	SA49	0101010XXX	32	150000h–157FFFh
	SA50	0101011XXX	32	158000h–15FFFFh
	SA51	0101100XXX	32	160000h–167FFFh
	SA52	0101101XXX	32	168000h–16FFFFh
	SA53	0101110XXX	32	170000h–177FFFh
	SA54	0101111XXX	32	178000h–17FFFFh
	SA55	0110000XXX	32	180000h–187FFFh
	SA56	0110001XXX	32	188000h–18FFFFh
	SA57	0110010XXX	32	190000h–197FFFh
	SA58	0110011XXX	32	198000h–19FFFFh
	SA59	0110100XXX	32	1A0000h–1A7FFFh
	SA60	0110101XXX	32	1A8000h–1AFFFFh
	SA61	0110110XXX	32	1B0000h–1B7FFFh
	SA62	0110111XXX	32	1B8000h–1BFFFFh
	SA63	0111000XXX	32	1C0000h–1C7FFFh
	SA64	0111001XXX	32	1C8000h–1CFFFFh
	SA65	0111010XXX	32	1D0000h–1D7FFFh
	SA66	0111011XXX	32	1D8000h–1DFFFFh
	SA67	0111100XXX	32	1E0000h–1E7FFFh
	SA68	0111101XXX	32	1E8000h–1EFFFFh
	SA69	0111110XXX	32	1F0000h–1F7FFFh
	SA70	0111111XXX	32	1F8000h–1FFFFFh

Table 9.4 PL064 Sector Architecture (Sheet 3 of 4)

Bank	Sector	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank C	SA71	1000000XXX	32	200000h–207FFFh
	SA72	1000001XXX	32	208000h–20FFFFh
	SA73	1000010XXX	32	210000h–217FFFh
	SA74	1000011XXX	32	218000h–21FFFFh
	SA75	1000100XXX	32	220000h–227FFFh
	SA76	1000101XXX	32	228000h–22FFFFh
	SA77	1000110XXX	32	230000h–237FFFh
	SA78	1000111XXX	32	238000h–23FFFFh
	SA79	1001000XXX	32	240000h–247FFFh
	SA80	1001001XXX	32	248000h–24FFFFh
	SA81	1001010XXX	32	250000h–257FFFh
	SA82	1001011XXX	32	258000h–25FFFFh
	SA83	1001100XXX	32	260000h–267FFFh
	SA84	1001101XXX	32	268000h–26FFFFh
	SA85	1001110XXX	32	270000h–277FFFh
	SA86	1001111XXX	32	278000h–27FFFFh
	SA87	1010000XXX	32	280000h–287FFFh
	SA88	1010001XXX	32	288000h–28FFFFh
	SA89	1010010XXX	32	290000h–297FFFh
	SA90	1010011XXX	32	298000h–29FFFFh
	SA91	1010100XXX	32	2A0000h–2A7FFFh
	SA92	1010101XXX	32	2A8000h–2AFFFFh
	SA93	1010110XXX	32	2B0000h–2B7FFFh
	SA94	1010111XXX	32	2B8000h–2BFFFFh
	SA95	1011000XXX	32	2C0000h–2C7FFFh
	SA96	1011001XXX	32	2C8000h–2CFFFFh
	SA97	1011010XXX	32	2D0000h–2D7FFFh
	SA98	1011011XXX	32	2D8000h–2DFFFFh
	SA99	1011100XXX	32	2E0000h–2E7FFFh
	SA100	1011101XXX	32	2E8000h–2EFFFFh
	SA101	1011110XXX	32	2F0000h–2F7FFFh
	SA102	1011111XXX	32	2F8000h–2FFFFFh
	SA103	1100000XXX	32	300000h–307FFFh
	SA104	1100001XXX	32	308000h–30FFFFh
	SA105	1100010XXX	32	310000h–317FFFh
	SA106	1100011XXX	32	318000h–31FFFFh
	SA107	1100100XXX	32	320000h–327FFFh
	SA108	1100101XXX	32	328000h–32FFFFh
	SA109	1100110XXX	32	330000h–337FFFh
	SA110	1100111XXX	32	338000h–33FFFFh
	SA111	1101000XXX	32	340000h–347FFFh
	SA112	1101001XXX	32	348000h–34FFFFh
	SA113	1101010XXX	32	350000h–357FFFh
	SA114	1101011XXX	32	358000h–35FFFFh
	SA115	1101100XXX	32	360000h–367FFFh
	SA116	1101101XXX	32	368000h–36FFFFh
	SA117	1101110XXX	32	370000h–377FFFh
	SA118	1101111XXX	32	378000h–37FFFFh

Table 9.4 PL064 Sector Architecture (Sheet 4 of 4)

Bank	Sector	Sector Address (A21-A12)	Sector Size (Kwords)	Address Range (x16)
Bank D	SA119	1110000XXX	32	380000h–387FFFh
	SA120	1110001XXX	32	388000h–38FFFFh
	SA121	1110010XXX	32	390000h–397FFFh
	SA122	1110011XXX	32	398000h–39FFFFh
	SA123	1110100XXX	32	3A0000h–3A7FFFh
	SA124	1110101XXX	32	3A8000h–3AFFFFh
	SA125	1110110XXX	32	3B0000h–3B7FFFh
	SA126	1110111XXX	32	3B8000h–3BFFFFh
	SA127	1111000XXX	32	3C0000h–3C7FFFh
	SA128	1111001XXX	32	3C8000h–3CFFFFh
	SA129	1111010XXX	32	3D0000h–3D7FFFh
	SA130	1111011XXX	32	3D8000h–3DFFFFh
	SA131	1111100XXX	32	3E0000h–3E7FFFh
	SA132	1111101XXX	32	3E8000h–3EFFFFh
	SA133	1111110XXX	32	3F0000h–3F7FFFh
	SA134	1111111000	4	3F8000h–3F8FFFh
	SA135	1111111001	4	3F9000h–3F9FFFh
	SA136	1111111010	4	3FA000h–3FAFFFh
	SA137	1111111011	4	3FB000h–3FBFFFh
	SA138	1111111100	4	3FC000h–3FCFFFh
	SA139	1111111101	4	3FD000h–3FDFFFh
	SA140	1111111110	4	3FE000h–3FEFFFh
	SA141	1111111111	4	3FF000h–3FFFFFh

Table 9.5 PL032 Sector Architecture (Sheet 1 of 2)

Bank	Sector	Sector Address (A20-A12)	Sector Size (Kwords)	Address Range (x16)
Bank A	SA0	000000000	4	000000h–000FFFh
	SA 1	000000001	4	001000h–001FFFh
	SA 2	000000010	4	002000h–002FFFh
	SA 3	000000011	4	003000h–003FFFh
	SA 4	000000100	4	004000h–004FFFh
	SA 5	000000101	4	005000h–005FFFh
	SA 6	000000110	4	006000h–006FFFh
	SA 7	000000111	4	007000h–007FFFh
	SA 8	000001XXX	32	008000h–00FFFFh
	SA 9	000010XXX	32	010000h–017FFFh
	SA 10	000011XXX	32	018000h–01FFFFh
	SA 11	000100XXX	32	020000h–027FFFh
	SA 12	000101XXX	32	028000h–02FFFFh
	SA 13	000110XXX	32	030000h–037FFFh
	SA 14	000111XXX	32	038000h–03FFFFh
Bank B	SA 15	001000XXX	32	040000h–047FFFh
	SA16	001001XXX	32	048000h–04FFFFh
	SA 17	001010XXX	32	050000h–057FFFh
	SA 18	001011XXX	32	058000h–05FFFFh
	SA 19	001100XXX	32	060000h–067FFFh
	SA 20	001101XXX	32	068000h–06FFFFh
	SA 21	001110XXX	32	070000h–077FFFh
	SA 22	001111XXX	32	078000h–07FFFFh
	SA 23	010000XXX	32	080000h–087FFFh
	SA 24	010001XXX	32	088000h–08FFFFh
	SA25	010010XXX	32	090000h–097FFFh
	SA 26	010011XXX	32	098000h–09FFFFh
	SA 27	010100XXX	32	0A0000h–0A7FFFh
	SA 28	010101XXX	32	0A8000h–0AFFFFh
	SA 29	010110XXX	32	0B0000h–0B7FFFh
	SA 30	010111XXX	32	0B8000h–0BFFFFh
	SA 31	011000XXX	32	0C0000h–0C7FFFh
	SA 32	011001XXX	32	0C8000h–0CFFFFh
	SA 33	011010XXX	32	0D0000h–0D7FFFh
	SA 34	011011XXX	32	0D8000h–0DFFFFh
	SA 35	011100XXX	32	0E0000h–0E7FFFh
	SA 36	011101XXX	32	0E8000h–0EFFFFh
	SA 37	011110XXX	32	0F0000h–0F7FFFh
	SA 38	011111XXX	32	0F8000h–0FFFFFh

Table 9.5 PL032 Sector Architecture (Sheet 2 of 2)

Bank	Sector	Sector Address (A20-A12)	Sector Size (Kwords)	Address Range (x16)
Bank C	SA39	100000XXX	32	100000h–107FFFh
	SA40	100001XXX	32	108000h–10FFFFh
	SA41	100010XXX	32	110000h–117FFFh
	SA42	100011XXX	32	118000h–11FFFFh
	SA43	100100XXX	32	120000h–127FFFh
	SA44	100101XXX	32	128000h–12FFFFh
	SA45	100110XXX	32	130000h–137FFFh
	SA46	100111XXX	32	138000h–13FFFFh
	SA47	101000XXX	32	140000h–147FFFh
	SA48	101001XXX	32	148000h–14FFFFh
	SA49	101010XXX	32	150000h–157FFFh
	SA50	101011XXX	32	158000h–15FFFFh
	SA51	101100XXX	32	160000h–167FFFh
	SA52	101101XXX	32	168000h–16FFFFh
	SA53	101110XXX	32	170000h–177FFFh
	SA54	101111XXX	32	178000h–17FFFFh
	SA55	110000XXX	32	180000h–187FFFh
	SA56	110001XXX	32	188000h–18FFFFh
	SA57	110010XXX	32	190000h–197FFFh
	SA58	110011XXX	32	198000h–19FFFFh
	SA59	110100XXX	32	1A0000h–1A7FFFh
	SA60	110101XXX	32	1A8000h–1AFFFFh
	SA61	110110XXX	32	1B0000h–1B7FFFh
	SA62	110111XXX	32	1B8000h–1BFFFFh
Bank D	SA63	111000XXX	32	1C0000h–1C7FFFh
	SA64	111001XXX	32	1C8000h–1CFFFFh
	SA65	111010XXX	32	1D0000h–1D7FFFh
	SA66	111011XXX	32	1D8000h–1DFFFFh
	SA67	111100XXX	32	1E0000h–1E7FFFh
	SA68	111101XXX	32	1E8000h–1EFFFFh
	SA69	111110XXX	32	1F0000h–1F7FFFh
	SA70	111111000	4	1F8000h–1F8FFFh
	SA71	111111001	4	1F9000h–1F9FFFh
	SA72	111111010	4	1FA000h–1FAFFFh
	SA73	111111011	4	1FB000h–1FBFFFh
	SA74	111111100	4	1FC000h–1FCFFFh
	SA75	111111101	4	1FD000h–1FDFFFh
	SA76	111111110	4	1FE000h–1FEFFFh
	SA77	111111111	4	1FF000h–1FFFFFh

Table 9.6 Secured Silicon Sector Addresses

	Sector Size	Address Range
Customer-Lockable Area	64 words	000040h-00007Fh

9.8 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 9.7. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 9.3). Table 9.7 show the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 15.1. *Note that if a Bank Address (BA) (on address bits PL064: A21–A19, PL032: A20–*A18*) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 15.1. This method does not require V_{ID}. Refer to the *Autoselect Command Sequence* for more information.

Table 9.7 Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	Amax to A12	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: Eon		L	L	H	BA	X	V_{ID}	H[1]	L	L	X	L	L	L	L	001Ch
								L								007Fh
Device ID	Read Cycle 1	L	L	H	BA	X	V_{ID}	X	L	L	L	L	L	L	H	227Eh
	Read Cycle 2	L										H	H	H	L	2202h (PL064) 220Ah (PL032)
	Read Cycle 3	L										H	H	H	H	2201h (PL064) 2201h (PL032)
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0001h (protected), 0000h (unprotected)
Secured Silicon Indicator Bit (DQ7, DQ6)		L	L	H	BA (See Note)	X	V_{ID}	X	X	L	X	L	L	H	H	DQ6=1 (customer locked)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care.

Note

1. A8=H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

When Polling the Secured Silicon indicator bit the Bank Address (BA) should be set within the address range 004000h-03FFFFh.

9.9 Selecting a Sector Protection Mode

Table 9.8 PL064 Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A21-A12	Sector/Sector Block Size
SA0	0000000000	4 Kwords
SA1	0000000001	4 Kwords
SA2	0000000010	4 Kwords
SA3	0000000011	4 Kwords
SA4	0000000100	4 Kwords
SA5	0000000101	4 Kwords
SA6	0000000110	4 Kwords
SA7	0000000111	4 Kwords
SA8	0000001XXX	32 Kwords
SA9	0000010XXX	32 Kwords
SA10	0000011XXX	32 Kwords
SA11-SA14	00001XXXXX	128 (4x32) Kwords
SA15-SA18	00010XXXXX	128 (4x32) Kwords
SA19-SA22	00011XXXXX	128 (4x32) Kwords
SA23-SA26	00100XXXXX	128 (4x32) Kwords
SA27-SA30	00101XXXXX	128 (4x32) Kwords
SA31-SA34	00110XXXXX	128 (4x32) Kwords
SA35-SA38	00111XXXXX	128 (4x32) Kwords
SA39-SA42	01000XXXXX	128 (4x32) Kwords
SA43-SA46	01001XXXXX	128 (4x32) Kwords
SA47-SA50	01010XXXXX	128 (4x32) Kwords
SA51-SA54	01011XXXXX	128 (4x32) Kwords
SA55-SA58	01100XXXXX	128 (4x32) Kwords
SA59-SA62	01101XXXXX	128 (4x32) Kwords
SA63-SA66	01110XXXXX	128 (4x32) Kwords
SA67-SA70	01111XXXXX	128 (4x32) Kwords
SA71-SA74	10000XXXXX	128 (4x32) Kwords
SA75-SA78	10001XXXXX	128 (4x32) Kwords
SA79-SA82	10010XXXXX	128 (4x32) Kwords
SA83-SA86	10011XXXXX	128 (4x32) Kwords
SA87-SA90	10100XXXXX	128 (4x32) Kwords
SA91-SA94	10101XXXXX	128 (4x32) Kwords
SA95-SA98	10110XXXXX	128 (4x32) Kwords
SA99-SA102	10111XXXXX	128 (4x32) Kwords
SA103-SA106	11000XXXXX	128 (4x32) Kwords
SA107-SA110	11001XXXXX	128 (4x32) Kwords
SA111-SA114	11010XXXXX	128 (4x32) Kwords
SA115-SA118	11011XXXXX	128 (4x32) Kwords
SA119-SA122	11100XXXXX	128 (4x32) Kwords
SA123-SA126	11101XXXXX	128 (4x32) Kwords
SA127-SA130	11110XXXXX	128 (4x32) Kwords
SA131	1111100XXX	32 Kwords
SA132	1111101XXX	32 Kwords
SA133	1111110XXX	32 Kwords
SA134	1111111000	4 Kwords
SA135	1111111001	4 Kwords
SA136	1111111010	4 Kwords
SA137	1111111011	4 Kwords
SA138	1111111100	4 Kwords
SA139	1111111101	4 Kwords
SA140	1111111110	4 Kwords
SA141	1111111111	4 Kwords

The device is shipped with all sectors unprotected. Optional Eon programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See the Table 9.6 *Secured Silicon Sector Addresses* for details.

10. Sector Protection

The PL064, and PL032 features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

10.1 Persistent Sector Protection

A command sector protection method that replaces the old 11 V controlled protection method.

10.2 WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors SA0, SA1, SA140 and SA141. (PL064) / SA0, SA1, SA76 and SA77. (PL032)

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

10.3 Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. There are two one-time programmable nonvolatile bits that define which sector protection method will be used. The device is shipped with all sectors unprotected. Optional Eon's programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode* for details.

11. Persistent Sector Protection

The Persistent Sector Protection method replaces the 11 V controlled protection method in previous flash devices. This new method provides the sector protection states:
■ Persistently Locked—The sector is protected and cannot be changed.

To achieve these states, two types of "bits" are used:
■ Persistent Protection Bit
■ Persistent Protection Bit Lock

11.1 Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing sector PPBs over-erasure.

11.2 Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors SA0, SA1, SA140 and SA141. (PL064) / SA0, SA1, SA76 and SA77. (PL032). When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

For customers who are concerned about malicious viruses there is another level of security - the persistently locked state. To persistently protect a given sector or sector group, the PPBs associated with that sector need to be set to “1”. Once all PPBs are programmed to the desired settings, the PPB Lock should be set to “1”. Setting the PPB Lock automatically disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock “freezes” the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = V_{IL}.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the PPB, and PPB lock for a given sector can be verified by writing a PPB/ PPB lock verify command to the device. There is an alternative means of reading the protection status. Take RESET# to V_{IL} and hold WE# at V_{IH}. (The high voltage A9 Autoselect Mode also works for reading the status of the PPBs). Scanning the addresses (A18–A11) while (A6, A1, A0) = (0, 1, 0) will produce a logical ‘1” code at device output DQ0 for a protected sector or a “0” for an unprotected sector. In this mode, the other addresses are don’t cares. Address location with A1 = V_{IL} are reserved for autoselect manufacturer and device codes.

12. Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the upper two and lower two sectors without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed *High Voltage Sector Protection* method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

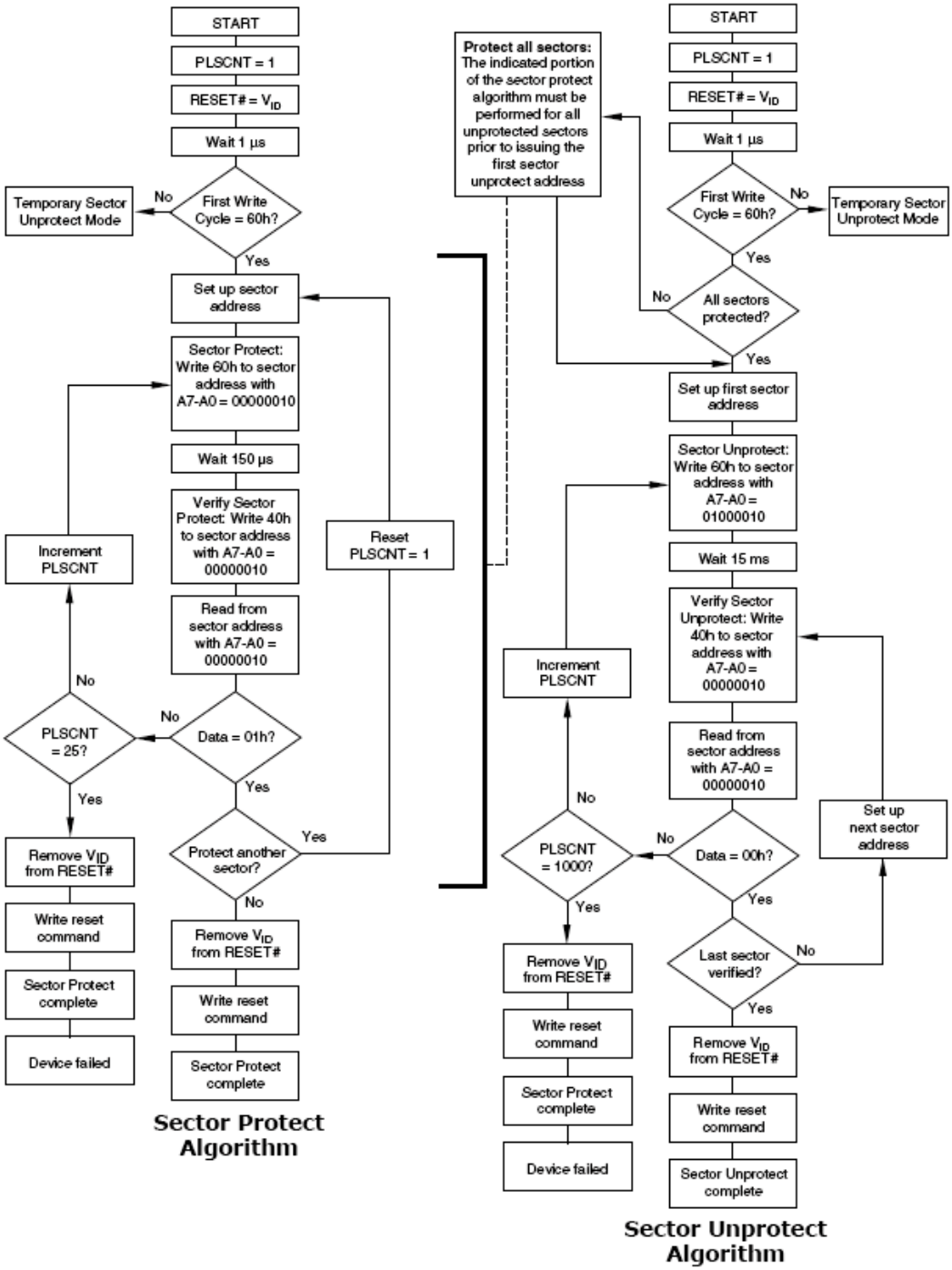
If the system asserts V_{IH} on the WP#/ACC pin, the device reverts the upper two and lower two sectors to whether they were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in the *High Voltage Sector Protection* .

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

13. High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 13.1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

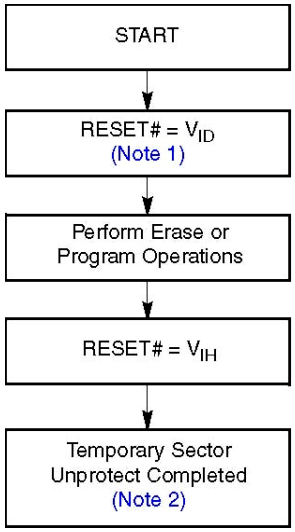
Figure 13.1 In-System Sector Protection/Sector Unprotection Algorithms



13.1 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 13.2 shows the algorithm, and Figure 21.1 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.

Figure 13.2 Temporary Sector Unprotect Operation



Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, upper two and lower two sectors will remain protected).*
2. *All previously protected sectors are protected once again*

13.2 Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The 64-word Secured Silicon sector is customer-lockable words that can be programmed and locked by the customer. The Secured Silicon sector is located at addresses 000040h-00007Fh. Indicator bit DQ6 is used to indicate the customer locked status of the part.

The system accesses the Secured Silicon Sector through a command sequence (see the *Enter/Exit Secured Silicon Sector Command Sequence*). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. Once the Enter SecSi Sector Command sequence has been entered, the standard array cannot be accessed until the Exit SecSi Sector command has been entered or the device has been reset. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

13.2.1 Customer-Lockable Area (64 words)

The customer-lockable area of the Secured Silicon Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The Secured Silicon Sector Customer-locked Indicator Bit (DQ6) is shipped as "0" and can be permanently locked to "1" by issuing the Secured Silicon Protection Bit Program Command. The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Sector.

The Customer-lockable Secured Silicon Sector area can be protected using one of the following procedures:

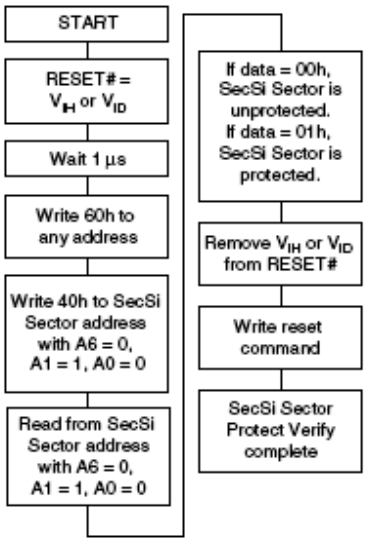
- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 13.1 , except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 13.3.
- Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

13.2.2 Secured Silicon Sector Protection Bits

The Secured Silicon Sector Protection Bits prevent programming of the Secured Silicon Sector memory area. Once set, the Secured Silicon Sector memory area contents are non-modifiable.

Figure 13.3 Secured Silicon Sector Protect Verify



13.3 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

13.3.1 Low V_{cc} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

13.3.2 Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on OE#, CE#, or WE# do not initiate a write cycle.

13.3.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

13.3.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

14. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 14.1 to Table 14.4. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 14.1 to Table 14.4. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact your local sales office for copies of these documents.

Table 14.1 CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 14.2 System Interface String

Addresses	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N µs
20h	0004h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for byte/word write 2^N times typical
24h	0005h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0004h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 14.3 Device Geometry Definition

Addresses	Data	Description
27h	0017h (PL064) 0016h (PL032)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0006h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h	007Dh (PL064) 003Dh (PL032)	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
32h 33h 34h	0000h 0000h 0001h	
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)

39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 14.4 Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0034h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	0008h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0002h	Sector Protect/Unprotect scheme 00h = High Voltage Sector Protection 01h = High Voltage + In-System Sector Protection 02h = HV + In-System Software Command Sector Protection
4Ah	0077h (PL064) 003Fh (PL032)	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV

Table 14.4 Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 01h = Both top and bottom boot with write protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
51h	0001h	Unlock Bypass 00 = Not Supported, 01 = Supported
52h	0007h	Secured Silicon Sector (Customer OTP Area) Size 2_N bytes
53h	000Fh	Hardware Reset Low Time-out during an embedded algorithm to read mode Maximum 2^N ns
54h	0009h	Hardware Reset Low Time-out not during an embedded algorithm to read mode Maximum 2^N ns
55h	0005h	Erase Suspend Latency Maximum 2^N µs
56h	0005h	Program Suspend Latency Maximum 2^N µs

57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0017h (PL064) 000Fh (PL032)	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0030h (PL064) 0018h (PL032)	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0030h (PL064) 0018h (PL032)	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	0017h (PL064) 000Fh (PL032)	Bank 4 Region Information X = Number of Sectors in Bank 4

15. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 15.1 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE# , whichever happens first. Refer to *AC Characteristic* for timing diagrams.

15.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/Erase Resume Commands* for more information.

After the device accepts a Program Suspend command, the corresponding bank enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same bank. See *Program Suspend/Program Resume Commands* for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, *Reset Command* , for more information.

See also *Requirements for Reading Array Data* for more information. The table *AC Characteristic* provides the read parameters, and Figure 16.2 shows the timing diagram.

15.2 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend and program-suspend-read mode if that bank was in Program Suspend).

15.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 15.1 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

15.4 Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 15.1 shows the address and data requirements for both command sequences. See also *Secured Silicon Sector Flash Memory Region* for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

15.5 Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 15.1 shows the address and data requirements for the program command sequence. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to *Write Operation Status* for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. Note that the Secured Silicon Sector, autoselect and CFI functions are unavailable when the Secured Silicon Sector is enabled.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

15.5.1 Unlock Bypass Command Sequence

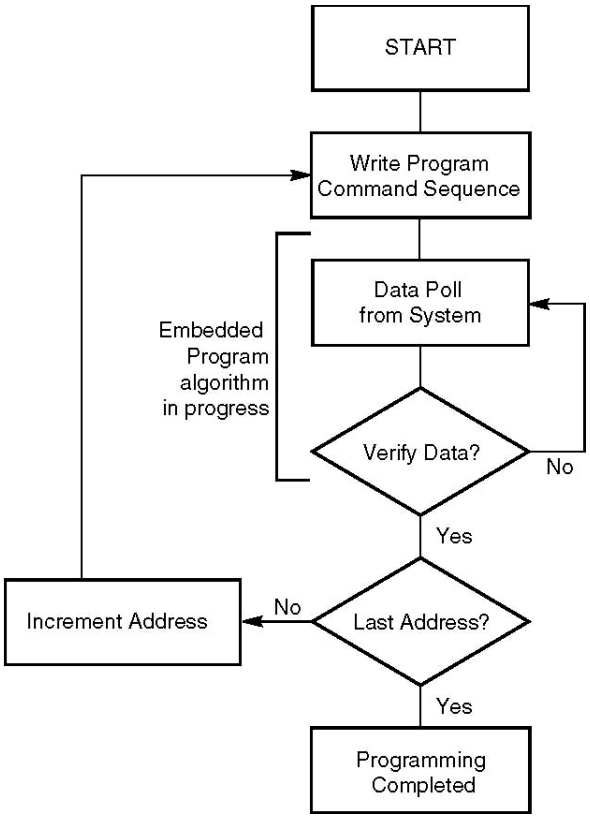
The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 15.1 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence.

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 15.1 illustrates the algorithm for the program operation. Refer to the table *Erase/Program Operations* for parameters, and Figure 20.6 for timing diagrams.

Figure 15.1 Program Operation



Note
See Table 15.1 for program command sequence.

15.6 Write Buffer Programming Operation

Write Buffer Programming allows the system to write a maximum of 32 words in one programming operation. The results in a faster effective word programming time than the standard "word" programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the starting address in which programming will occur. At this point, the system writes the number of " **word locations minus 1** " that will be loaded into the page buffer at the starting address in which programming will occur. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the "Program Buffer of Flash" confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. (NOTE: the number loaded = the number of locations to program minus 1. For example, if the system will program 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the "write-buffer-page" address. All subsequent address/data pairs **must** fall within the "selected-write-buffer-page".

The "write- buffer-page" is selected by using the addresses A_{max}– A_5

The "write- buffer-page" addresses **must be the same for all address/data pairs loaded into the write buffer.** (This means Write Buffer Programming **cannot** be performed across multiple "write-buffer-page". This also means that Write Buffer Programming **cannot** be performed across multiple sectors. If the system attempts to load programming data outside of the selected "write- buffer-page", the operation will ABORT.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pars into the write buffer. Write buffer locations may be loaded in any order.

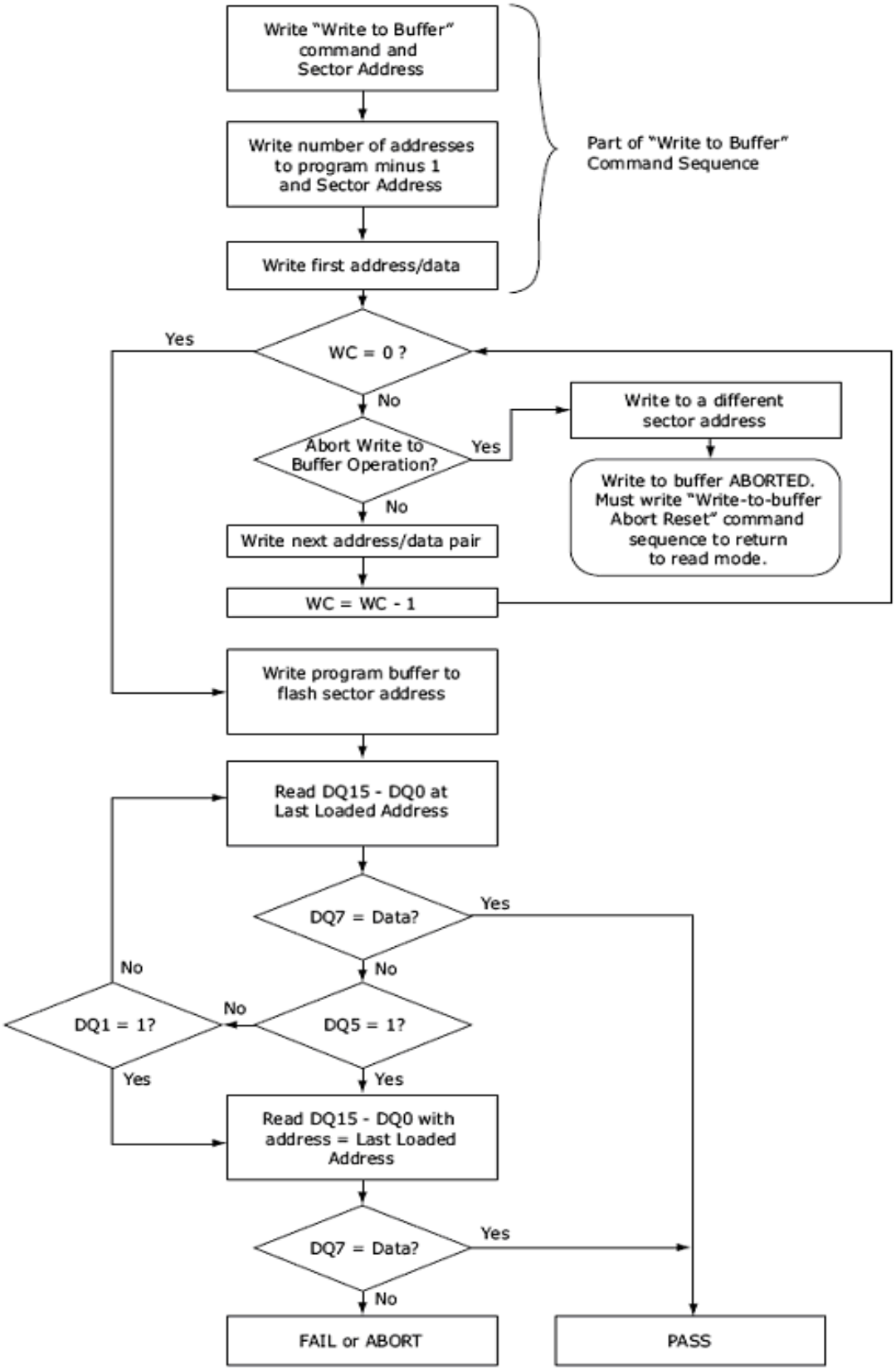
Note that if a Write Buffer address location is loaded multiple times, the “address/data pair” counter **will be decremented for every data load operation**. Also, the **last data loaded** at a location before the “Program Buffer to Flash” confirm command will be programmed into the device. It is the software’s responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements **for each data load operation**, **NOT for each unique write-buffer-address location.**

Once the specified number of write buffer locations have been loaded, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data write combinations will abort the Write Buffer Programming operation. The device will then “go busy”. The Data Bar polling techniques should be used while monitoring the **last address location loaded into the write buffer.** This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.
The write-buffer “embedded” programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device will return to READ mode.
The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the “Number of Locations to Program” step.
- Write to an address in a sector different than the one specified during the “Write-Buffer-Load” command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the “Starting Address” during the “write buffer data loading” stage of the operation.
- Write data other than the “Confirm Command” after the specified number of “data load” cycle.

The ABORT condition is indicated by DQ = 1, DQ7 = DATA# (for the “last address location loaded”) , DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A “Write-to-Buffer-Abort reset” command sequence is required when using the Write Buffer Programming feature in Unlock Bypass mode. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed. Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases.



Write Buffer Programming Operation

15.7 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 15.1 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/ BY#. Refer to *Write Operation Status* for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.* However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 15.2 illustrates the algorithm for the erase operation. Refer to the tables in *Erase/Program Operations* for parameters, and Figure 20.8 for timing diagrams.

15.8 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 15.1 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. *Note that Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

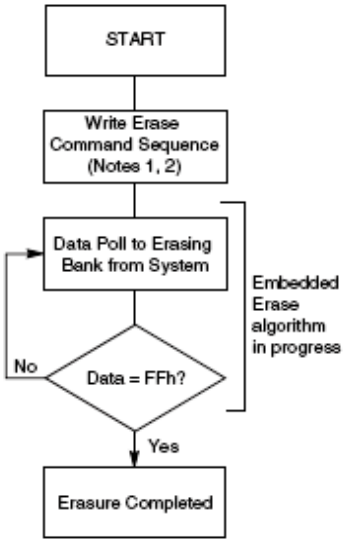
The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to *Write Operation Status* for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 15.2 illustrates the algorithm for the erase operation. Refer to the tables in *Erase/Program Operations* for parameters, and Figure 20.8 for timing diagrams.

Figure 15.2 Erase Operation



Notes
1. *See Table 15.1 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

15.9 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to *Write Operation Status* for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. Refer to *Write Operation Status* for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to Table 9.6, *Secured Silicon Sector Addresses* and *Autoselect Command Sequence* for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don't care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

If the Secured Silicon Sector Protection Bit is verified as programmed without margin, the Secured Silicon Sector Protection Bit Program Command should be reissued to improve program margin. After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin. The programming of the PPB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

15.10 Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are "don't-cares" when writing the Program Suspend command. After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region. The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information. After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information. The system must write the Program Resume command (address bits are "don't care") to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

15.11 Command Definitions Tables

Table 15.1 contains the Memory Array Command Definitions.

Table 15.1 Memory Array Command Definitions

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) 100 (BA) 000	001C 007F				
	Device ID (10)	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	227E	(BA) X0E	(10)	(BA) X0F	(10)
	Secured Silicon Sector Factory Protect (8)	4	555	AA	2AA	55	(BA) 555	90	X03	(8)				
	Sector Group Protect Verify(9)	4	555	AAA	2AA	55	(BA) 555	90	(SA) X02	XX00 / XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer		6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset		3	555	AA	2AA	55	555	F0						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (11)		1	BA	B0										
Program/Erase Resume (12)		1	BA	30										
CFI Query (13)		1	55	98										
Accelerated Program (15)		2	XX	A0	PA	PD								
Unlock Bypass Entry (15)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (15)		2	XX	A0	PA	PD								
Unlock Bypass Erase (15)		2	XX	80	XX	10								
Unlock Bypass CFI (13)(15)		1	XX	98										
Unlock Bypass Reset (15)		2	XXX	90	XXX	00								

Legend

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by PL064 Amax:A19, PL032: Amax:A18.
PA = Program Address (Amax:A0). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.
PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.
RA = Read Address (Amax:A0).
RD = Read Data (DQ15:DQ0) from location RA.
SA = Sector Address (Amax:A12) for verifying (in autoselect mode) or erasing.
WC = Word Count is the number of write buffer location to load minus 1.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
X = Don't care

Notes

1. *See Table 9.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase*

Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).

7. *Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence for more information.*
8. *The data is DQ6=1 for customer locked .*
9. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Device ID must be read across cycles 4, 5, and 6. PL064 (X0Eh = 2202h, X0Fh = 2201h), PL032 (X0Eh = 220Ah, X0Fh = 2201h).*
11. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/ Erase Suspend command is valid only during a sector erase operation, and requires bank address.*
12. *Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
14. *WP#/ACC must be at VID during the entire operation of command.*
15. *Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.*

Table 15.2 Sector Protection Command Definitions

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)													
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0												
Secured Silicon Sector Entry (16)	3	555	AA	2AA	55	555	88								
Secured Silicon Sector Exit (16)	4	555	AA	2AA	55	555	90	XX	00						
Secured Silicon Protection Bit Program (Notes 5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD (0)		
Secured Silicon Protection Bit Status	5	555	AA	2AA	55	555	60	OW	48	OW	RD (0)				
PPB Program (Notes 5, 6, 11)	6	555	AA	2AA	55	555	60	(SA) WP	68	(SA) WP	48	(SA) WP	RD (0)		
PPB Status	4	555	AA	2AA	55	555	90	(SA) WP	RD (0)						
All PPB Erase (Notes 5, 6, 13, 14)	6	555	AA	2AA	55	555	60	WP	60	(SA)	40	(SA) WP	RD (0)		
PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
PPB Lock Bit Status (15)	4	555	AA	2AA	55	555	58	SA	RD (1)						

Legend

OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
SA = Sector Address where security command applies. Address bits Amax:A12 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010)
X = Don't care
SPMLB = Persistent Protection Mode Locking Bit

Notes

1. *See Table 9.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns device to reading array.*
6. *Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *Entire command sequence must be entered for each portion of password.*

9. *Command sequence returns FFh if PPMLB is set.*
10. *The password is written over four consecutive cycles, at addresses 0-3.*
11. *A 2 µs timeout is required between any two portions of password.*
12. *A 100 µs timeout is required between cycles 4 and 5.*
13. *A 1.2 ms timeout is required between cycles 4 and 5.*
14. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.*
15. *DQ1 = 1 if PPB locked, 0 if unlocked.*
16. *Once the Secured Silicon Sector Entry Command sequence has been entered, the standard array cannot be accessed until the Exit SecSi Sector command has been entered or the device has been reset.*

16. Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 16.1 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

16.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

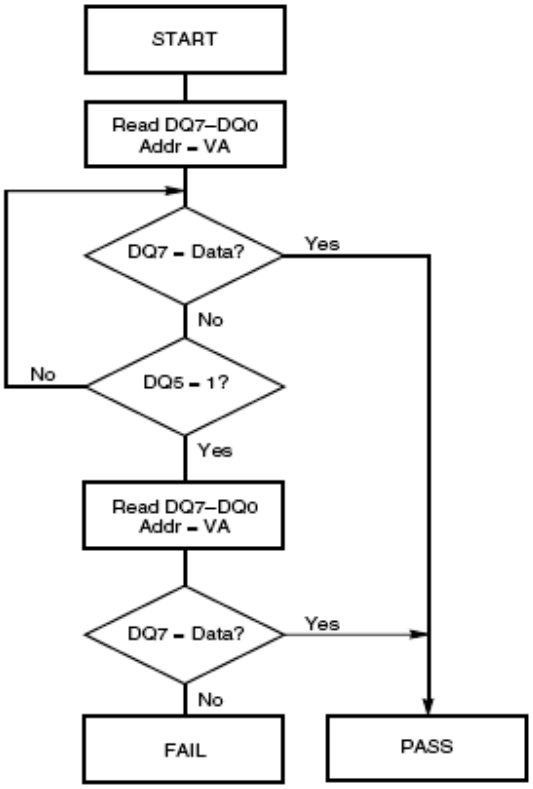
During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 400 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles.

Table 16.1 shows the outputs for Data# Polling on DQ7. Figure 16.1 shows the Data# Polling algorithm. Figure 20.10 shows the Data# Polling timing diagram.

Figure 16.1 Data# Polling Algorithm



Notes

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

16.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 16.1 shows the outputs for RY/BY#.

16.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

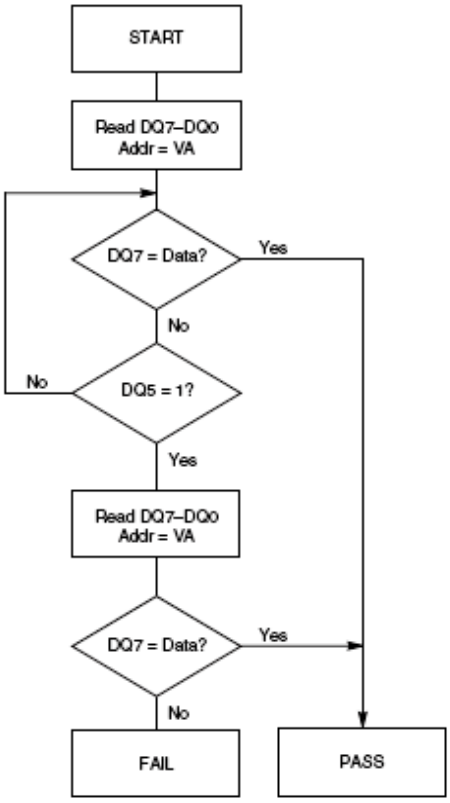
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the *DQ7: Data# Polling*).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 16.1 shows the outputs for Toggle Bit I on DQ6. Figure 16.2 shows the toggle bit algorithm. Figure 20.11 shows the toggle bit timing diagrams. Figure 20.12 shows the differences between DQ2 and DQ6 in graphical form. See also the *DQ2: Toggle Bit II* .

Figure 16.2 Toggle Bit Algorithm



Note:
The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the DQ6: Toggle Bit I and DQ2: Toggle Bit II for more information.

16.4 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 16.1 to compare outputs for DQ2 and DQ6.

Figure 16.2 shows the toggle bit algorithm in flowchart form, and the *DQ2: Toggle Bit II* explains the algorithm. See also the *DQ6: Toggle Bit I* . Figure 20.11 shows the toggle bit timing diagram. Figure 20.12 shows the differences between DQ2 and DQ6 in graphical form.

16.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 16.2 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

16.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

16.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.). When the time-out period is complete, DQ3 switches from a “0” to a “1.” See also the *Sector Erase Command Sequence*.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read

DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 16.1 shows the status of DQ3 relative to the other status bits.

Table 16.1 Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend -Program		DQ7#	Toggle	0	N/A	N/A	0
Program Suspend Mode **(Note 3)**	Reading within Program Suspended Sector		Invalid (Not Allowed)	Invalid (Not Allowed)	Invalid (Not Allowed)	Invalid (Not Allowed)	Invalid (Not Allowed)	1
	Reading within Non-program Suspended Sector		Data	Data	Data	Data	Data	1

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to DQ5: Exceeded Timing Limits for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

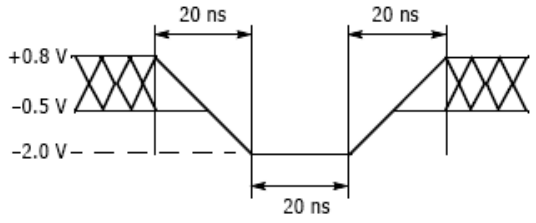
17. Absolute Maximum Ratings

Storage Temperature Plastic Packages	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
Voltage with Respect to Ground	
V_{CC} (Note 1)	–0.5 V to +4.0 V
A9, OE#, and RESET# (Note 2)	–0.5 V to +12.0 V
WP#/ACC (Note 2)	–0.5 V to +10.5 V
All other pins (Note 1)	–0.5 V to VCC +0.5 V
Output Short Circuit Current (Note 3)	200 mA

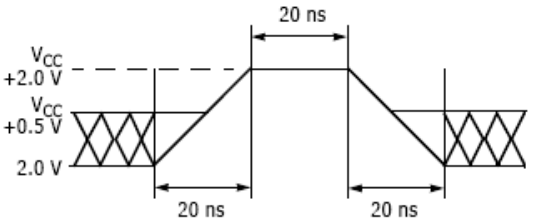
Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 17.1*
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 17.1 . Maximum DC input voltage on pin A9, OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability*

Figure 17.1 Maximum Overshoot Waveforms



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

18. Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

Industrial (I) Devices

Ambient Temperature (T_A) .....–40°C to +85°C

Wireless (W) Devices

Ambient Temperature (T_A) .....–25°C to +85°C

Supply Voltages

V_{CC} .....2.7–3.6 V

19. DC Characteristics

Table 19.1 CMOS Compatible

Parameter	Parameter Description (notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max				±1.0	µA
I_{LIT}	A9, OE#, RESET# Input Load Current	$V_{CC} = V_{CC}$ max; V_{ID}= 11.5 V				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC}$ max; V_{ID}= 11.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, OE# = V_{IH} $V_{CC} = V_{CC}$ max				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (1, 2)	OE# = V_{IH}, $V_{CC} = V_{CC}$ max	5 MHz		20	30	mA
			10 MHz		45	55	
I_{CC2}	V_{CC} Active Write Current (2, 3)	OE# = V_{IH}, WE# = V_{IL}			15	25	mA
I_{CC3}	V_{CC} Standby Current (2)	CE#, RESET#, WP#/ACC = V_{IO} ± 0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (2)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{IO}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (1, 2)	OE# = V_{IH},	5 MHz		21	45	mA
			10 MHz		46	70	
I_{CC7}	V_{CC} Active Read-While-Erase Current (1, 2)	OE# = V_{IH},	5 MHz		21	45	mA
			10 MHz		46	70	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (2, 5)	OE# = V_{IH}			17	25	mA
I_{CC9}	V_{CC} Active Page Read Current (2)	OE# = V_{IH}, 4 word Page Read			10	15	mA
V_{IL}	Input Low Voltage	V_{IO} = 2.7–3.6 V		–0.5		0.8	V
V_{IH}	Input High Voltage	V_{IO} = 2.7–3.6 V		2		V_{CC}+0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		10.5		11.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA, $V_{CC} = V_{CC}$ min, V_{IO} = 2.7–3.6 V				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{IO} = V_{CC}$ min		V_{CC}- 0.2V			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (5)			2.3		2.5	V

Notes

1. *The I_{CC} current listed is typically less than 5 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 2 µA.*
5. *Not 100% tested.*

20. AC Characteristic

20.1 Test Conditions

Figure 20.1 Test Setups

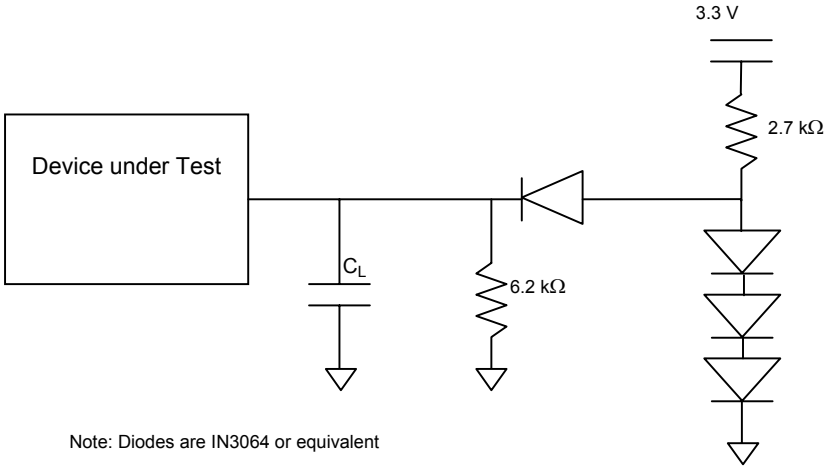


Table 20.1 Test Specifications

Test Conditions	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0-3.0	V
Input timing measurement reference levels	$V_{cc}/2$	V
Output timing measurement reference levels	$V_{cc}/2$	V

20.2 Switching Waveforms

Table 20.2 Key To Switching Waveforms

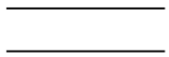
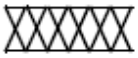
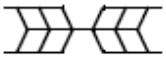
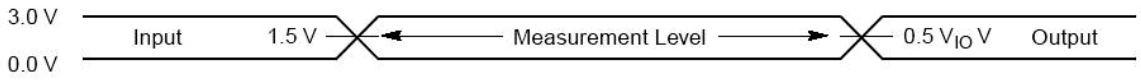
Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Figure 20.2 Input Waveforms and Measurement Levels



20.3 VCC Ramp Rate

All DC characteristics are specified for a V_{CC} ramp rate > 1V/100 µs. If the V_{CC} ramp rate is < 1V/100 µs, a hardware reset required.+

20.4 Read Operations

Table 20.3 Read-Only Operations

Parameter		Description (Notes)	Test Setup		Speed Options	Unit
JEDEC	Std.				70	
t_{AVAV}	t_{RC}	Read Cycle Time (1)		Min	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL}	Max	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	Max	70	ns
	t_{PACC}	Page Access Time		Max	25	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (3)		Max	16	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (1, 3)		Max	16	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (3)		Min	5	ns
	t_{OEH}	Output Enable Hold Time (1)	Read	Min	0	ns
			Toggle and Data# Polling	Min	10	ns

Notes

1. *Not 100% tested.*
2. *See Figure 20.1 and Table 20.1 for test specifications*
3. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of VCC /2. The time from OE# high to the data bus driven to VCC /2 is taken as tDF.*

Figure 20.3 Read Operation Timings

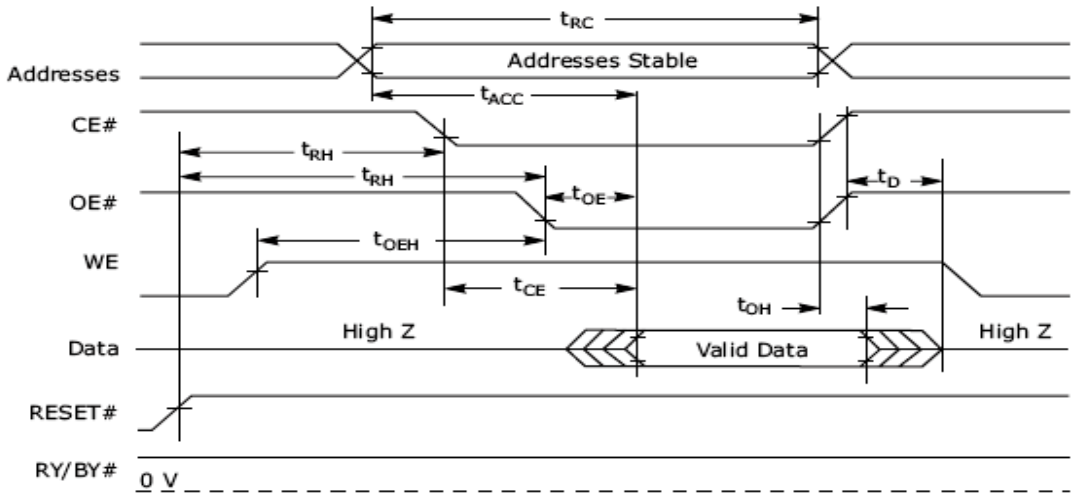
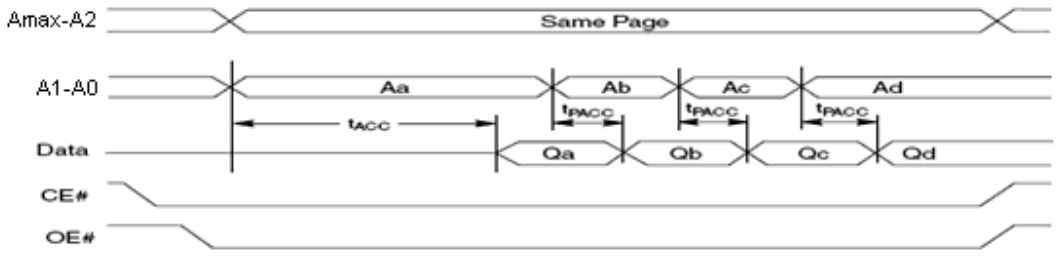


Figure 20.4 Page Read Operation Timings



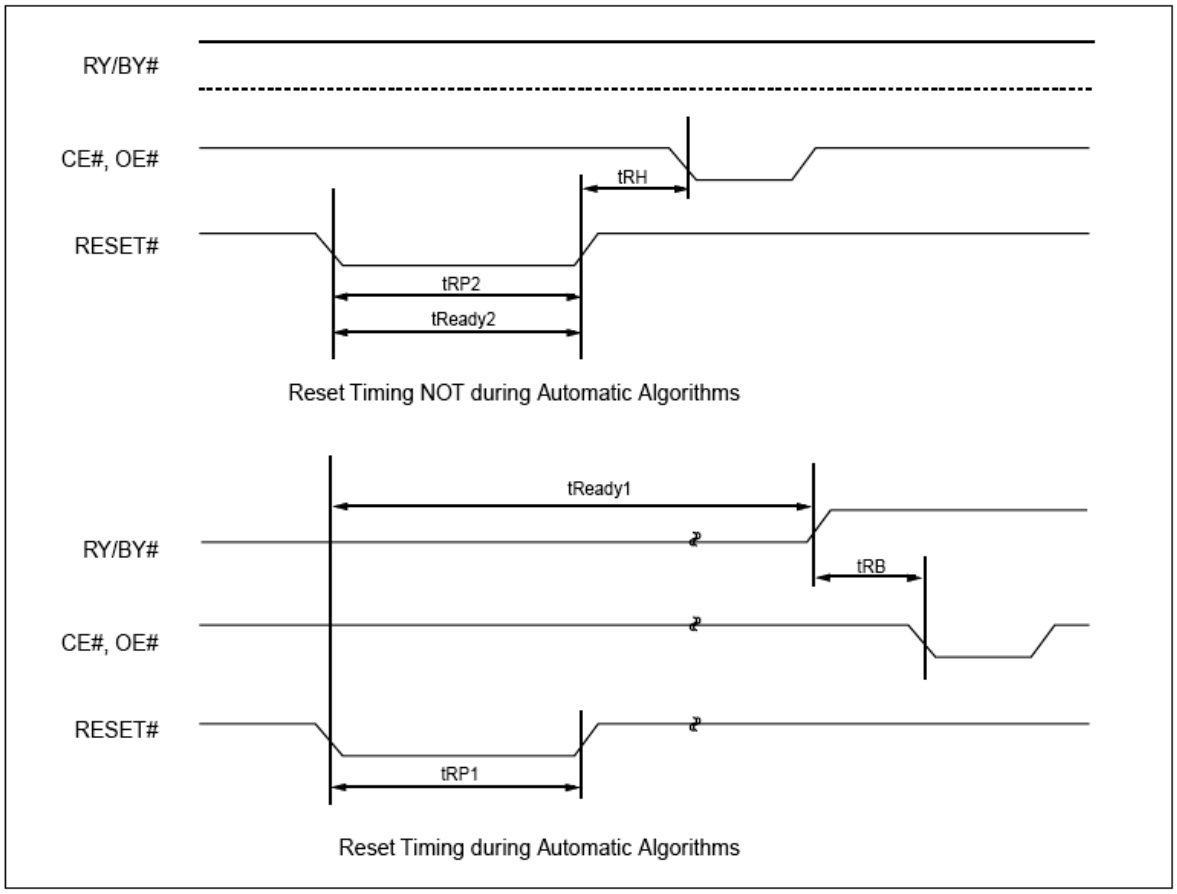
20.5 Reset

Table 20.4 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	tReady	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note
Not 100% tested.

Figure 20.5 Reset Timings



20.6 Erase/Program Operations

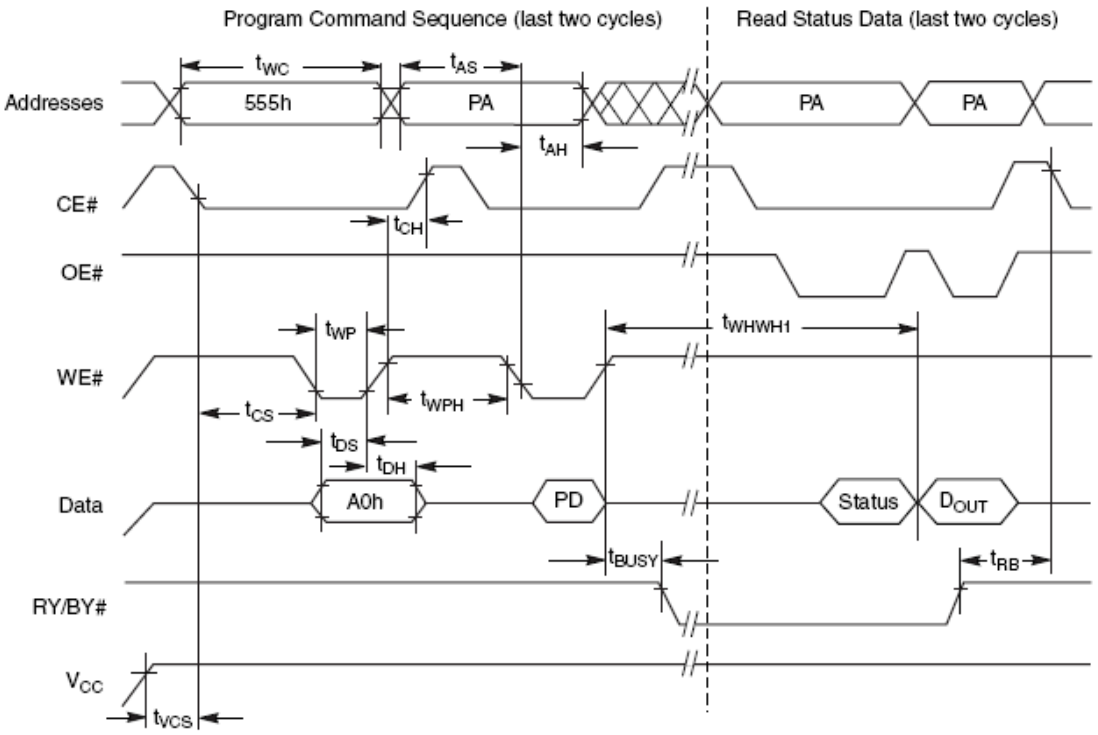
Table 20.5 Erase and Program Operations

Parameter		Description		Speed Options (ns)	
JEDEC	Std			70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	35	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	25	ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0	ns
$t_{WHWH\ 1}$	$t_{WHW\ H1}$	Programming Operation (Note 2)	Typ	6	µs
$t_{WHWH\ 1}$	$t_{WHW\ H1}$	Accelerated Programming Operation (Note 2)	Typ	4	µs
$t_{WHWH\ 2}$	$t_{WHW\ H2}$	Sector Erase Operation (Note 2)	Typ	0.5	sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50	µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Max	90	ns
			Min	35	ns
	t_{PSL}	Program Suspend Latency	Max	35	µs
	t_{ESL}	Erase Suspend Latency	Max	35	µs

Notes:
1. *Not 100% tested.*
2. *See Table 21.4 for more information.*

20.7 Timing Diagrams

Figure 20.6 Program Operation Timings



Notes

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address*

Figure 20.7 Accelerated Program Timing Diagram

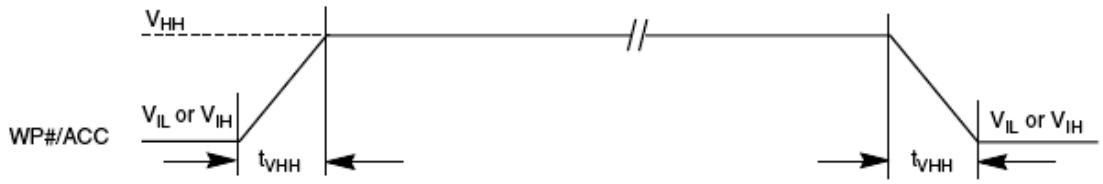
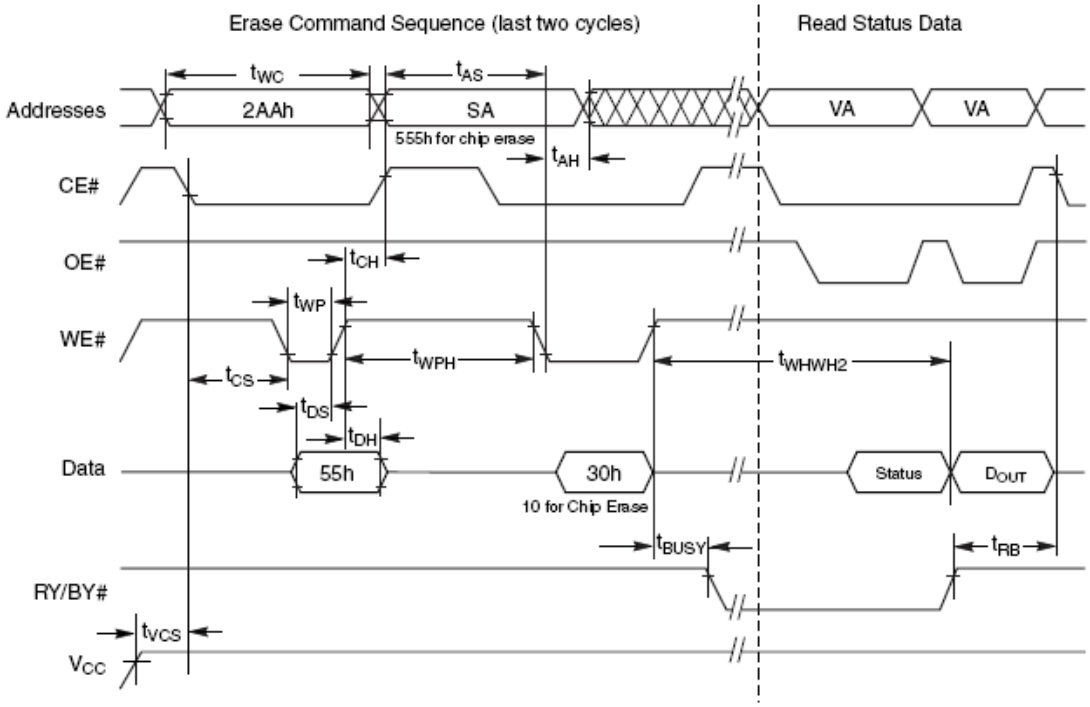


Figure 20.8 Chip/Sector Erase Operation Timings



Notes

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status)*

Figure 20.9 Back-to-back Read/Write Cycle Timings

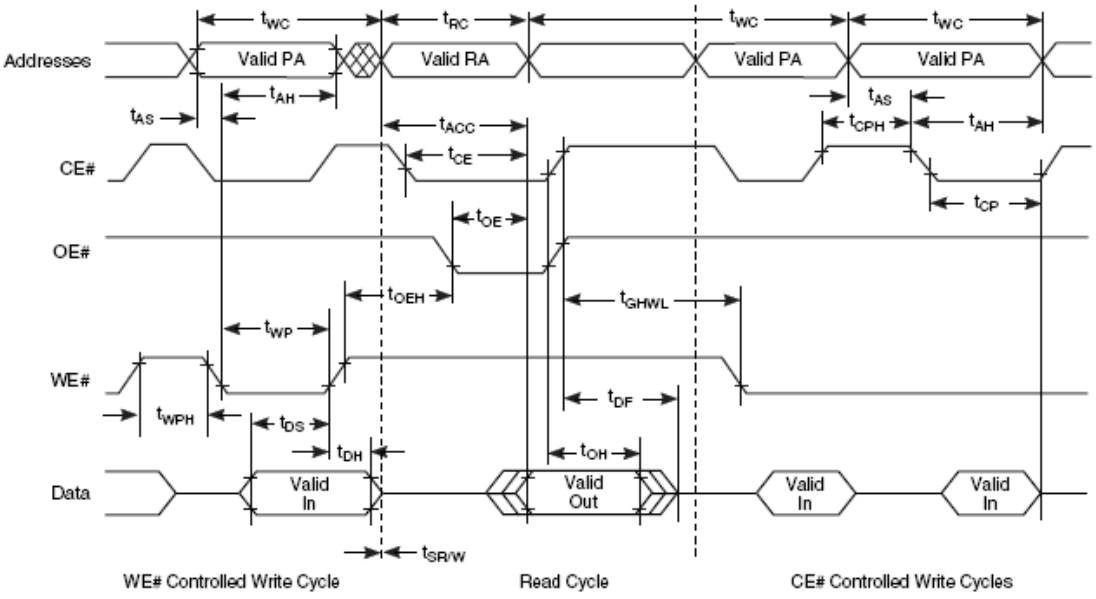
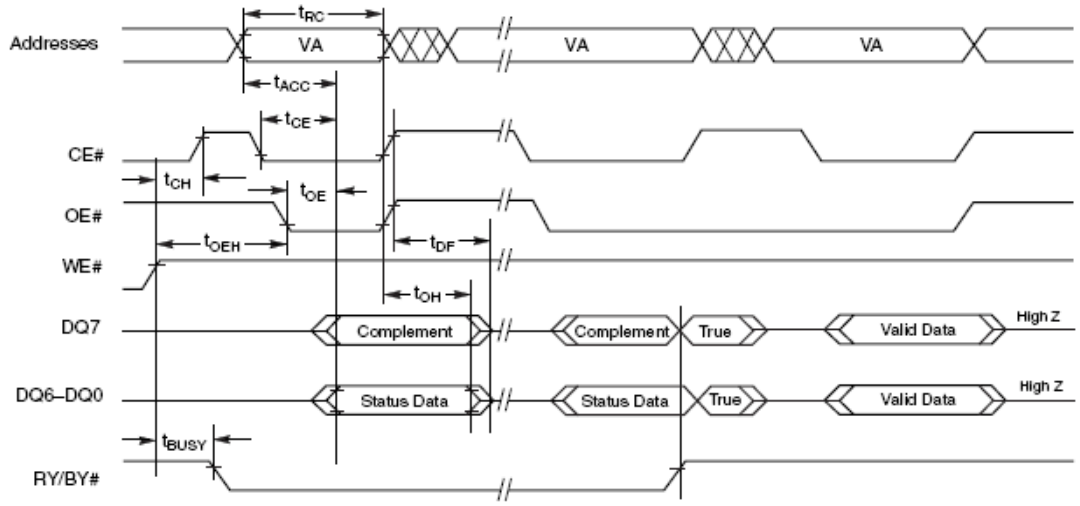


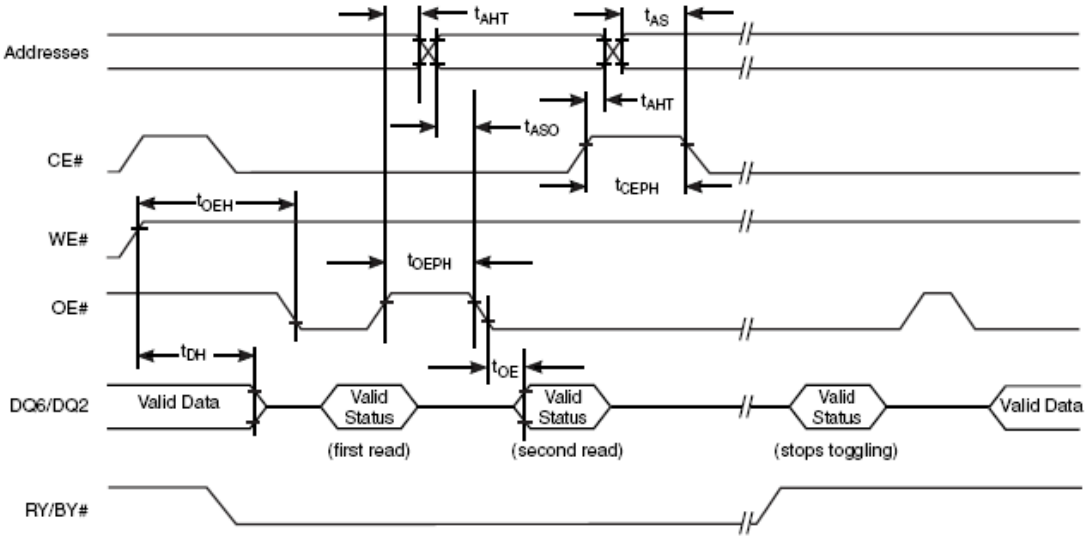
Figure 20.10 Data# Polling Timings (During Embedded Algorithms)



Note

VA = Valid address. The illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

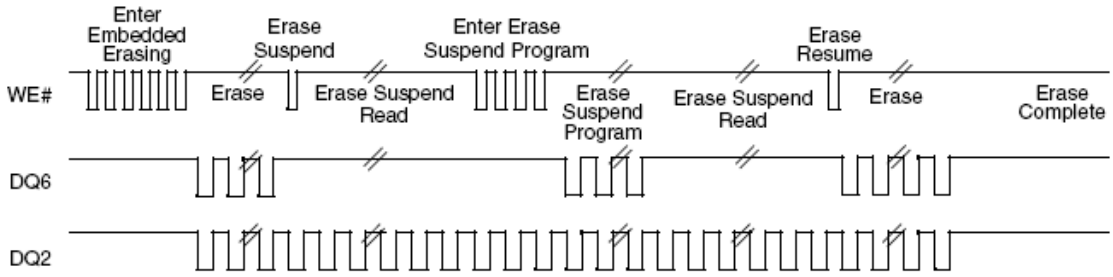
Figure 20.11 Toggle Bit Timings (During Embedded Algorithms)



Notes

1. *VA = Valid address; not required for DQ6. The illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 20.12 DQ2 vs. DQ6



Note
DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

21. Protect/Unprotect

Table 21.1 Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note
Not 100% tested

Figure 21.1 Temporary Sector Unprotect Timing Diagram

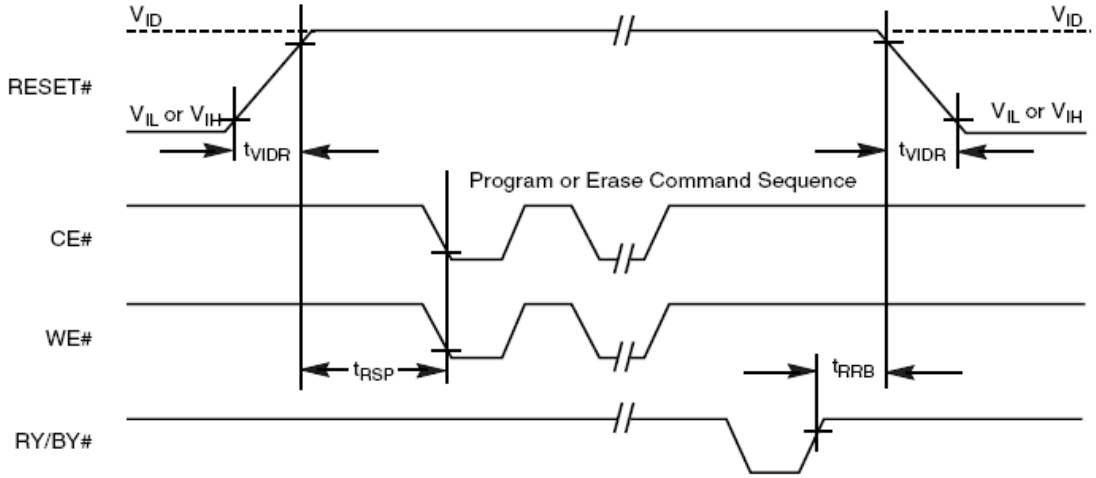
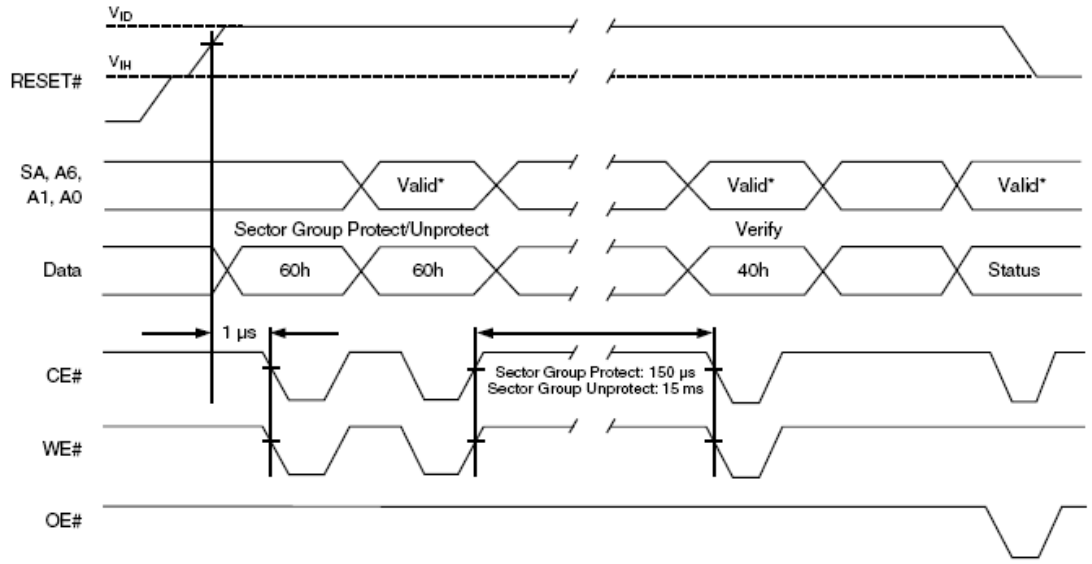


Figure 21.2 Sector/Sector Block Protect and Unprotect Timing Diagram



Notes

1. *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

21.1 Controlled Erase Operations

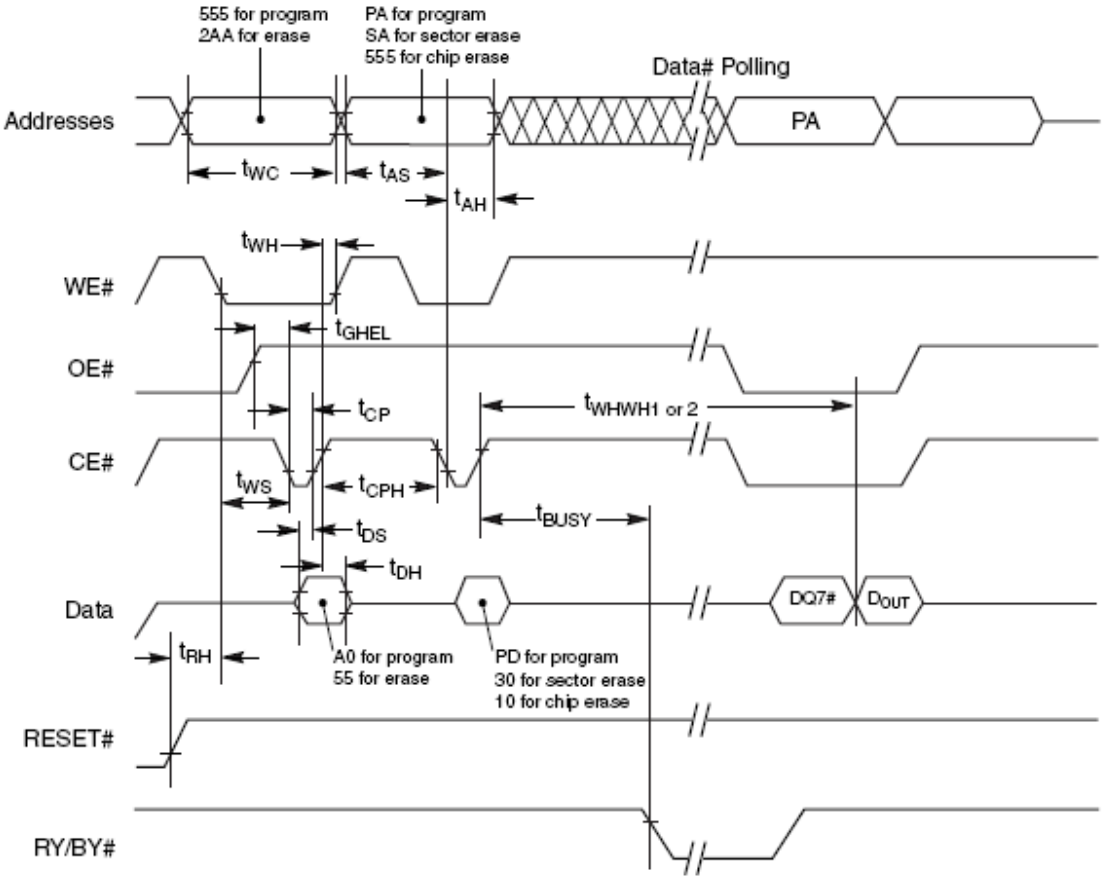
Table 21.2 Alternate CE# Controlled Erase and Program Operations

Parameter		Description (Notes)		Speed Options	Unit
JEDEC	Std			70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	35	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	25	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	sec

Notes

1. *Not 100% tested.*
2. *See Erase And Programming Performance for more information.*

Figure 21.3 Alternate CE# Controlled Write (Erase/Program) Operation Timings 555 for program PA for program



Notes

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device*

Table 21.4 Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	2	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	PL064	71	113.6	sec	
	PL032	39	62.4	sec	
Word Program Time		6	100	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time		4	60	µs	
Chip Program Time **(Note 3)**	PL064	25.2	50.4	sec	
	PL032	12.6	25.2	sec	

Notes

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typical assume checkerboard pattern. All values are subject to change.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles. All values are subject to change.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 15.1 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

22. 48-PIN TSOP PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Note: Test conditions are Temperature = 25°C and f = 1.0 MHz

23. BGA Pin Capacitance

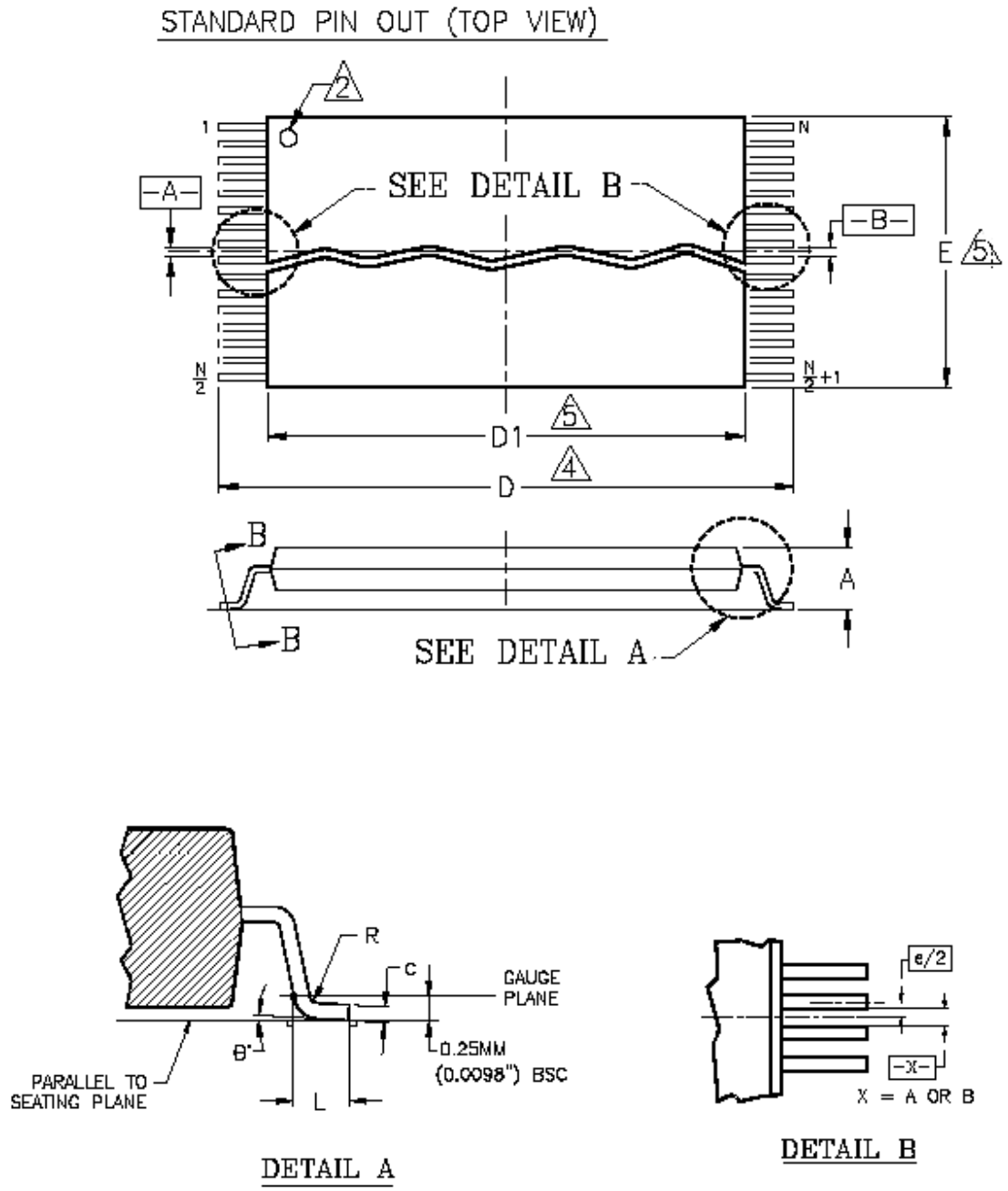
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6.3	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	7	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	5.5	8	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	11	12	pF

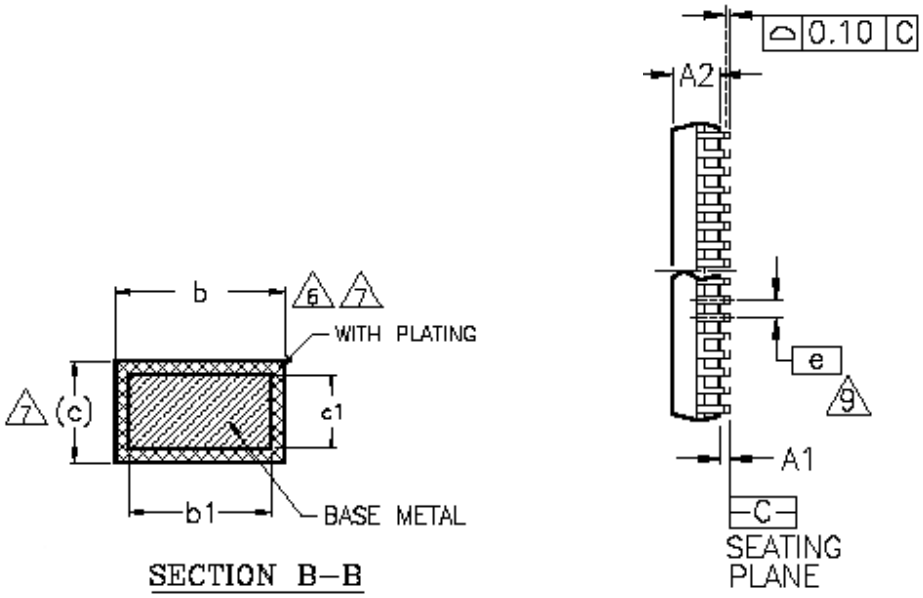
Notes

1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25°C, f = 1.0 MHz.*

24. Physical Dimensions

Figure 24.1 TSOP 48-pin 12mm x 20mm



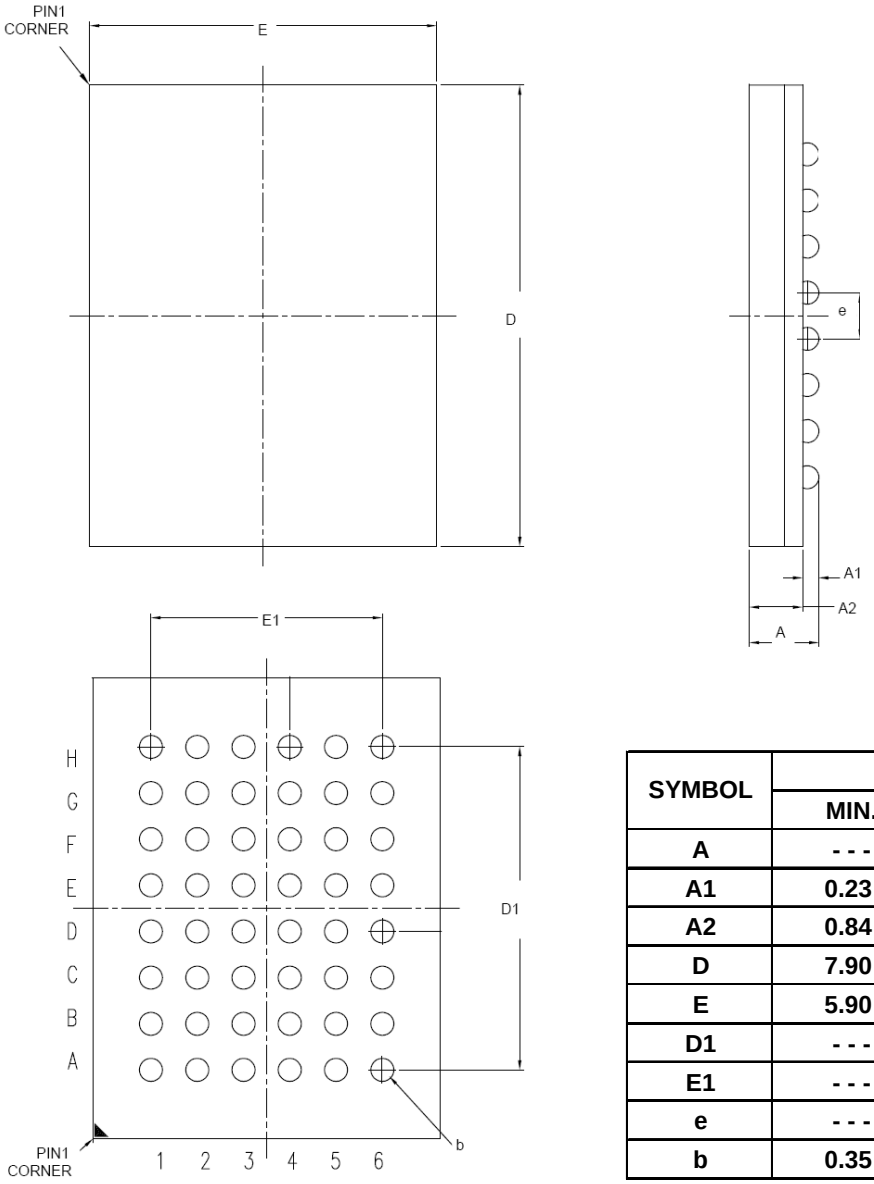


Package	TS 48		
Jedec	MO–142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

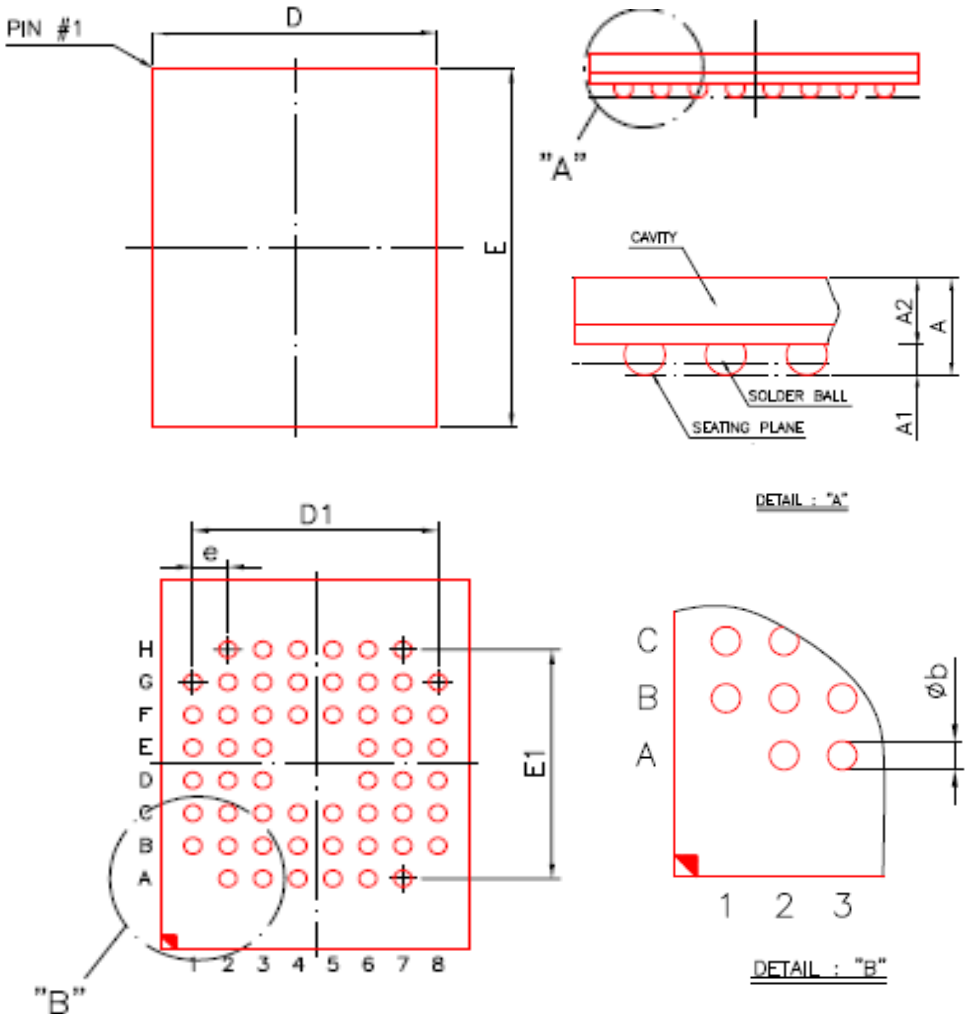
Figure 24.2 48-ball TFBGA package outline (PL032)



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.30
A1	0.23	0.29	- - -
A2	0.84	0.91	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	- - -	5.60	- - -
E1	- - -	4.00	- - -
e	- - -	0.80	- - -
b	0.35	0.40	0.45

Note : 1. Coplanarity: 0.1 mm

Figure 24.3 56-ball Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.20
A1	0.25	0.30	0.35
A2	0.71	0.76	0.81
D	6.90	7.00	7.10
E	8.90	9.00	9.10
D1	- - -	5.60	- - -
E1	- - -	5.60	- - -
e	- - -	0.80	- - -
b	0.35	0.40	0.45

Revisions List

Revision No	Description	Date
A	Initial Release	2007/9/19
B	Update the 48 Ball package thickness from 1.31mm to 1.2mm in page 64	2007/12/21
C	Correct the Manufacturer ID at Table 9.7 Autoselect Codes (High Voltage Method) in page 21	2008/1/3
D	1. Change the customer-lockable words from 128 words to 64 words in page 1, 21, 26 and 27 2. Change the page access times from 20ns to 25ns in page 1, 2, 5 and 52. 3. Remove 65ns speed grade in page 1, 2, 5, 52, 54 and 59. 4. Change V_{ID} from 11.5-12.5V to 10.5-11.5V in page 11and 49. 5. Update the CFI table in page 29 and 30. 6. Remove the 48-ball FBGA Connection Diagrams for PL064 in page 8 7. Correct the 48 Ball package thickness from 1.2mm to 1.3mm in page 64 8. Add the 56 Ball FBGA Connection Diagrams and Physical Dimensions in page 9 and page 65	2008/3/27