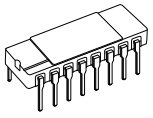
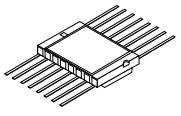
M54HC595

RAD-HARD 8 BIT SHIFT REGISTER WITH OUTPUT LATCHES (3 STATE)

- HIGH SPEED:
  f_{MAX} = 59MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN.) FOR QA to QH
  $|I_{OH}| = I_{OL}$ = 4mA (MIN.) FOR QH'
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 595
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9306-051



DILC-16



FPC-16

ORDER CODES

PACKAGE	FM	EM
DILC	M54HC595D	M54HC595D1
FPC	M54HC595K	M54HC595K1

DESCRIPTION

The M54HC595 is an high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated with silicon gate C^2MOS technology.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.
The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

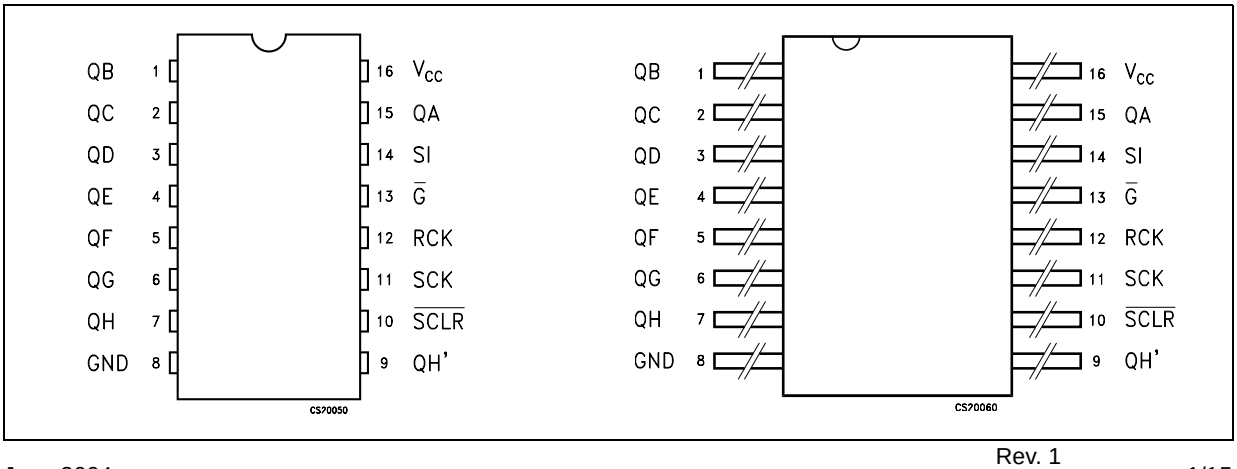


Figure 1: IEC Logic Symbols

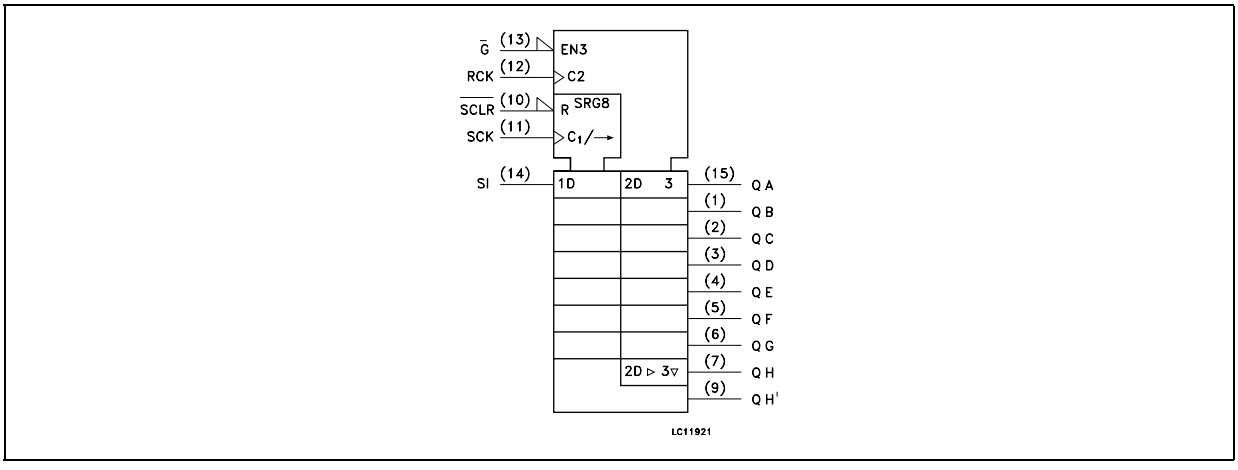


Figure 2: Input And Output Equivalent Circuit

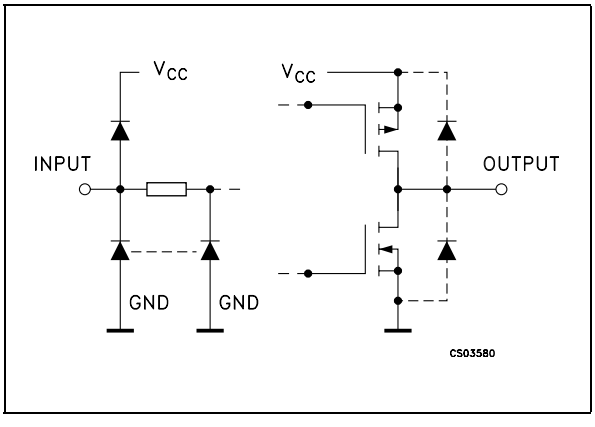


Table 1: Pin Description

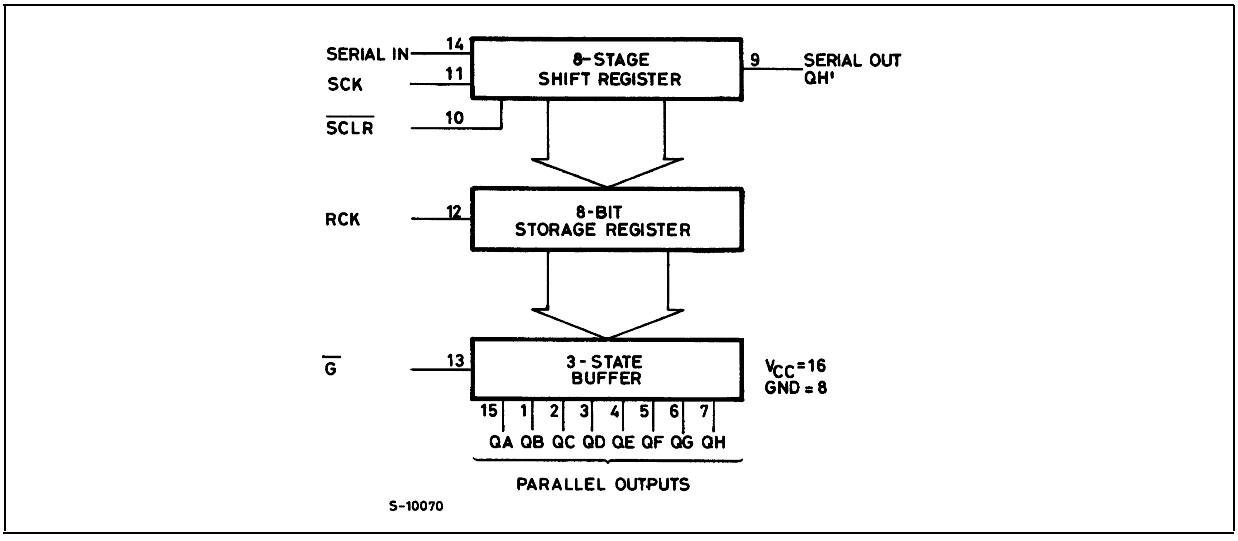
PIN N°	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Data Outputs
9	QH'	Serial Data Outputs
10	$\overline{SCLR}$	Shift Register Clear Input
11	SCK	Shift Register Clock Input
13	$\overline{G}$	Output Enable Input
14	SI	Serial Data Input
12	RCK	Storage Register Clock Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUTS					OUTPUTS
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L	⎍	H	X	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H	⎍	H	X	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X	⎏	H	X	X	STATE OF S.R. IS NOT CHANGED
X	X	X	⎍	X	S.R. DATA IS STORED INTO STORAGE REGISTER
X	X	X	⎏	X	STORAGE REGISTER STATE IS NOT CHANGED

X: Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Figure 4: Logic Diagram

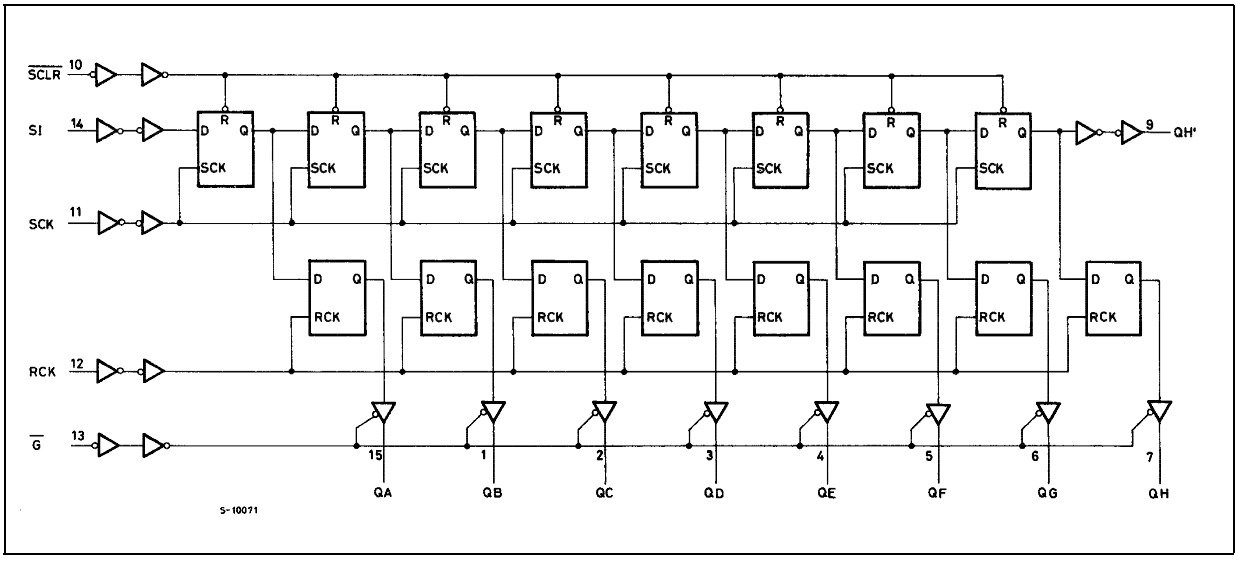


Table 5: This logic diagram has not be used to estimate propagation delays

Figure 6: Timing Chart

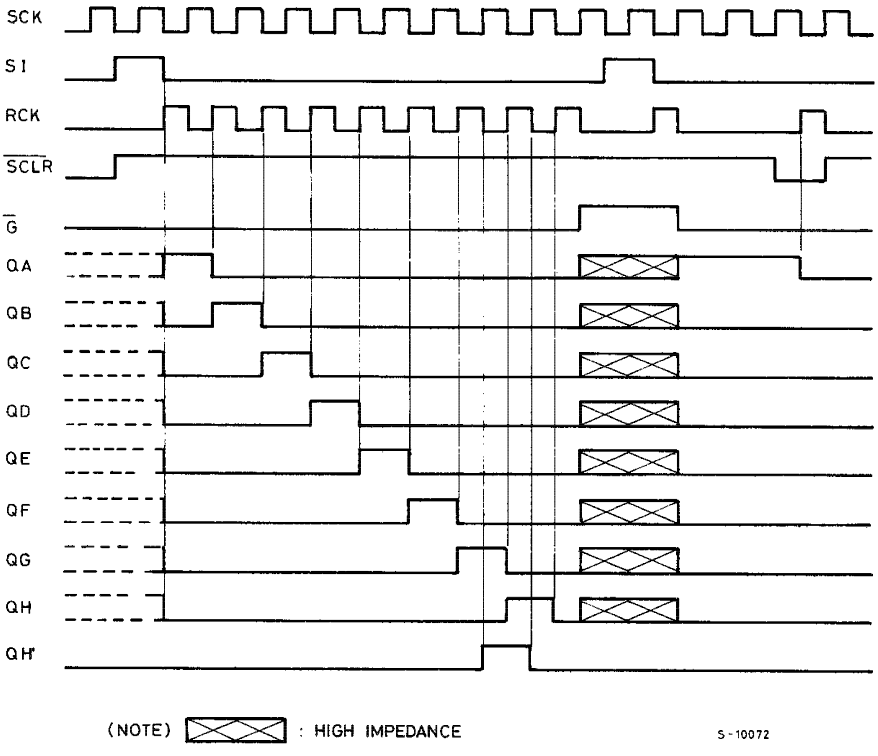


Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	420	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (for QH' outputs)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (for QA to QH outputs)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (for QH' outputs)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (for QA to QH outputs)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 10	µA

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	µA

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Qn)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time (QH')	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK - QH')	2.0	50			45	125		155		190	ns
		4.5				15	25		31		38	
		6.0				13	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SCLR}$ - QH')	2.0	50			60	175		220		265	ns
		4.5				18	35		44		53	
		6.0				15	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Qn)	2.0	50			60	150		190		225	ns
		4.5				20	30		38		45	
		6.0				17	26		32		38	
		2.0	150			75	190		240		285	ns
		4.5				25	38		48		57	
		6.0				22	32		41		48	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		45	135		170		205	ns
		4.5				15	27		34		41	
		6.0				13	23		29		35	
		2.0	150	R_L = 1 KΩ		60	175		220		265	ns
		4.5				20	35		44		53	
		6.0				17	30		37		45	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		30	150		190		225	ns
		4.5				15	30		38		45	
		6.0				14	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.0	17		4.8		4		MHz
		4.5			30	50		24		20		
		6.0			35	59		28		24		
		2.0	150		5.2	14		4.2		3.4		MHz
		4.5			26	40		21		17		
		6.0			31	45		25		20		
$t_{W(H)}$	Minimum Pulse Width (SCK, RCK)	2.0	50			17	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	

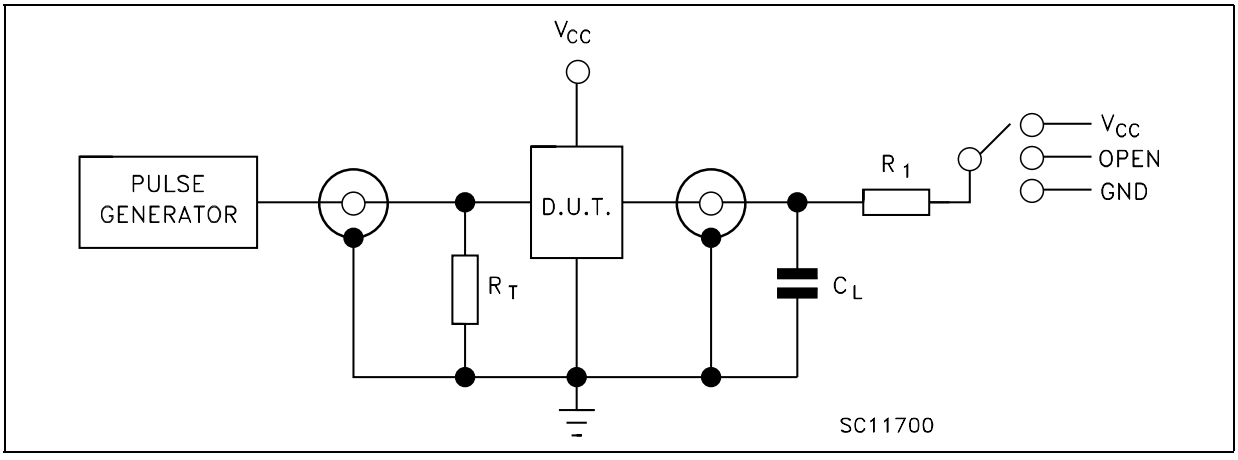
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(L)}$	Minimum Pulse Width (SCLR)	2.0	50			20	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (SI - CCK)	2.0	50			25	50		65		75	ns
		4.5				5	10		13		15	
		6.0				4	9		11		13	
t_s	Minimum Set-up Time (SCK - RCK)	2.0	50			35	75		95		110	ns
		4.5				8	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (SCRL - RCK)	2.0	50			40	100		125		145	ns
		4.5				10	20		25		29	
		6.0				7	17		21		25	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Clear Removal Time	2.0	50			15	50		65		75	ns
		4.5				3	10		13		15	
		6.0				3	9		11		13	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)					184						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Figure 7: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 8: Waveform - SCK To QH' Propagation Delay Times, SCK Minimum Pulse Width (f=1MHz; 50% duty cycle)

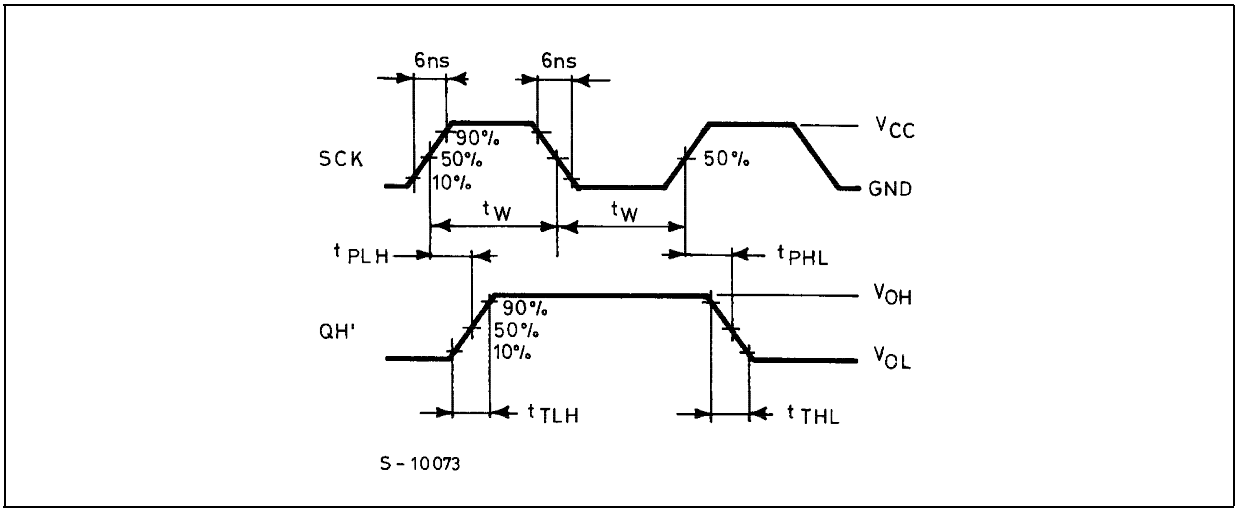


Figure 9: Waveform - RCK To Qn Propagation Delay Times (f=1MHz; 50% duty cycle)

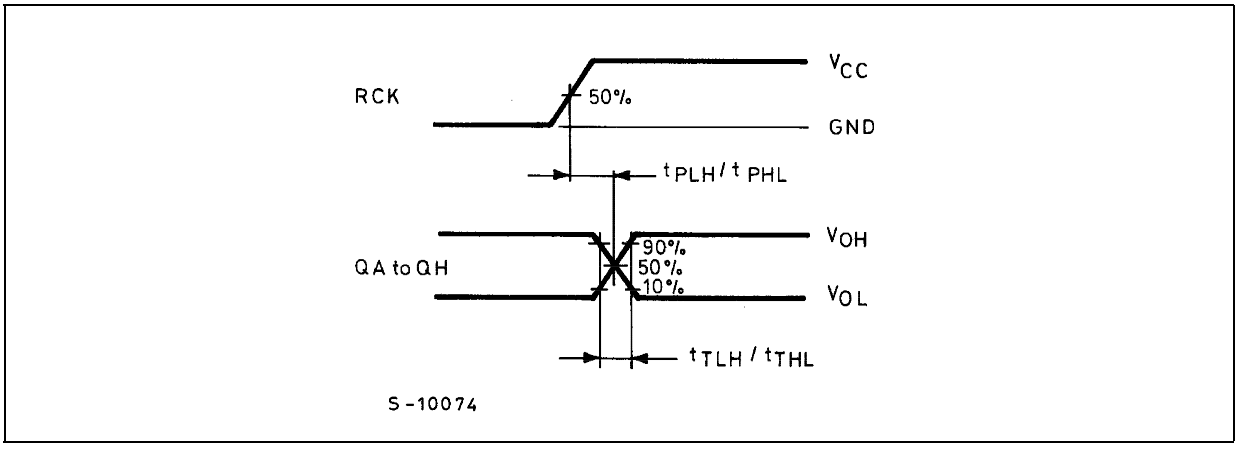


Figure 10: Waveform - SI To SCK Setup And Hold Times (f=1MHz; 50% duty cycle)

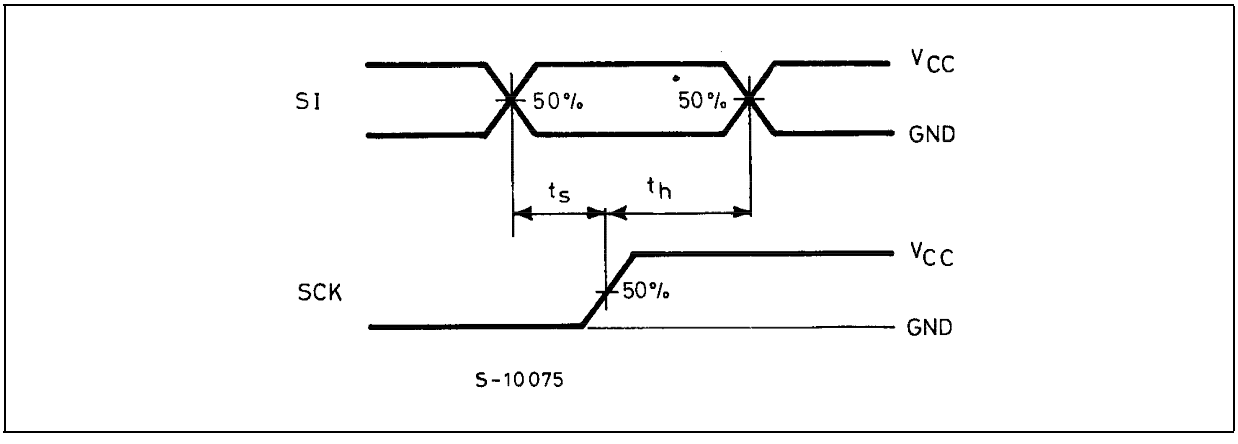


Figure 11: Waveform - SCK To RCK Setup And Hold Times (f=1MHz; 50% duty cycle)

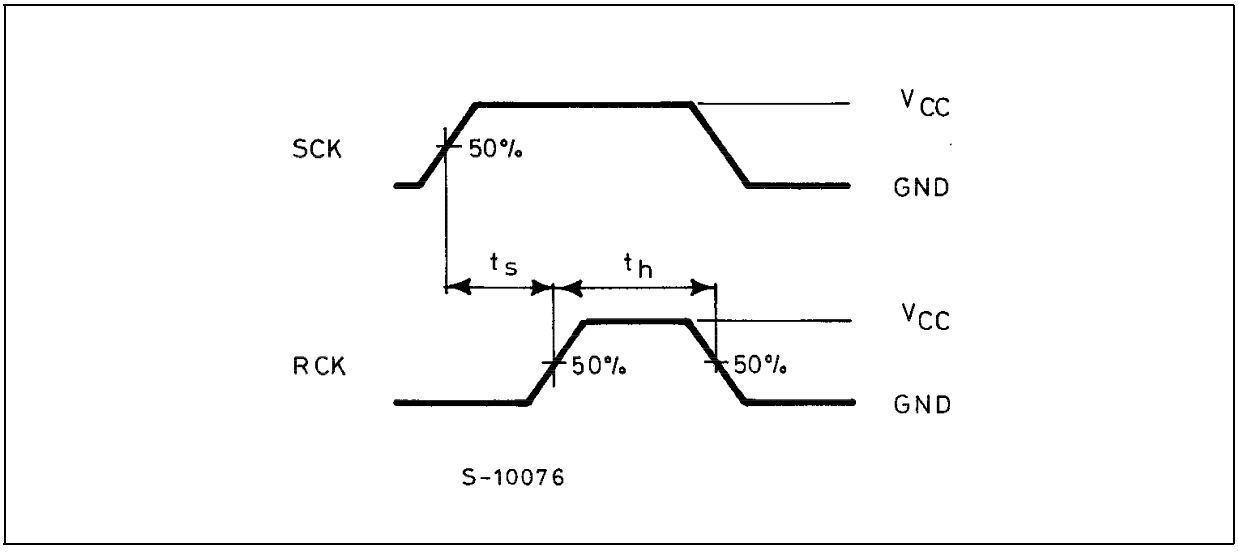


Figure 12: Waveform - $\overline{SCLR}$ Minimum Pulse Width, Minimum Removal Time
(f=1MHz; 50% duty cycle)

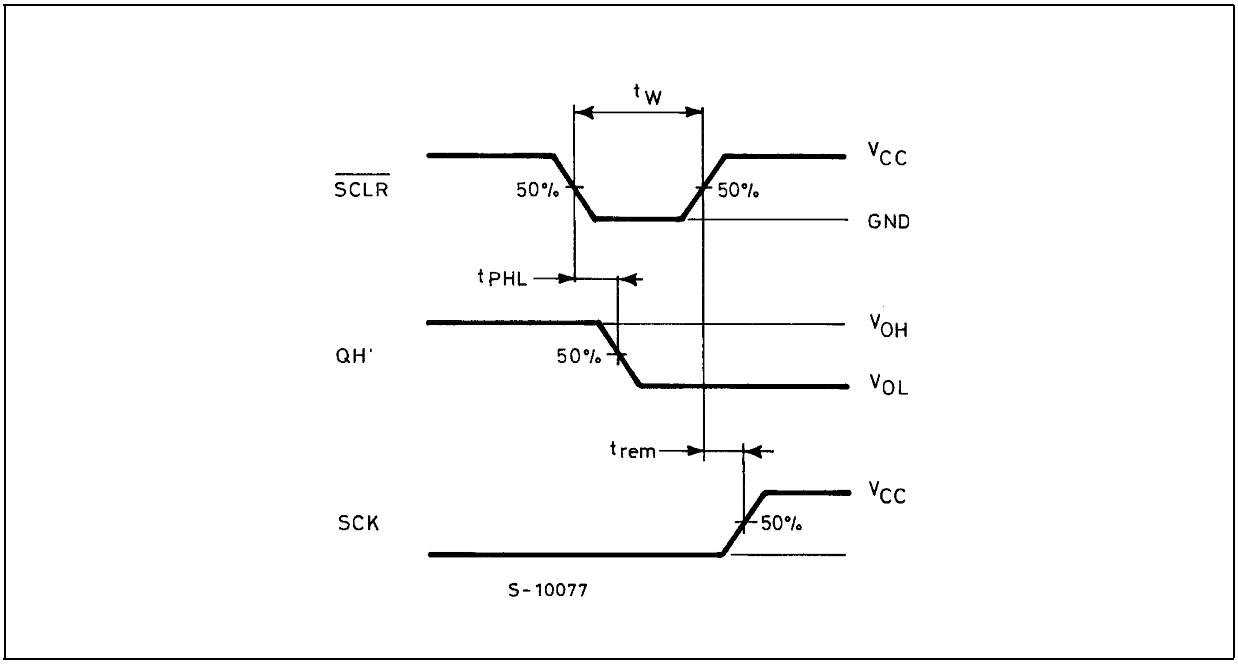


Figure 13: Waveform - Output Enable And Disable Times (f=1MHz; 50% duty cycle)

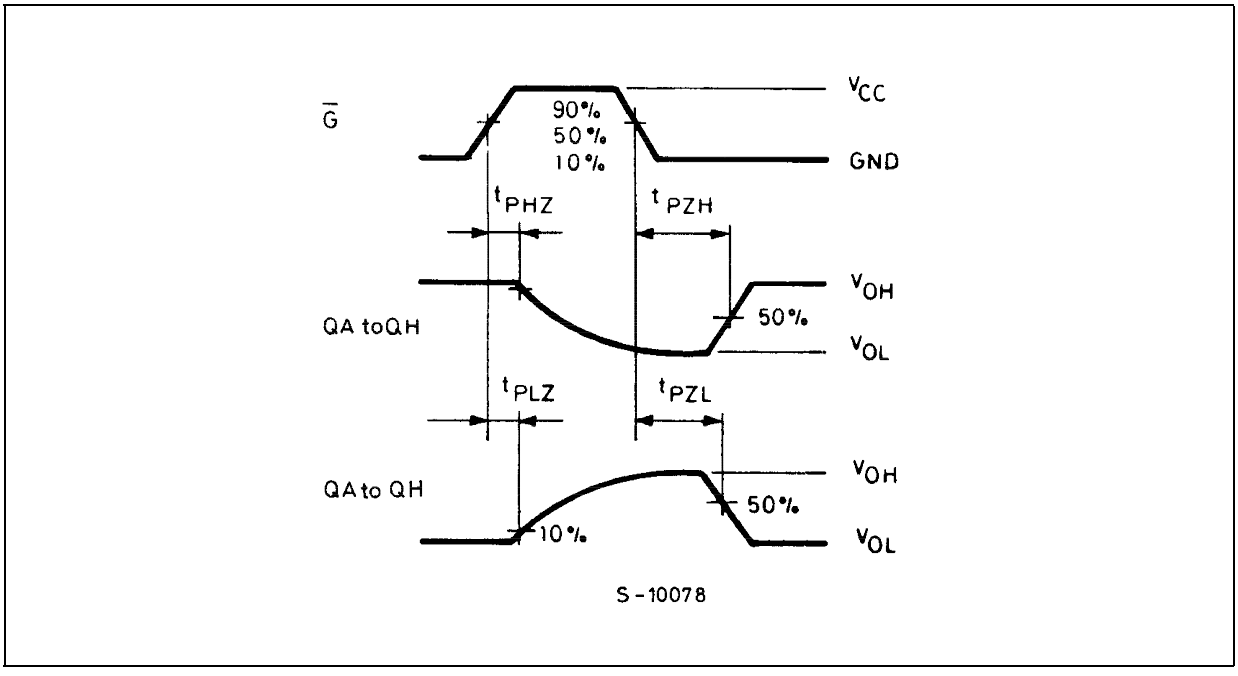
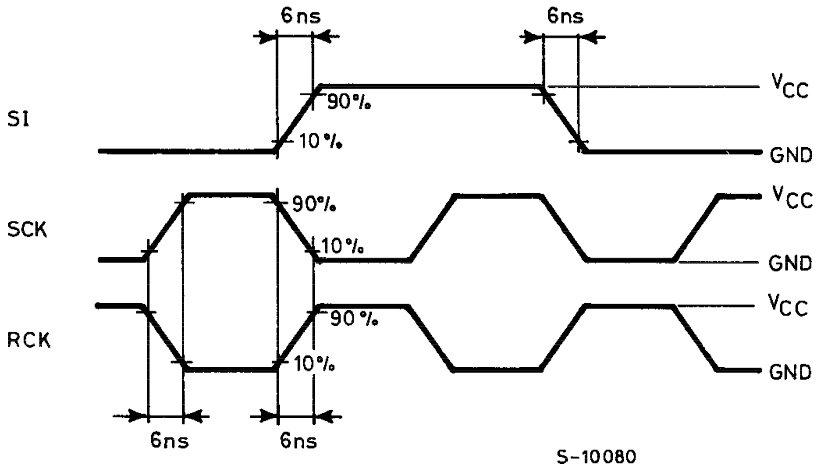
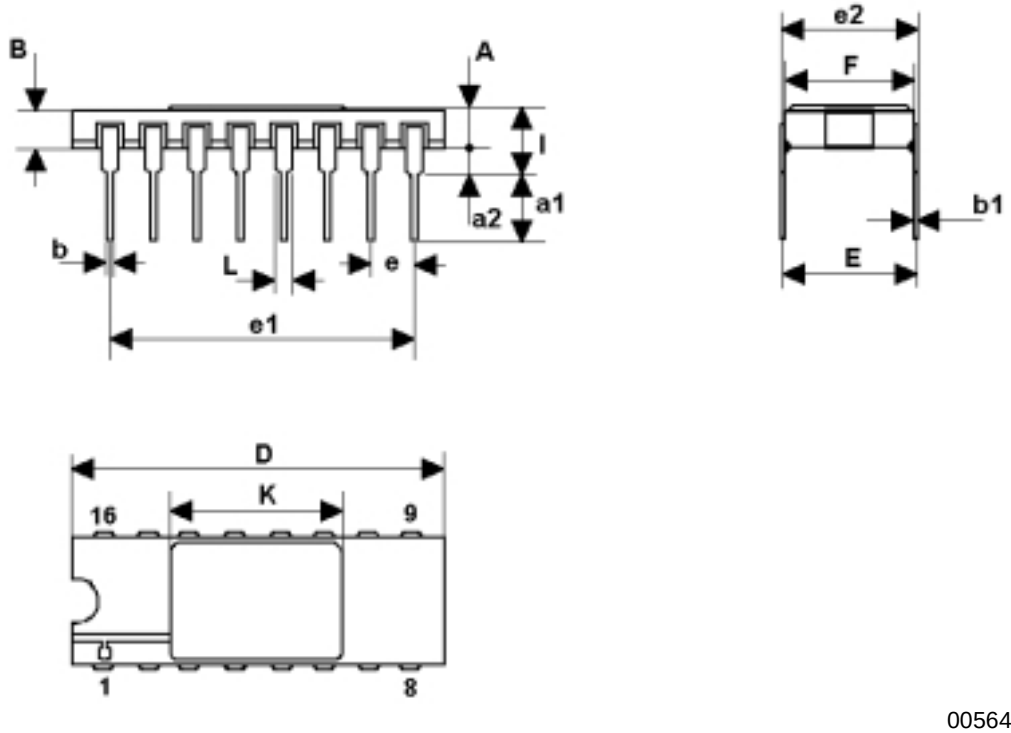


Figure 14: Waveform - Input Waveform (f=1MHz; 50% duty cycle)



DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	17.65	17.78	17.90	0.695	0.700	0.705
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	

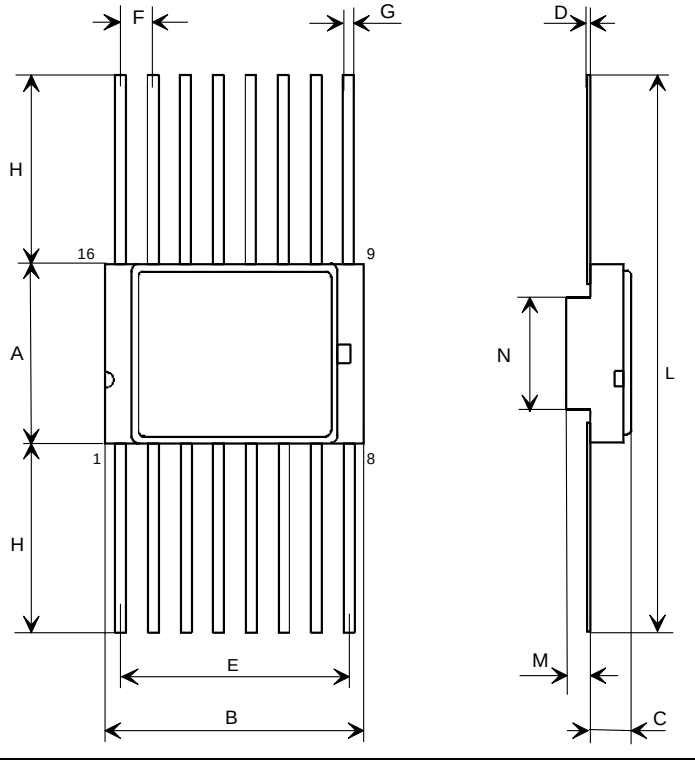

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Table 8: Revision History

Date	Revision	Description of Changes
01-Jun-2004	1	First Release