TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCXR162500FT

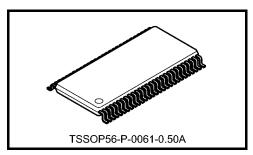
Low-Voltage 18-Bit Universal Bus Transceiver with 3.6-V Tolerant Inputs and Outputs

The TC74VCXR162500FT is a high-performance CMOS 18-bit universal bus transceiver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CKAB and CKBA) inputs.

For A-to-B data flow, the device operates in the transparent mode when \underline{LEAB} is high. When \underline{LEAB} is low, the A data is latched if \overline{CKAB} is held at a high or low logic level. If \underline{LEAB} is



Weight: 0.25 g (typ.)

low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of CKAB.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CKBA.

When the \overline{OE} input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The $26-\Omega$ series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.

Features (Note)

- 26-Ω series resistors on outputs
- Low-voltage operation: VCC = 1.8 to 3.6 V
- High-speed operation: $t_{pd} = 3.8 \text{ ns (max) (V}_{CC} = 3.0 \text{ to } 3.6 \text{ V)}$

 $t_{pd} = 4.9 \text{ ns (max) (VCC} = 2.3 \text{ to } 2.7 \text{ V)}$

 $: t_{pd} = 9.8 \text{ ns (max) (VCC} = 1.8 \text{ V)}$

• Output current: $I_{OH}/I_{OL} = \pm 12 \text{ mA (min)} (V_{CC} = 3.0 \text{ V})$

 $: I_{OH}/I_{OL} = \pm 8 \text{ mA (min) (V}_{CC} = 2.3 \text{ V)}$

: $I_{OH}/I_{OL} = \pm 4$ mA (min) ($V_{CC} = 1.8$ V)

- Latch-up performance: -300 mA
- ESD performance: Machine model ≥ ±200 V

Human body model $\geq \pm 2000 \text{ V}$

- Package: TSSOP
- Bidirectional interface between 2.5 V and 3.3 V signals.
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

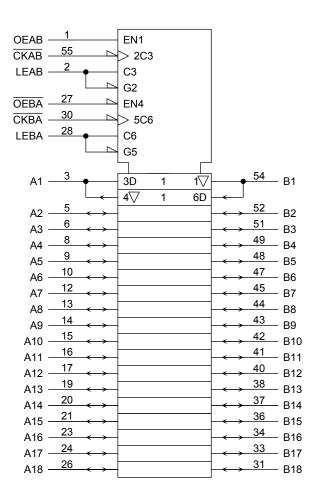
Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)

56 GND **OEAB LEAB** 2 55 CKAB Α1 3 54 В1 4 GND **GND** 53 A2 5 52 B2 А3 6 ВЗ 51 7 V_{CC} 50 V_{CC} 8 B4 A4 49 A5 48 В5 A6 10 В6 GND 11 46 **GND** A7 12 В7 45 A8 13 В8 В9 A9 14 43 A10 15 42 B10 A11 16 B11 A12 17 B12 GND 18 GND 39 A13 19 38 B13 A14 20 37 B14 B15 A15 21 36 V_{CC} 22 35 V_{CC} A16 23 34 B16 A17 24 33 B17 GND 25 32 **GND** A18 26 31 B18 OEBA 27 30 CKBA LEBA 28 GND 29

IEC Logic Symbol





Truth Table (A bus → B bus)

	Inputs					
OEAB	LEAB	CKAB	Α	В		
L	Х	Х	Х	Z		
Н	Н	Х	L	L		
Н	Н	Х	Н	Н		
Н	L	\neg	L	L		
Н	L	$\overline{}$	Н	Н		
Н		Н	X	В0		
П	L	П	^	(Note)		
Н			X	В0		
	L	L	^	(Note)		

Note: Output level before the indicated steady-state input conditions were established, provided that CKAB was low or high before LEAB went low.

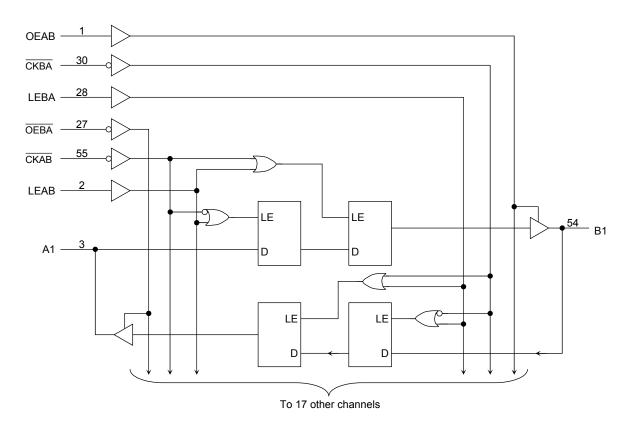
Truth Table (B bus → A bus)

	Inputs					
OEBA	LEBA	CKBA	В	Α		
Н	Х	Х	Х	Z		
L	Н	Х	L	L		
L	Н	Х	Н	Н		
L	L	\neg	L	L		
L	L	\neg	Н	Н		
		Н	Х	A0		
L	L	П	^	(Note)		
			X	A0		
	L	L	^	(Note)		

Note: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CKBA}}$ was low or high before LEBA went low.

3

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 4.6	V
DC input voltage (OEAB, <u>OEBA</u> , <u>LEAB</u> , LEBA, CKAB, CKBA)	V _{IN}	-0.5 to 4.6	٧
		-0.5 to 4.6 (Note 2)	
DC bus I/O voltage	$V_{I/O}$	-0.5 to V _{CC} + 0.5	V
		(Note 3)	
Input diode current	I _{IK}	-50	mA
Output diode current	lok	±50 (Note 4)	mA
DC output current	lout	±50	mA
Power dissipation	P_{D}	400	mW
DC V _{CC} /ground current per supply pin	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 2: OFF state
- Note 3: High or low state. IOUT absolute maximum rating must be observed.
- Note 4: $V_{OUT} < GND, V_{OUT} > V_{CC}$



Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit	
Dowar cupply voltage	Vaa	1.8 to 3.6	V	
Power supply voltage	V _{CC}	1.2 to 3.6 (Note 2)	V	
Input voltage (OEAB, OEBA, LEAB, LEBA, CKAB, CKBA)	V _{IN}	-0.3 to 3.6	٧	
Bus I/O voltage	Vivo	0 to 3.6 (Note 3)	V	
bus I/O vollage	V _{I/O}	0 to V _{CC} (Note 4)	V	
		±12 (Note 5)		
Output current	I _{OH} /I _{OL}	±8 (Note 6)	mA	
		±4 (Note 7)		
Operating temperature	T _{opr}	-40 to 85	°C	
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V	

- Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

 Unused inputs must be tied to either VCC or GND.
- Note 2: Data retention only
- Note 3: OFF state
- Note 4: High or low state
- Note 5: $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
- Note 6: $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$
- Note 7: $V_{CC} = 1.8 \text{ V}$
- Note 8: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

5



Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C, 2.7 V < $V_{CC} \leq 3.6 \ V)$

Characteri	stics	Symbol	Test Co	ondition	V _{CC} (V)	Min	Max	Unit							
Innut voltage	H-level	V _{IH}	_	_	2.7 to 3.6	2.0	_	V							
Input voltage	L-level	V _{IL}	-	_	2.7 to 3.6	_	0.8	V							
				I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2									
	H-level	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -6 mA	2.7	2.2	_								
				$I_{OH} = -8 \text{ mA}$	3.0	2.4									
Output voltage				$I_{OH} = -12 \text{ mA}$	3.0	2.2		V							
		Vol	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	2.7 to 3.6	_	0.2								
	L-level			$I_{OL} = 6 \text{ mA}$	2.7	_	0.4								
	L-level	VOL		AIN - AIH OI AIL	VIN - VIH OI VIL	VIN - VIH OI VIL	AIM — AIH OL AIF	VIN - VIH OI VIL	VIIV — VIH OI VIL	AIM — AIM OL AIC	$I_{OL} = 8 \text{ mA}$	3.0	_	0.55	
				I _{OL} = 12 mA	3.0	_	0.8								
Input leakage curre	nt	I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	_	±5.0	μΑ							
2 state output OFF	otata aurrant	loz	$V_{IN} = V_{IH}$ or V_{IL}		2.7 to 3.6		±10.0	μА							
3-state output OFF	3-state output OFF state current		V _{OUT} = 0 to 3.6 V		2.7 10 3.0		±10.0	μА							
Power-off leakage of	urrent	I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	_	10.0	μΑ							
Quincoant aupply aurrant		Icc	V _{IN} = V _{CC} or GND		2.7 to 3.6	_	20.0								
Quiescent supply ct	Quiescent supply current		$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6 \text{ V}$		2.7 to 3.6	_	±20.0	μΑ							
Increase in I _{CC} per	input	Δlcc	$V_{IH} = V_{CC} - 0.6 V$		2.7 to 3.6	_	750								

DC Characteristics (Ta = -40 to 85°C, 2.3 V \leq V_{CC} \leq 2.7 V)

Characte	ristics	Symbol	Test Condition		Test Condition		V _{CC} (V)	Min	Max	Unit						
	H-level	V _{IH}		_	2.3 to 2.7	1.6	_									
Input voltage	L-level	V _{IL}		_	2.3 to 2.7	_	0.7	V								
				I _{OH} = -100 μA	2.3 to 2.7	V _{CC} - 0.2	_									
	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -4 mA	2.3	2.0	_									
												I _{OH} = -6 mA	2.3	1.8	_	
Output voltage				I _{OH} = -8 mA	2.3	1.7	_	V								
				I _{OL} = 100 μA	2.3 to 2.7	_	0.2									
	L-level	V _{OL}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OL} = 6 mA	2.3	_	0.4									
				I _{OL} = 8 mA	2.3	_	0.6									
Input leakage curre	ent	I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	_	±5.0	μА								
3-state output OFF state current I _{O2}		la-	$V_{IN} = V_{IH}$ or V_{IL}		2.3 to 2.7		±10.0									
		102	V _{OUT} = 0 to 3.6 V		2.3 10 2.7	_	±10.0	μΑ								
Power-off leakage	current	l _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0		10.0	μА								
Outro and supply supply			V _{IN} = V _{CC} or GND		2.3 to 2.7		20.0	μА								
Quiescent supply	Current	Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le$	3.6 V	2.3 to 2.7	_	±20.0	μΑ								



DC Characteristics (Ta = -40 to 85°C, 1.8 V \leq V_{CC} < 2.3 V)

Characteristics		Symbol	Test C	ondition		Min	Max	Unit
		Í			V _{CC} (V)			
Input voltage	H-level	V _{IH}	-	_	1.8 to 2.3	$\begin{array}{c} 0.7 \times \\ V_{CC} \end{array}$	_	V
input voitage	L-level	V _{IL}	_	_	1.8 to 2.3		0.2 × V _{CC}	V
	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	1.8	V _{CC} - 0.2	_	
Output voltage				I _{OH} = -4 mA	1.8	1.4	_	V
	L-level	\/a.	V. V. or V.	$I_{OL} = 100 \mu A$	1.8	_	0.2	
	L-level	V _{OL}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OL} = 4 mA	1.8	_	0.3	
Input leakage currer	nt	I _{IN}	V _{IN} = 0 to 3.6 V		1.8	_	±5.0	μА
3-state output OFF	state current	I _{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 0 \text{ to } 3.6 \text{ V}$			_	±10.0	μА
Power-off leakage of	urrent	I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	_	10.0	μА
Quioscont supply of	ırront	loo	V _{IN} = V _{CC} or GND		1.8		20.0	^
Quiescent supply cu	<u></u>	Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6 \text{ V}$		1.8	_	±20.0	μА



AC Characteristics (Ta = -40 to 85°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500~\Omega$) (Note 1)

Characteristics	Symbol	Test Condition		Min	Max	Unit
Characteriolis	Cymbol	Took Condition	V _{CC} (V)		Max	O.m.
			1.8	100		
Maximum clock frequency	f _{max}	Figure 1, Figure 3	2.5 ± 0.2	200	_	MHz
			3.3 ± 0.3	250	_	
Dranagation dalay time	•		1.8	1.5	9.8	
Propagation delay time (An, Bn-Bn, An)	t _{pLH}	Figure 1, Figure 2	2.5 ± 0.2	0.8	4.9	ns
(All, Bli-Bli, All)	t _{pHL}		3.3 ± 0.3	0.6	3.8	
Dranagation delay time	•		1.8	1.5	9.8	
Propagation delay time (CKAB , CLKBA -Bn, An)	t _{pLH}	Figure 1, Figure 3	2.5 ± 0.2	8.0	6.7	ns
(CNAD, CLNDA-BII, AII)	t _{pHL}		3.3 ± 0.3	0.6	5.1	
Propagation delay time	•		1.8	1.5	9.8	
(LEAB, LEBA-Bn, An)	t _{pLH}	Figure 1, Figure 4	2.5 ± 0.2	8.0	6.3	ns
(LEAD, LEDA-DII, AII)	t _{pHL}		3.3 ± 0.3	0.6	4.7	
Outroit analys times		Figure 1, Figure 5, Figure 6	1.8	1.5	9.8	
Output enable time (OEAB, OEBA -Bn, An)	t _{pZL} t _{pZH}		2.5 ± 0.2	0.8	5.9	ns
(OEAB, OEBA-BII, AII)			3.3 ± 0.3	0.6	4.3	
Output disable time		Figure 1, Figure 5, Figure 6	1.8	1.5	8.8	ns
Output disable time (OEAB, OEBA -Bn, An)	t _{pLZ}		2.5 ± 0.2	0.8	4.9	
(OEAB, OEBA-BII, AII)	t _{pHZ}		3.3 ± 0.3	0.6	4.3	
			1.8	4.0	_	
Minimum pulse width	t _{W (H)}	Figure 1, Figure 3, Figure 4	2.5 ± 0.2	1.5	_	ns
	t _{W (L)}		3.3 ± 0.3	1.5	_	
			1.8	2.5	_	
Minimum setup time	ts	Figure 1, Figure 3, Figure 4	2.5 ± 0.2	1.5		ns
			3.3 ± 0.3	1.5	_	
			1.8	1.0		
Minimum hold time	th	Figure 1, Figure 3, Figure 4	2.5 ± 0.2	1.0	_	ns
			3.3 ± 0.3	1.0	_	
			1.8	_	0.5	
Output to output skew	t _{osLH}	(Note 2)	2.5 ± 0.2	_	0.5	ns
	t _{osHL}		3.3 ± 0.3	_	0.5	

8

Note 1: For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design. $(t_{OSLH} = |t_{DLHm} - t_{DLHn}|, \, t_{OSHL} = |t_{DHLm} - t_{DHLn}|)$



Dynamic Switching Characteristics

(Ta = 25°C, input: $t_r = t_f = 2.0 \text{ ns}, C_L = 30 \text{ pF}, R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 1.8	0.15	
Quiet output maximum dynamic V _{OI}	V _{OLP}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 2.5	0.25	٧
3, 1 3, 2		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 3.3	0.35	
	V _{OLV}	$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 1.8	-0.15	
Quiet output minimum dynamic V _{OI}		$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 2.5	-0.25	V
, 62		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 3.3	-0.35	
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 1.8	1.55	
Quiet output minimum dynamic V _{OH}	V _{OHV}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 2.5	2.05	V
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (No	e) 3.3	2.65	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

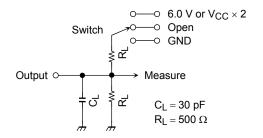
Characteristics	Symbol	Test Condition		Тур.	Unit
Cridiacteristics	Symbol	rest condition	V _{CC} (V)		Offic
Input capacitance	C _{IN}	_	1.8, 2.5, 3.3	6	pF
Bus I/O capacitance	C _{I/O}	_	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note	1.8, 2.5, 3.3	20	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18 \text{ (per bit)}$

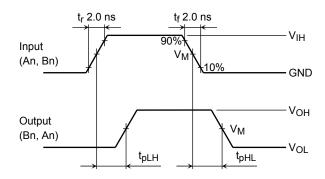
AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
t _{pHZ} , t _{pZH}	GND

Figure 1

AC Waveform



Symbol	Vcc							
Syllibol	$3.3\pm0.3~\textrm{V}$	$2.5\pm0.2\textrm{V}$	1.8 V					
V _{IH}	2.7 V	V _{CC}	V _{CC}					
V _M	1.5 V	V _{CC} /2	V _{CC} /2					
VX	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V					
VY	V _{OH} – 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V					

Figure 2 t_{pLH}, t_{pHL}

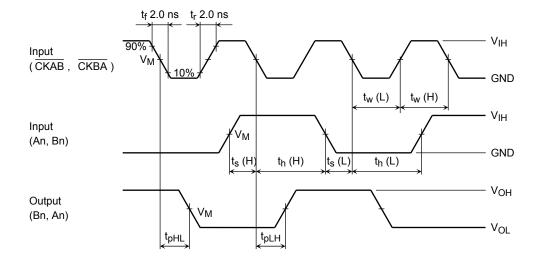


Figure 3 t_{pLH} , t_{pHL} , t_w , t_s , t_h

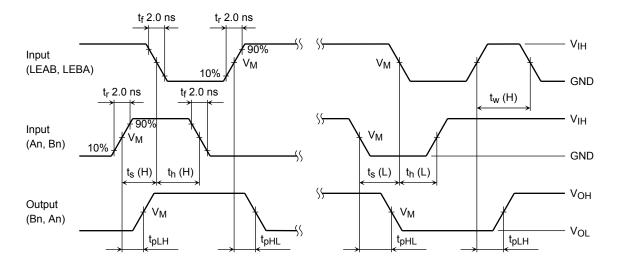


Figure 4 tpLH, tpHL, tw, ts, th

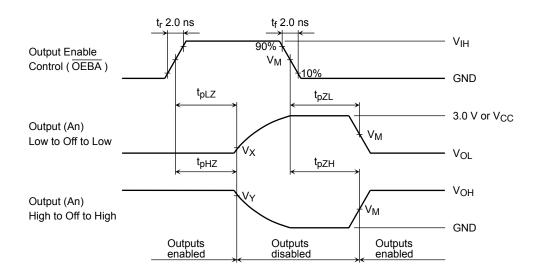


Figure 5 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

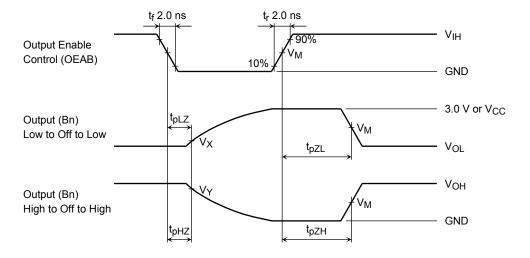
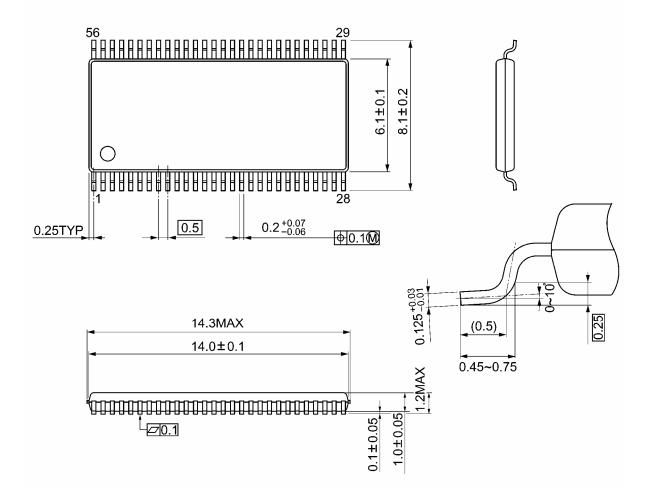


Figure 6 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Package Dimensions

TSSOP56-P-0061-0.50A Unit: mm



Weight: 0.25 g (typ.)

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20070701-EN GENERAL

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