Elektronische Bauelemente

SEMP8965

Fast Ultra High-PSRR, Low Noise, Low-Dropout, 600 mA Micropower CMOS Linear Regulator

RoHS Compliant Product
A suffix of "-C" specifies halogen or lead -free

DESCRIPTION

The SEMP8965 low-dropout (LDO) CMOS linear regulators, consisting of SEMP8965, SEMP8966, and SEMP8968, feature ultra-high power supply rejection ratio (75dB at 1kHz), low output voltage noise (30μV), low dropout voltage (270mV), low quiescent current (110μA), and fast transient response. It guarantees delivery of 600mA output current, and supports preset (1.2V~3.3V with 0.1V increment, except for 1.85V and 2.85V) as well as adjustable (1.2V to 5.0V) output voltage versions.

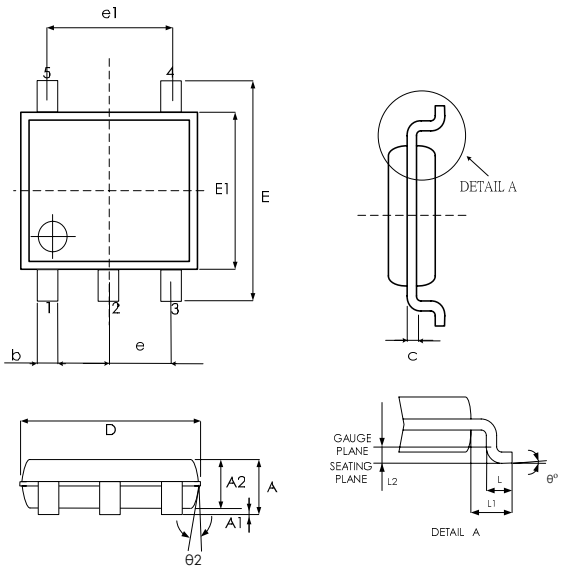
The SEMP8965 is ideal for battery-powered applications by virtue of its low quiescent current consumption and its 1nA shutdown mode of logical operation. The regulator provides fast turn-on and start-up time by using dedicated circuitry to pre-charge an optional external bypass capacitor. This bypass capacitor is used to reduce the output voltage noise without adversely affecting the load transient response. The high power supply rejection ratio of the SEMP8965 holds well for low input voltages typically encountered in battery- operated systems. The regulator is stable with small ceramic capacitive loads (2.2μF typical).

Additional features include regulation fault detection, band-gap voltage reference, constant current limiting and thermal overload protection.

FEATURES

- 600mA guaranteed output current
- 75dB typical PSRR at 1kHz
- 30μV RMS output voltage noise (10Hz to 100kHz)
- 270mV typical dropout at 600mA
- 110μA typical quiescent current
- 1nA typical shutdown mode
- Fast line and load transient response
- 80μs typical fast turn-on time
- 2.5V to 5.5V input range
- Stable with small ceramic output capacitors
- Over temperature and over current protection
- ±2% output voltage tolerance

PACKAGE DIMENSIONS



SOT-25

SYMBOLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0	-	0.15
A2	1.00	1.10	1.20
b	0.30	-	0.55
c	0.08	-	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
θ°	0	5	10
θ2°	6	8	10

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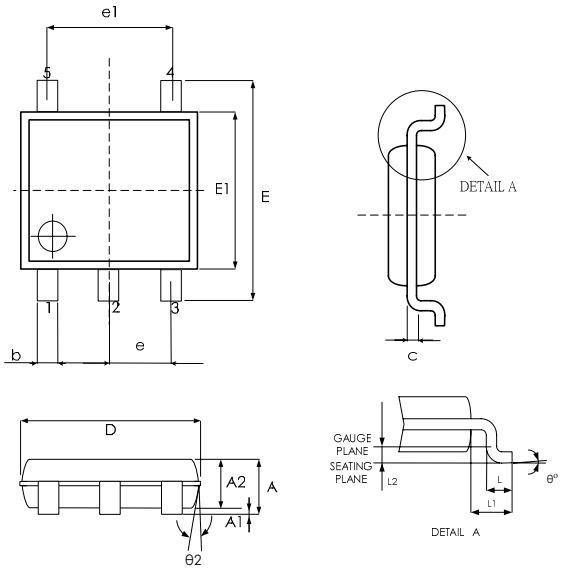


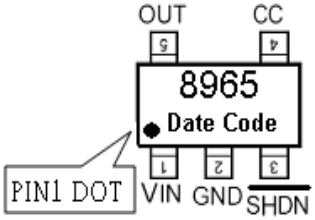
MSOP-8

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.1
A1	0	-	0.15
A2	0.75	0.85	0.95
D			3.00 BSC
E			4.90 BSC
E1			3.00 BSC
L	0.40	0.60	0.80
L1	0.95 BSC		
θ°	0	-	8

APPLICATIONS

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

MARKING & PACKING INFORMATION



Vout Code	Vout	Order Information
12	1.2	SEMP8965-12
15	1.5	SEMP8965-15
18	1.8	SEMP8965-18
25	2.5	SEMP8965-25
30	3.0	SEMP8965-30
33	3.3	SEMP8965-33

PIN FUNCTIONS

Symbol	Pin #	Function
V_{IN}	1	Supply Voltage Input. Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
G_{ND}	2	Ground Pin.
$\overline{SHDN}$	3	Shutdown Input. Set the regulator into the disable mode by pulling the SHDN pin low. To keep the regulator on during normal operation, connect the SHDN pin to VIN. The SHDN pin must not exceed VIN under all operating conditions.
CC	4	Compensation Capacitor. Connect an optimum 33nF noise bypass capacitor between the CC and the ground pins to reduce noise in VOUT.
V_{OUT}	5	Output Voltage Feedback.

MAXIMUM RATINGS

Parameter		Value	Units
VIN, VOUT, $V_{\overline{SHDN}}$, VSET, VCC, $V_{\overline{FAULT}}$		-0.3 ~ 6.0	V
Supply Voltage		2.5 ~ 5.5	V
Power Dissipation		(Note 3)	W
ESD Susceptibility		HBM (Note 5) 2	kV
Temperature	Lead (10 sec.)	260	°C
	Storage (T_{STG})	-65 ~ +160	
(Note 1)(Note 2)	Operating (T_{OPR})	-40 ~ 85	
	Junction (T_J)	150	

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_{OUT}$ +1V (Note 6), $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$. **Boldface** limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
V_{IN}	Input Voltage		2.5		5.5	V
ΔV_{OTL}	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 300mA $V_{OUT\ (NOM)}$ +0.5V ≤ VIN ≤ 5.5V (Note 6)	-2		+2	% of $V_{OUT\ (NOM)}$
		ADJ/NC=VOUT for the Adjust Versions	-3		+3	
V_{OUT}	Output Adjust Range	Adjust Version Only	1.20		5.0	V
I_{OUT}	Maximum Output Current	Average DC Current Rating	600			mA
I_{LIMIT}	Output Current Limit		600	950		mA
I_Q	Supply Current	I_{OUT} = 0mA		110		µA
		I_{OUT} = 600mA		255		
	Shutdown Supply Current	V_{OUT} = 0V, $\overline{SHDN}$ = GND		0.001	1	
V_{DO}	Dropout Voltage (MSOP-8) (Note 4), (Note 6)	I_{OUT} = 50mA		19		mV
		I_{OUT} = 300mA		110		
		I_{OUT} = 600mA		230		
	Dropout Voltage (SOT-25, SOT-26) (Note 4), (Note 6)	I_{OUT} = 50mA		22		
		I_{OUT} = 300mA		130		
		I_{OUT} = 600mA		270		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 7)	-0.1	0.02	0.1	%/V
	Load Regulation	100µA ≤ I_{OUT} ≤ 600mA		0.001		%/mA
e_n	Output Voltage Noise	I_{OUT} = 10mA, 10Hz ≤ f ≤ 100kHz		30		μV_{RMS}
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{IH}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 6)	1.2			V
		V_{IL}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 6)			0.4	
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or VIN		0.1	100	nA
$I_{ADJ/NC}$	ADJ/NC Input Leakage	ADJ/NC=1.3V, Adjust Version Only (Note 9)		0.1	3	nA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Detection Voltage	V_{OUT} ≥ 2.5V, I_{OUT} = 200mA (Note 10)		125		mV
	$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 2mA		0.2		V

$I_{\overline{FAULT}}$	$\overline{FAULT}$ Off-Leakage Current	$\overline{FAULT}$ = 3.6V, $\overline{SHDN}$ = 0V		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			165		℃
	Thermal Shutdown Hysteresis			30		
T_{ON}	Start-Up Time	C_{OUT} = 10μF, V_{OUT} at 90% of Final Value		80		μs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The maximum power dissipation is found to be 561mW. The derating factor ($-1/\theta_{JA}$) = -4.5mW/°C, thus below 25°C the power dissipation figure can be increased by 4.5mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 4: Typical Values represent the most likely parametric norm.

Note 5: Human body model: 1.5k Ω in series with 100pF.

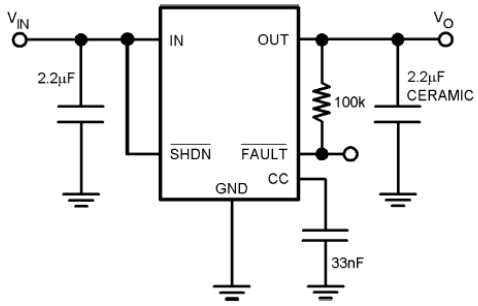
Note 6: Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.

Note 7: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 0.5V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.5V.

Note 8: The ADJ/NC pin is disconnected internally for the preset versions.

Note 9: The $\overline{FAULT}$ detection voltage is specified for the input to output voltage differential at which the $\overline{FAULT}$ pin goes active low.

TYPICAL APPLICATION



BLOCK DIAGRAM

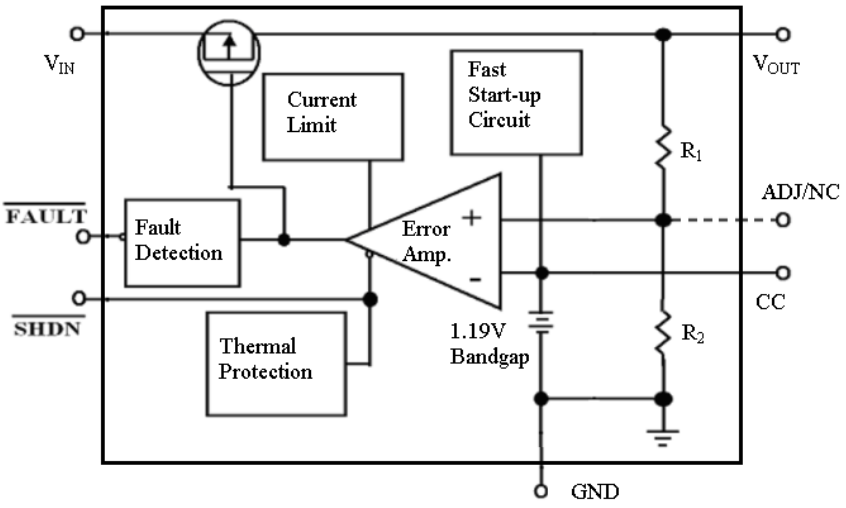


Fig.1a. The SEMP8965 Functional Block Diagram
(Preset Version with the ADJ/NC Pin Disconnected internally)

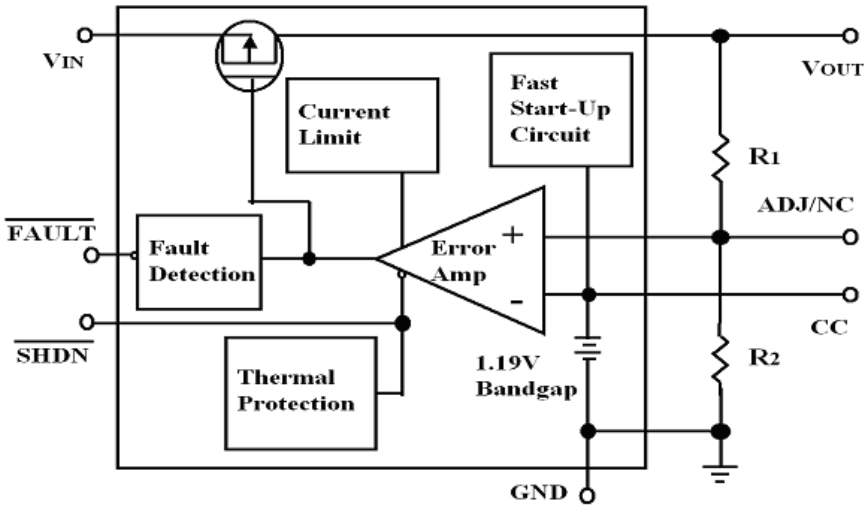
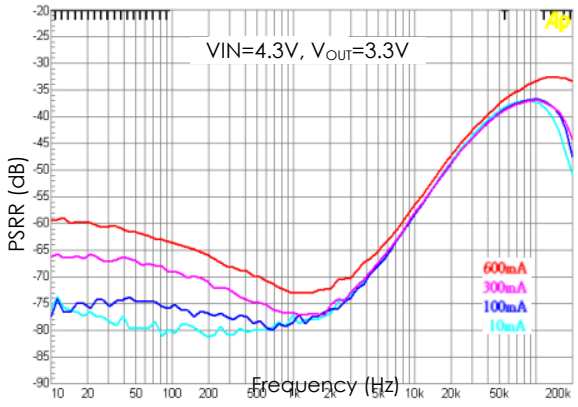


Fig.1b. The SEMP8965 Functional Block Diagram
(Adjustable Version with the ADJ/NC Pin Connected to External Resistors R1 and R2)

TYPICAL CHARACTERISTICS

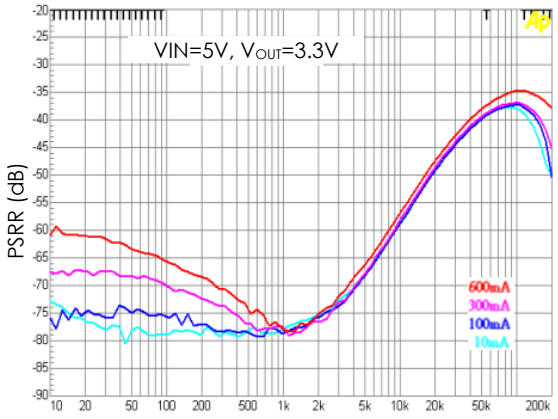
Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN.

PSRR vs. Frequency



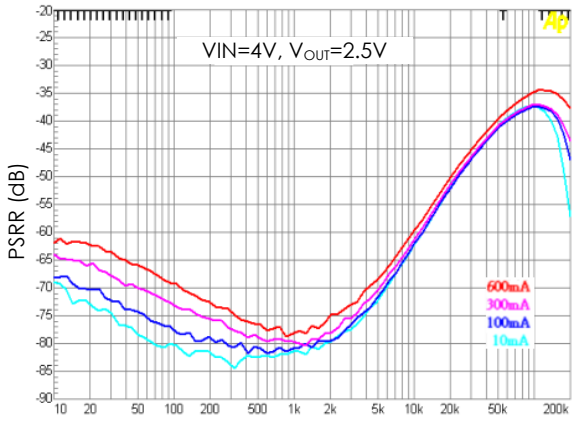
Frequency (Hz)

PSRR vs. Frequency



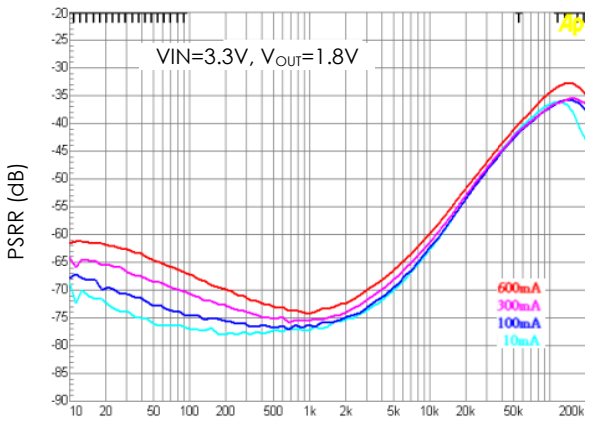
Frequency (Hz)

PSRR vs. Frequency



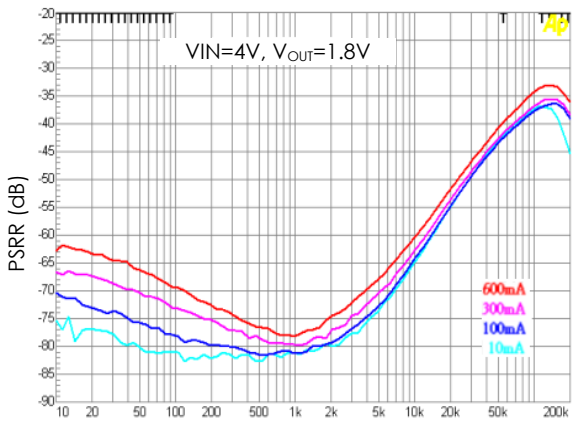
Frequency (Hz)

PSRR vs. Frequency



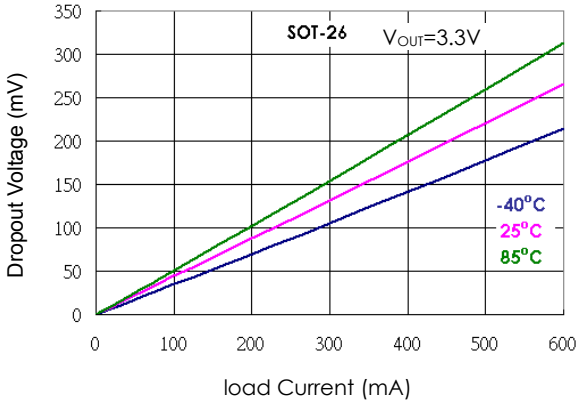
Frequency (Hz)

PSRR vs. Frequency



Frequency (Hz)

Dropout Voltage vs. Load Current

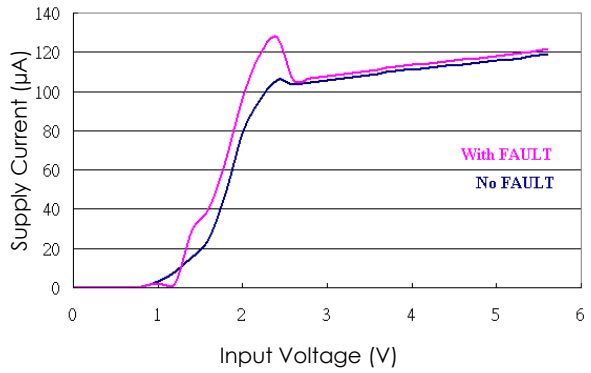


load Current (mA)

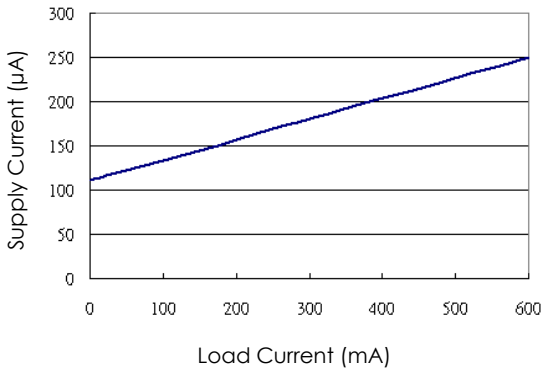
TYPICAL CHARACTERISTICS

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN. (cont'd)

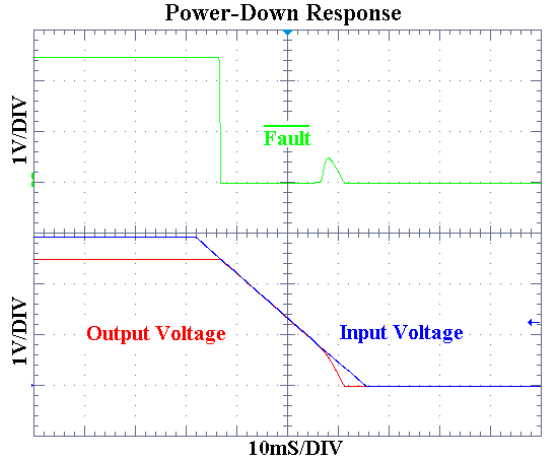
Supply Current vs. Input Voltage



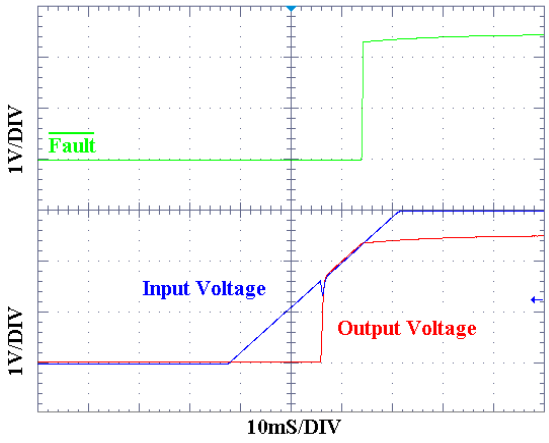
Supply Current vs. Load Current



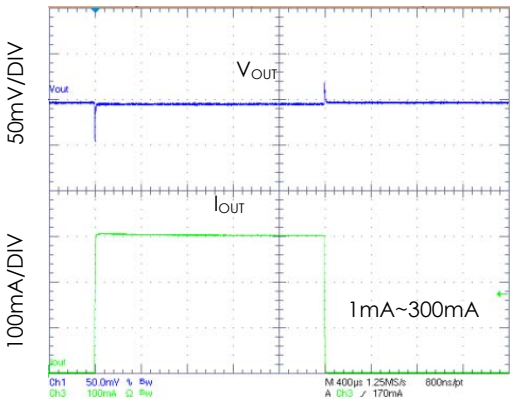
Power-Down Response



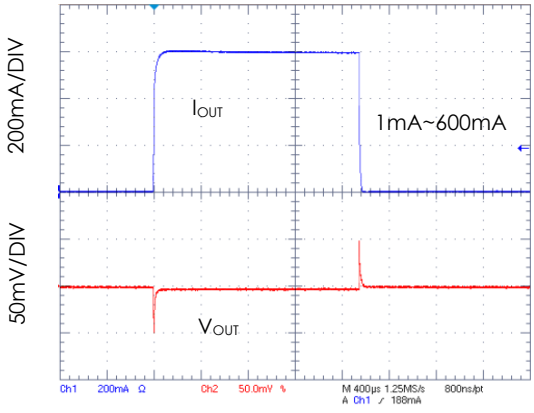
Power-Up Response



Load Transient



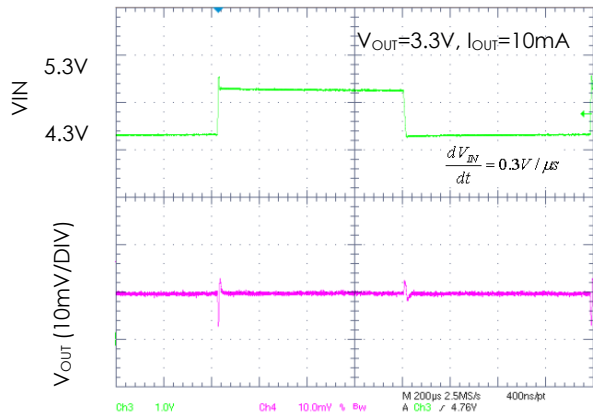
Load Transient



TYPICAL CHARACTERISTICS

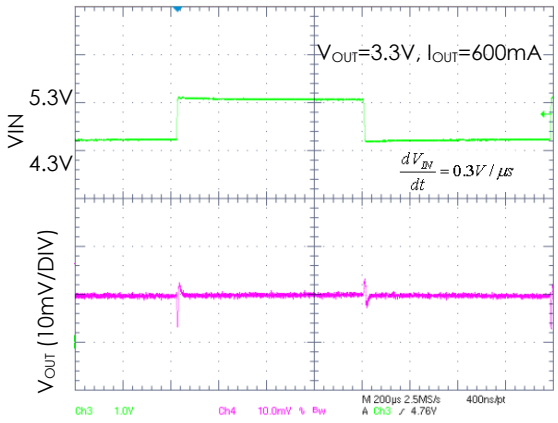
Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN. (cont'd)

Line Transient



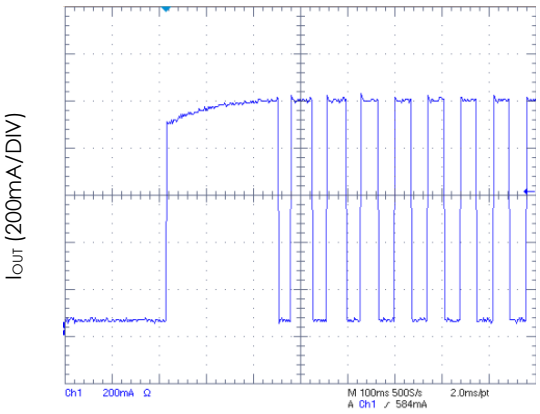
200µs/DIV

Line Transient



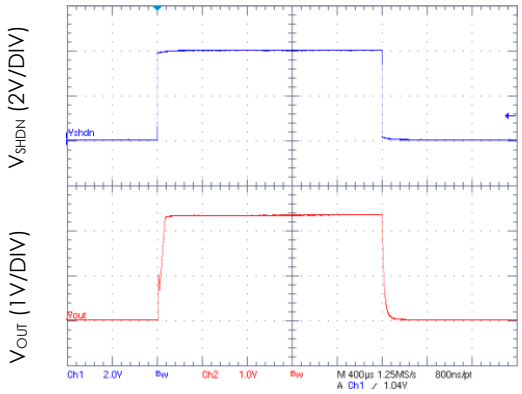
200µs/DIV

Current Limit



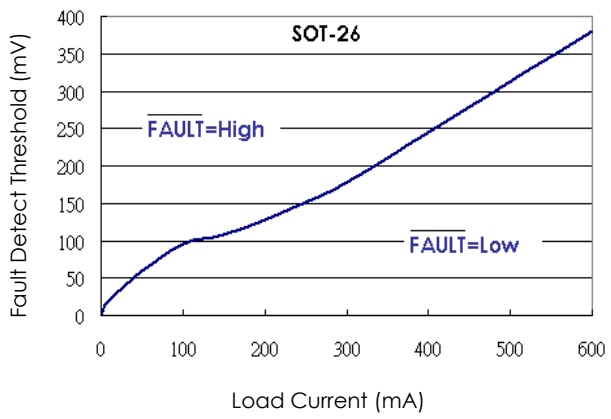
100ms/DIV

Enable and Disable



400µs/DIV

Fault Detection Threshold vs. Load Current



APPLICATION INFORMATION

GENERAL DESCRIPTION

Referring to Figure 1 as shown in the Functional Block Diagram section, the SEMP8965 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage. These feedback resistors can be either internal or external to the SEMP8965, depending on whether a preset or an adjustable output voltage version is being used.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

OUTPUT VOLTAGE CONTROL (Adjustable Version Only)

The SEMP8965 allows direct user control of the output voltage in accordance with the amount of negative feedback present. To see the explicit relationship between the output voltage and the negative feedback, it is convenient to conceptualize the SEMP8965 as an ideal non-inverting operational amplifier with a fixed DC reference voltage VREF at its non-inverting input. Such a conceptual representation of the SEMP8965 in closed-loop configuration is shown in Figure 2. This ideal op amp features an ultra-high input resistance such that its inverting input voltage is virtually fixed at VREF. The output voltage is therefore given by:

$$V_{OUT} = V_{REF}\left[\frac{R_1}{R_2} + 1\right]$$

This equation can be rewritten in the following form to facilitate the determination of the resistor values for a chosen output voltage:

$$R_1 = R_2\left[\frac{V_{OUT}}{1.19V} - 1\right]$$

Set R2 equal to 100kΩ to optimize for overall accuracy, power supply rejection, noise, and power consumption.

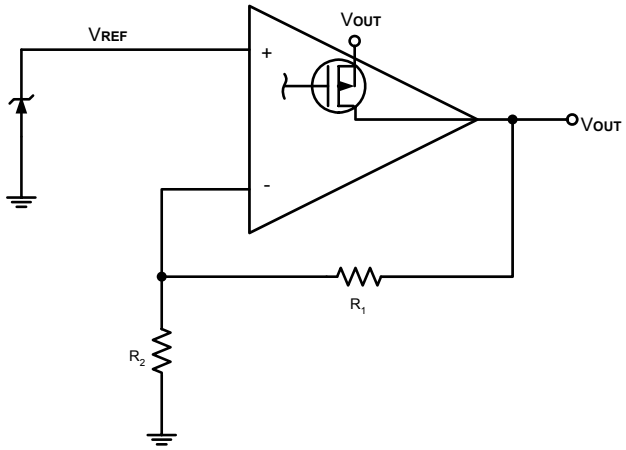


Figure 2. Simplified Regulator Topology

OUTPUT CAPACITOR

The SEMP8965 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the SEMP8965 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The SEMP8965 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

INPUT CAPACITOR

A minimum input capacitance of 1μF is required for SEMP8965. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

COMPENSATION (NOISE BYPASS) CAPACITOR

Substantial reduction in the output voltage noise of the SEMP8965 is accomplished through the connection of the noise bypass capacitor CC (33nF optimum) between pin 6 and the ground. Because pin 6 connects directly to the high impedance output of the bandgap reference circuit, the level of the DC leakage currents in the CC capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the CC capacitor types for use with the SEMP8965. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the CC capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Tradeoff exists between output noise level and turn-on time when selecting the CC capacitor value.

POWER DISSIPATION AND THERMAL SHUTDOWN

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The SEMP8965 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θJA and TJ is as follows:

$T_J = \theta_{JA} (PD) + T_A$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$P_D = I_{OUT} (V_{IN} - V_{OUT})$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the SEMP8965, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

FAULT DETECTION

In the event of the occurrence of various fault conditions that cause failure in the output voltage regulation, such as during thermal overload or current limit, the $\overline{FAULT}$ pin of the SEMP8965 becomes low. Because the $\overline{FAULT}$ pin connects to the open-drain output of a N-channel MOS transistor, a large pull-up resistor (100kΩ typical) is required to provide the necessary output voltage and yet without compromising the overall power consumption performance of the regulator. The $\overline{FAULT}$ pin also goes low when the input-to-output differential voltage becomes too small to sustain good load and line regulation at the output. This occurs typically during near dropout when the input-to-output differential voltage is less than 110mV for a load current of 200mA. The SEMP8965 detects near dropout conditions by comparing the differential voltage against a predefined differential threshold that is always slightly above the dropout voltage. This differential threshold is dynamical in the sense that it not only tracks the dropout voltage as the load current varies, but also scale linearly with the load current.

SHUTDOWN

The SEMP8965 enters the sleep mode when the $\overline{SHDN}$ pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the SEMP8965 best suited for battery-powered applications. The maximum guaranteed voltage at the $\overline{SHDN}$ pin for the sleep mode to take effect is 0.4V. A minimum guaranteed voltage of 1.2V at the $\overline{SHDN}$ pin will activate the SEMP8965. Direct connection of the $\overline{SHDN}$ pin to the VIN to keep the regulator on is allowed for the SEMP8965. In this case, the $\overline{SHDN}$ pin must not exceed the supply voltage VIN.

FAST START-UP

Fast start-up time is important for overall system efficiency improvement. The SEMP8965 assures fast start-up speed when using the optional noise bypass capacitor (CC). To shorten start-up time, the SEMP8965 internally supplies a 500μA current to charge up the capacitor until it reaches about 90% of its final value.