CoreAHB2APB

DirectCore

Key Features

- Supplied in SysBASIC Core Bundle
- Bridges between Advanced Microcontroller Bus Architecture (AMBA) Advanced High-Performance Bus (AHB) and Advanced Peripheral Bus (APB)
- Up to 16 APB Slave Devices Supported
- Automatic Connection to CoreAHB and CoreAPB in CoreConsole

Benefits

- Allows Easy Connection of APB Devices to a CoreMP7 or Cortex-M1 Subsystem
- Auto Stitch in CoreConsole for Rapid Development
- Compatible with AMBA, CoreMP7, and Cortex-M1

Supported Device Families

- Fusion
- IGLOO™
- IGLOOe
- ProASIC®3L
- ProASIC3
- ProASIC3E

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

CoreAHB2APB (AMBA Bridge) is an AHB slave that links the AHB bus to the APB bus and acts as the Master on the APB bus. Address decoding for the APB bus is carried out within CoreAHB2APB, and this provides select signals for up to 16 APB slave slots.

Read and write transfers on the AHB bus are converted to corresponding transfers on the APB bus. High-bandwidth peripherals, such as memory controllers, are typically connected to the AHB, whereas the APB bus is used for less demanding peripherals, such as watchdogs. Unlike the AHB bus, transfers on the APB bus are not pipelined.
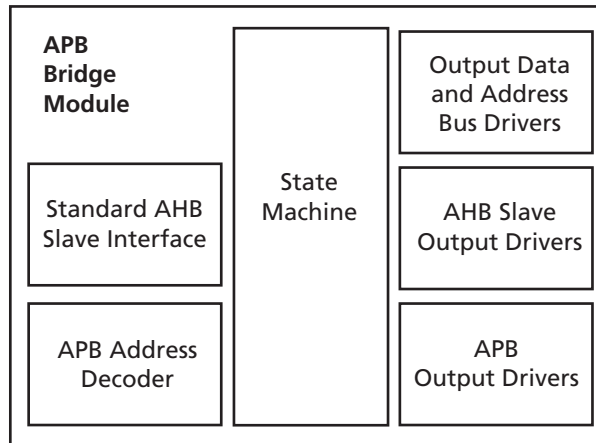
Figure 1 shows the CoreAHB2APB block diagram.

Figure 1 • **CoreAHB2APB**

Connecting CoreAHB2APB in CoreConsole

Table 1 lists the ports present on the AMBA Bridge and describes how to connect these in CoreConsole.

Table 1 • **AMBA Bridge Connections**

Connection	CoreConsole Label	Description
Required Connections		
AHB slave interface	AHBslave	Connect this to any of the 16 available slave slots on the AHB bus (CoreAHB).
APB master interface	APBmaster	Connect this to the APBmaster interface on the APB bus (CoreAPB).
HCLK	HCLK	AHB system clock input. Connect this to the HCLK output of CoreMP7Bridge.
HRESETn	HRESEETn	Active-low AHB system reset. Connect this to the HCLK output of CoreMP7Bridge.

Resource Requirements

The utilization for CoreAHB2APB in a ProASIC3 device is 250 tiles.

Ordering Information

CoreAHB2APB is included in the SysBASIC core bundle supplied with the Actel CoreConsole IP Deployment Platform (IDP). The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreAHB2APB cannot be ordered separately from the SysBASIC core bundle.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.1)	Page
v2.0	The "Supported Device Families" section was updated to include ProASIC3L.	1
	The "Resource Requirements" section was updated to change ProASIC3E to ProASIC3.	2
Advanced v0.1	The "Benefits" section was updated to include Cortex-M1.	1
	The "Supported Device Families" section was updated to include IGLOO and IGLOOe devices.	1

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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51700074-2/1.08