

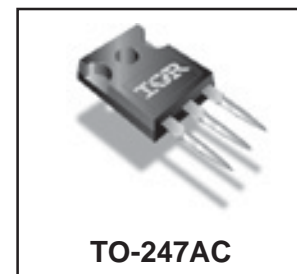
**Applications**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

$V_{DSS}$	$R_{DS(on)}$ typ.	$I_D$
<b>500V</b>	<b>0.135Ω</b>	<b>32A</b>

**Benefits**

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low  $R_{DS(on)}$



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	32	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	20	
$I_{DM}$	Pulsed Drain Current ①	130	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	460	W
	Linear Derating Factor	3.7	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case )	300	
	Mounting torque, 6-32 or M3 screw		

**Avalanche Characteristics**

Symbol	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	450	mJ
$I_{AR}$	Avalanche Current①	—	32	A
$E_{AR}$	Repetitive Avalanche Energy①	—	46	mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case④	—	0.26	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient④	—	40	

# IRFP32N50K

International  
IR Rectifier

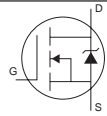
## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.54	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ④
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.135	0.16	$\Omega$	$V_{GS} = 10V, I_D = 32A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	50	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250	$\mu A$	$V_{DS} = 400V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

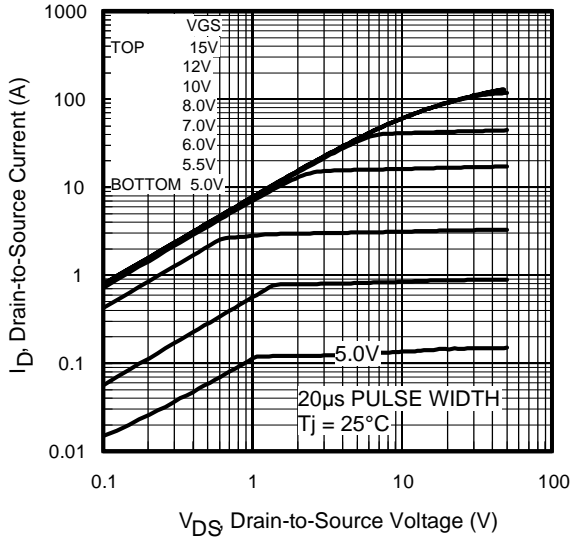
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	14	—	—	S	$V_{DS} = 50V, I_D = 32A$
$Q_g$	Total Gate Charge	—	—	190	nC	$I_D = 32A$
$Q_{gs}$	Gate-to-Source Charge	—	—	59	nC	$V_{DS} = 400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	84	nC	$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	$V_{DD} = 250V$
$t_r$	Rise Time	—	120	—		$I_D = 32A$
$t_{d(off)}$	Turn-Off Delay Time	—	48	—		$R_G = 4.3\Omega$
$t_f$	Fall Time	—	54	—		$V_{GS} = 10V$ ④
$C_{iss}$	Input Capacitance	—	5280	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	550	—		$V_{DS} = 25V$
$C_{rSS}$	Reverse Transfer Capacitance	—	45	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	5630	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	155	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	265	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑥

## Diode Characteristics

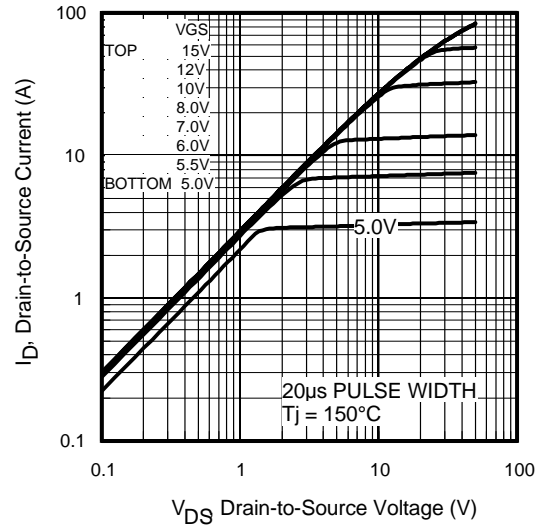
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	32	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	130		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 32A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	530	800	ns	$T_J = 25^\circ\text{C}, I_F = 32A$
$Q_{rr}$	Reverse Recovery Charge	—	9.0	13.5	$\mu C$	$di/dt = 100A/\mu s$ ④
$I_{RRM}$	Reverse Recovery Current	—	30	—	A	
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

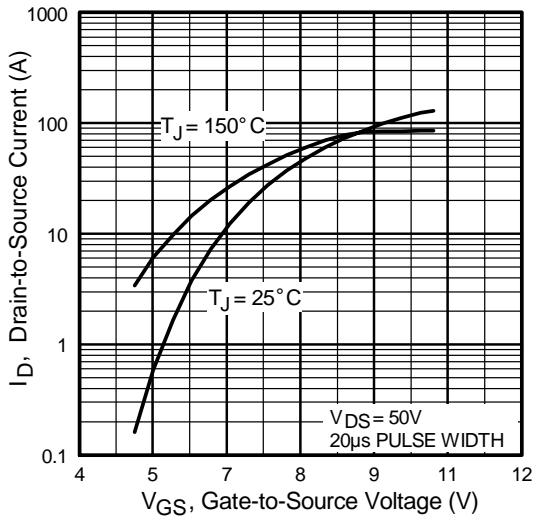
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.87\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 32A$ ,
- ③  $I_{SD} \leq 32A$ ,  $di/dt \leq 296A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$



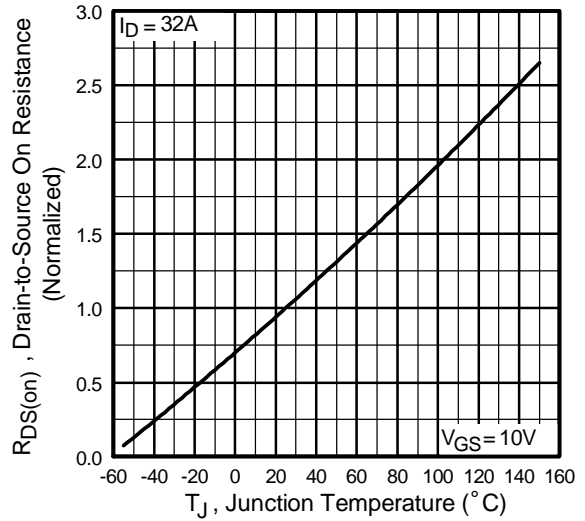
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

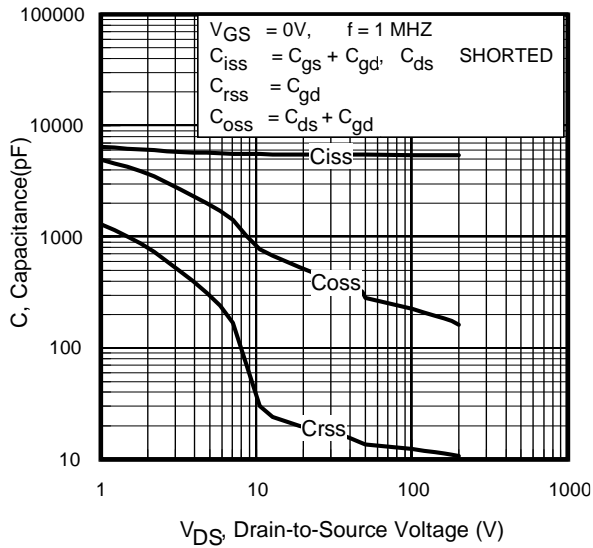


**Fig 3.** Typical Transfer Characteristics

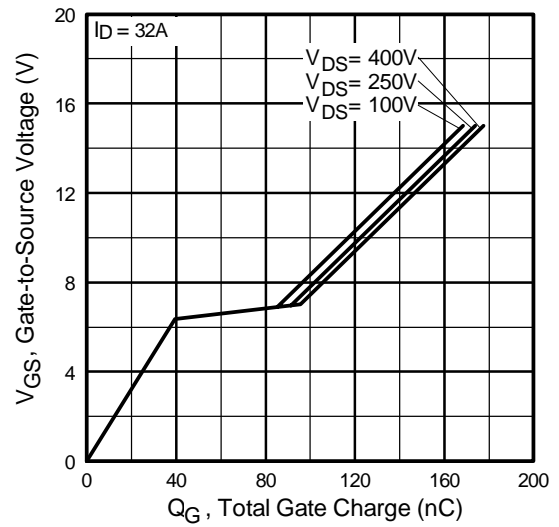


**Fig 4.** Normalized On-Resistance Vs. Temperature

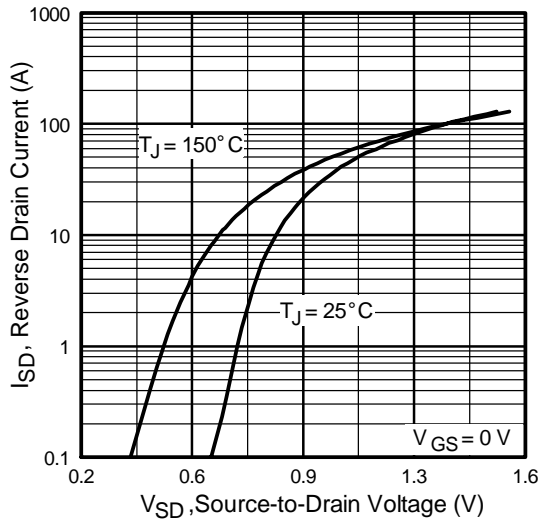
# IRFP32N50K



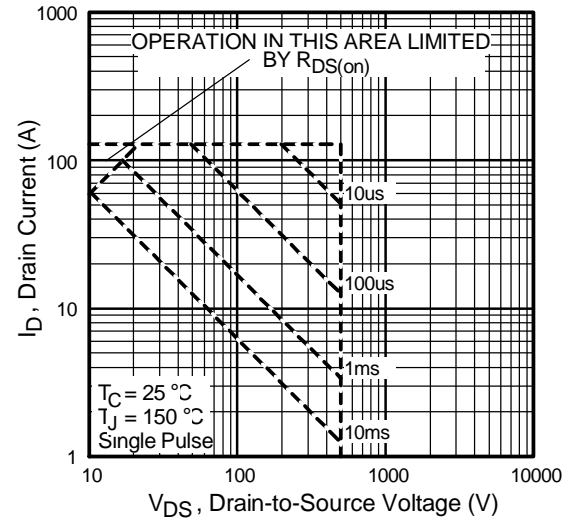
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



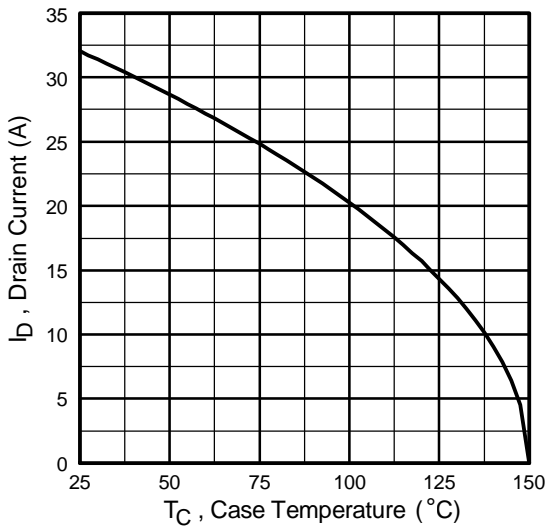
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



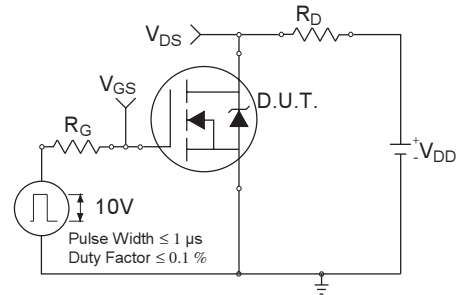
**Fig 7.** Typical Source-Drain Diode Forward Voltage



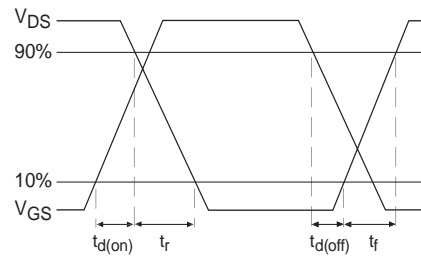
**Fig 8.** Maximum Safe Operating Area



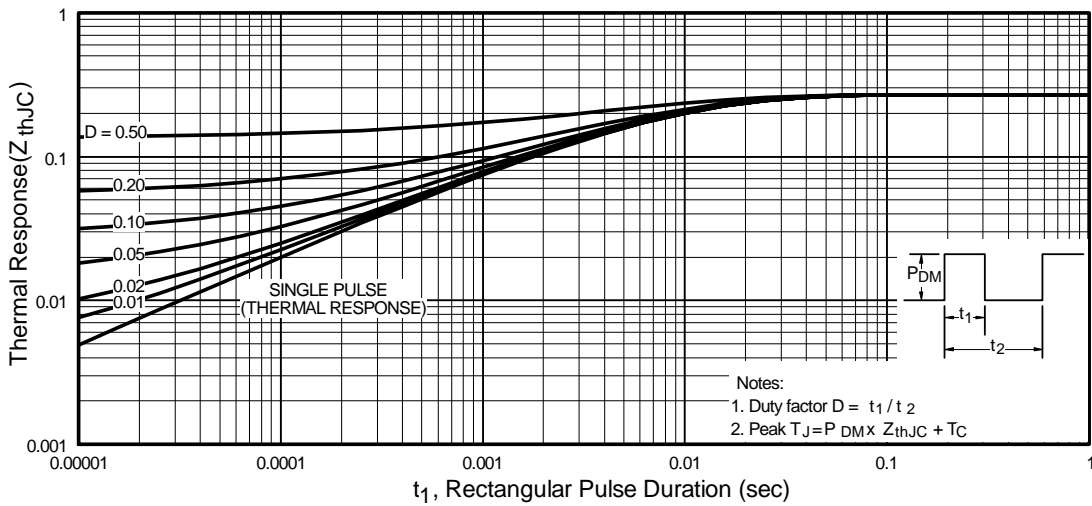
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

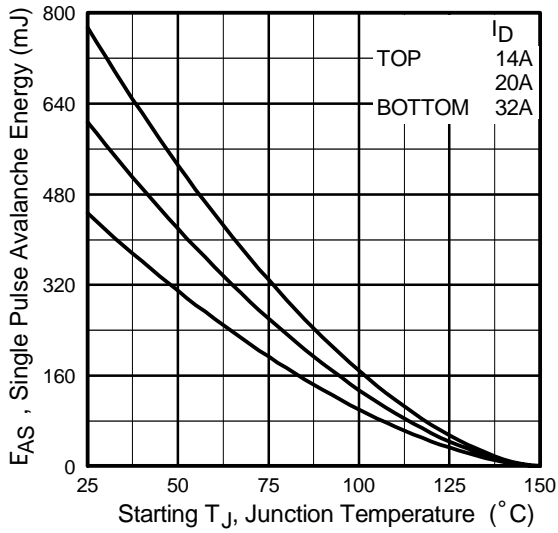


**Fig 10b.** Switching Time Waveforms

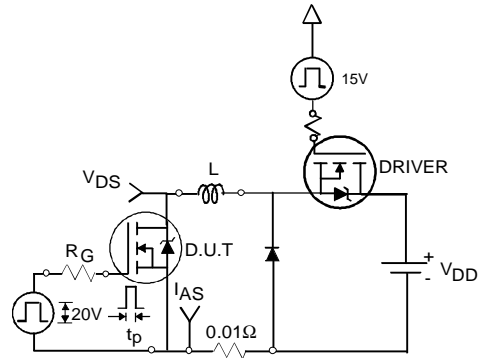


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

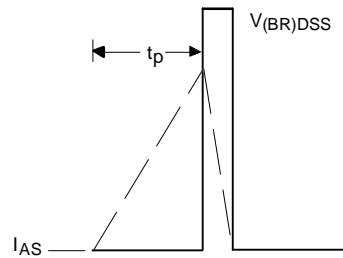
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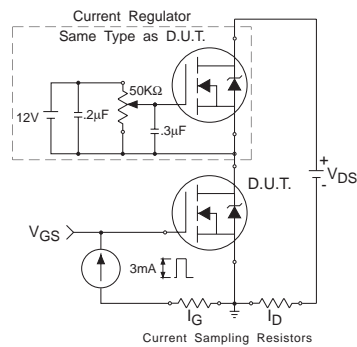
**Fig 12a.** Maximum Avalanche Energy Vs. Drain Current



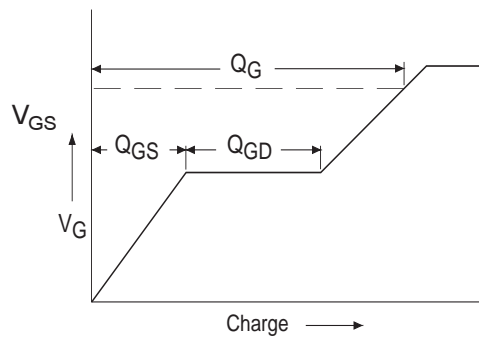
**Fig 12c.** Unclamped Inductive Test Circuit



**Fig 12d.** Unclamped Inductive Waveforms

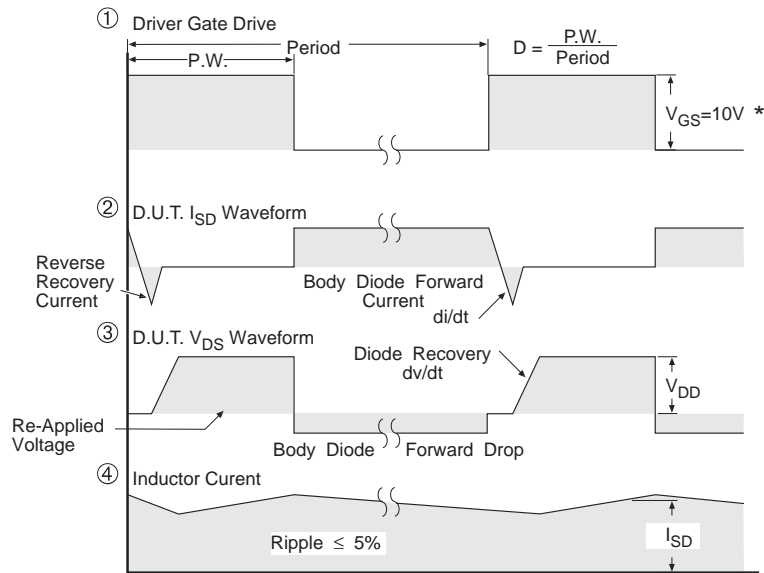
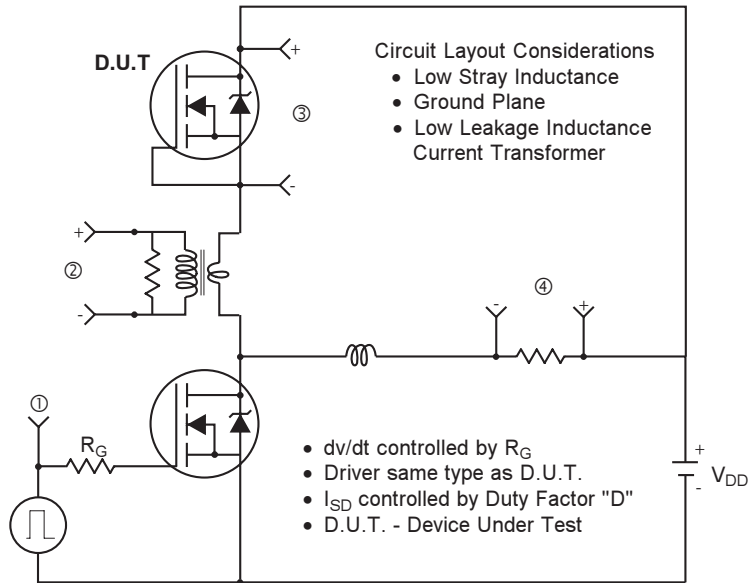


**Fig 13a.** Gate Charge Test Circuit



**Fig 13b.** Basic Gate Charge Waveform

## Peak Diode Recovery dv/dt Test Circuit



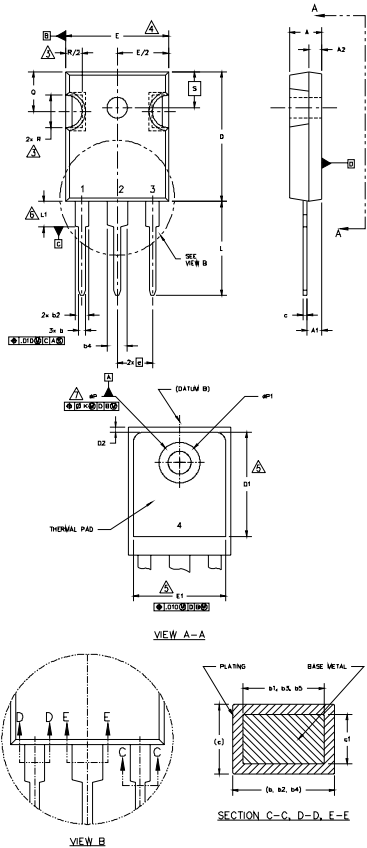
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRFP32N50K

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- CONTOUR OF SLOT OPTIONAL.
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
- LEAD FINISH UNCONTROLLED IN L1.
- ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91]
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION C.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.		
A	.183	.209	4.65	5.31		
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		
b1	.039	.053	0.99	1.35		
b2	.065	.094	1.65	2.39		
b3	.065	.092	1.65	2.37		
b4	.102	.135	2.59	3.43		
b5	.102	.133	2.59	3.38		
c	.015	.034	0.38	0.86		
c1	.015	.030	0.38	0.76		
D	.776	.815	19.71	20.70	4	
D1	.515	-	13.08	-	5	
D2	.020	.030	0.51	0.76		
E	.602	.625	15.29	15.87	4	
E1	.540	-	15.72	-		
e	.215 BSC		5.46 BSC			
Øk	.010		2.54			
L	.559	.634	14.20	16.10		
L1	.146	.169	3.71	4.29		
N	3		7.62 BSC			
ØP1	.140	.144	3.56	3.66		
Q	-	.275	-	6.98		
Q1	.209	.224	5.31	5.69		
R	.178	.216	4.52	5.49		
S	.217 BSC		5.51 BSC			

LEAD ASSIGNMENTS

HEXFEEET

1.- GATE  
2.- DRAIN  
3.- SOURCE  
4.- DRAIN

IGBTs, CoPACK

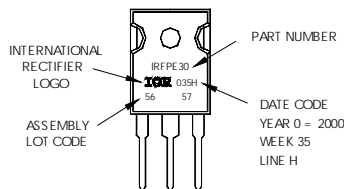
1.- GATE  
2.- COLLECTOR  
3.- EMITTER  
4.- COLLECTOR

DIODES

1.- ANODE/OPEN  
2.- CATHODE  
3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 5657 ASSEMBLED ON WW35, 2000 IN THE ASSEMBLY LINE "H"  
Note: "P" in assembly line position indicates "Lead-Free"



This product has been designed and qualified for the industrial market. Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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