

### 3.3V CMOS Buffer Clock Driver

#### Features

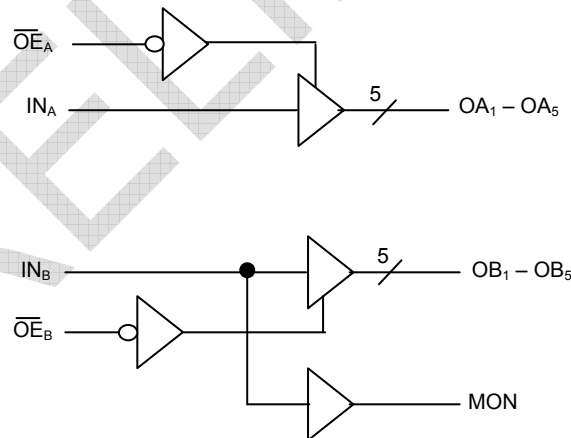
- Advanced CMOS Technology
- Guaranteed low skew < 500pS (max.)
- Very low duty cycle distortion < 1.0nS (max)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- $V_{CC} = 3.3V \pm 0.3V$
- Available in SSOP, SOIC and QSOP Packages

#### Functional Description

The PCS2P3805A is a 3.3V, non-inverting clock driver built using advanced CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The PCS2P3805A offers low capacitance inputs.

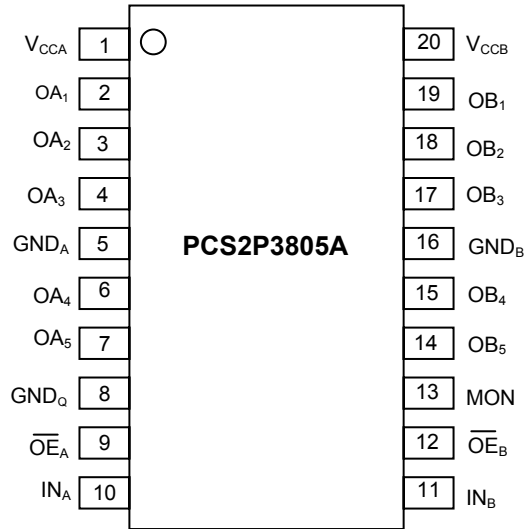
The PCS2P3805A is designed for high speed clock distribution where signal quality and skew are critical. The PCS2P3805A also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

#### Block Diagram



rev 0.3

Pin Diagram



Pin Description

Pin #	Pin Names	Description
9,12	OE <sub>A</sub> , OE <sub>B</sub>	3-State Output Enable Inputs (Active LOW)
10,11	IN <sub>A</sub> , IN <sub>B</sub>	Clock Inputs
2,3,4,6,7	OA <sub>1</sub> -OA <sub>5</sub>	Clock Outputs
19,18,17,15,14	OB <sub>1</sub> -OB <sub>5</sub>	Clock Outputs
1	V <sub>CCA</sub>	Power supply for Bank A
20	V <sub>CCB</sub>	Power supply for Bank B
5	GND <sub>A</sub>	Ground for Bank A
16	GND <sub>B</sub>	Ground for Bank B
8	GND <sub>Q</sub>	Ground
13	MON	Monitor Output

rev 0.3

Function Table

Inputs		Outputs	
$\overline{OE}_A, \overline{OE}_B$	$IN_A, IN_B$	$OA_n, OB_n$	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

Note: H = HIGH; L = LOW; Z = High-Impedance

Capacitance ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

Symbol	Parameter <sup>1</sup>	Conditions	Typ	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

Note: 1 This parameter is measured at characterization but not tested.

Absolute Maximum Ratings<sup>1</sup>

Symbol	Description	Max	Unit
$V_{TERM}^2$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^3$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^4$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
$I_{OUT}$	DC Output Current	-60 to +60	mA
$T_{STG}$	Storage Temperature	-65 to +150	$^\circ\text{C}$
$T_J$	Junction Temperature	150	$^\circ\text{C}$
$T_s$	Max. Soldering Temperature (10 sec)	260	$^\circ\text{C}$
$T_{DV}$	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: 1 These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

- 2.  $V_{CC}$  terminals.
- 3. Input terminals.
- 4. Outputs and I/O terminals.

rev 0.3

**DC Electrical Characteristics over Operating Range**

Following Conditions Apply Unless Otherwise Specified

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ; Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions <sup>1</sup>		Min	Typ <sup>2</sup>	Max	Unit
$V_{IH}$	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2		5.5	V
	Input HIGH Level (I/O pins)			2		$V_{CC} + 0.5$	
$V_{IL}$	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5		0.8	V
$I_{IH}$	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$			$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$			$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$			$\pm 1$	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$			$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output Pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = \text{GND}$			$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$			-0.7	-1.2	V
$I_{ODH}$	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^3$		-36	-60	-110	mA
$I_{ODL}$	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^3$		50	90	200	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$			V
			$I_{OH} = -8\text{mA}$	$2.4^5$	3		
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 0.1\text{mA}$			0.2	V
			$I_{OL} = 16\text{mA}$		0.2	0.4	
			$I_{OL} = 24\text{mA}$		0.3	0.5	
$I_{OFF}$	Input Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} = 4.5\text{V}$				$\pm 1$	$\mu\text{A}$
$I_{OS}$	Short Circuit Current <sup>4</sup>	$V_{CC} = \text{Max.}, V_O = \text{GND}^3$		-60	-135	-240	mA
$V_H$	Input Hysteresis				150		mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$			0.1	10	$\mu\text{A}$

Notes: 1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at  $V_{CC} = 3.3\text{V}, +25^\circ\text{C}$  ambient.

3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

4. This parameter is guaranteed but not tested.

5.  $V_{OH} = V_{CC} - 0.6\text{V}$  at rated current.

rev 0.3

Power Supply Characteristics

Symbol	Parameter	Test Conditions <sup>1</sup>		Min	Typ <sup>2</sup>	Max	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max. } V_{IN} = V_{CC} - 0.6V^3$			10	30	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current <sup>4</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Per Output Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$		0.035	0.06	mA/ MHz
$I_C$	Total Power Supply Current <sup>6</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_O = 25\text{MHz}$ 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = V_{CC}$ Mon. Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$		0.9	1.6	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$		0.9	1.6	
		$V_{CC} = \text{Max.}$ Outputs Open $f_O = 50\text{MHz}$ 50% Duty Cycle $OE_A = OE_B = \text{GND}$ Eleven Outputs Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$		45	$62^5$	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$		45	$62^5$	

Notes:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 3.3V$ ,  $+25^\circ C$  ambient.
- Per TTL driven input ( $V_{IN} = V_{CC} - 0.6V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_C$  formula.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$   
 $I_{CC} = \text{Quiescent Current } (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = V_{CC} - 0.6V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_O = \text{Output Frequency}$   
 $N_O = \text{Number of Outputs at } f_O$   
 All currents are in milliamps and all frequencies are in megahertz.

rev 0.3

Switching Characteristics Over Operating Range – Commercial<sup>3,4</sup>

Symbol	Parameter	Conditions <sup>1</sup>	PCS2P3805A		Unit	
			Min <sup>2</sup>	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay IN <sub>A</sub> to OA <sub>n</sub> , IN <sub>B</sub> to OB <sub>n</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	5	nS	
t <sub>R</sub>	Output Rise Time (0.8V to 2.0V)			2	nS	
t <sub>F</sub>	Output Fall Time (2.0V to 0.8V)			2	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of all banks of same package (inputs tied together)			0.5	nS	
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> – t <sub>PLH</sub>  )			1	nS	
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade			1.2	nS	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time OE <sub>A</sub> to OA <sub>n</sub> , OE <sub>B</sub> to OB <sub>n</sub>			1.5	6	nS
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time OE <sub>A</sub> to OA <sub>n</sub> , OE <sub>B</sub> to OB <sub>n</sub>			1.5	5	nS

Switching Characteristics Over Operating Range – Industrial<sup>3,4</sup>

Symbol	Parameter	Conditions <sup>1</sup>	PCS2P3805A		Unit	
			Min <sup>2</sup>	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay IN <sub>A</sub> to OA <sub>n</sub> , IN <sub>B</sub> to OB <sub>n</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	5.2	nS	
t <sub>R</sub>	Output Rise Time (0.8V to 2.0V)			2	nS	
t <sub>F</sub>	Output Fall Time (2.0V to 0.8V)			2	nS	
t <sub>SK(O)</sub>	Output skew: skew between outputs of all banks of same package (inputs tied together)			0.6	nS	
t <sub>SK(P)</sub>	Pulse skew: skew between opposite transitions of same output ( t <sub>PHL</sub> – t <sub>PLH</sub>  )			1	nS	
t <sub>SK(T)</sub>	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade			1.2	nS	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time OE <sub>A</sub> to OA <sub>n</sub> , OE <sub>B</sub> to OB <sub>n</sub>			1.5	6	nS
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time OE <sub>A</sub> to OA <sub>n</sub> , OE <sub>B</sub> to OB <sub>n</sub>			1.5	5	nS

Note: 1. See test circuits and waveforms.

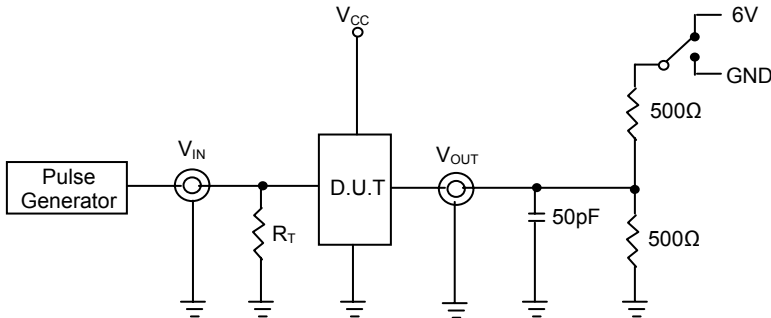
2. Minimum limits are guaranteed but not tested on Propagation Delays.

3. t<sub>PLH</sub>, t<sub>PHL</sub>, t<sub>SK(O)</sub> are production tested. All other parameters guaranteed but not production tested.

4. Propagation delay range indicated by Min. and Max. limit is due to V<sub>CC</sub>, operating temperature and process parameters. These propagation delay limits do not imply skew.

rev 0.3

### Test Circuits and Waveforms



### Switch Position

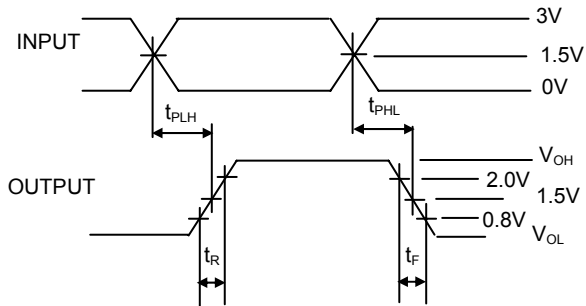
Test	Switch
Disable Low Enable Low	6V
Disable High Enable High	GND

Definitions:

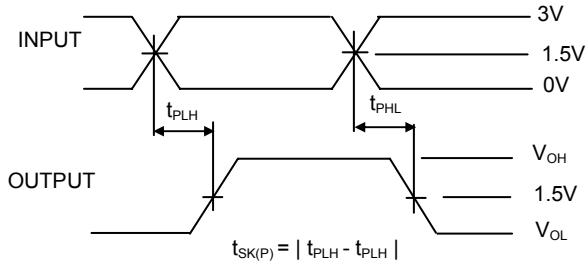
$C_L$  = Load capacitance: includes jig and probe capacitance.

$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

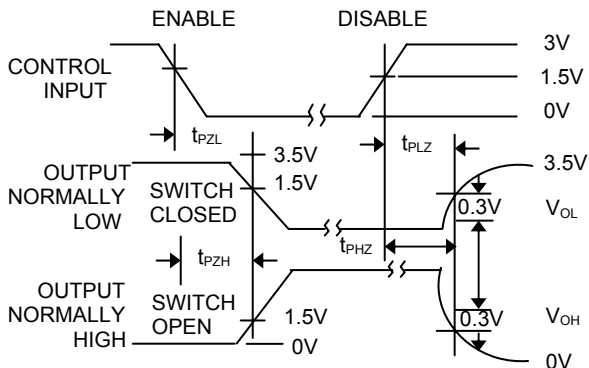
### Test Circuits for All Outputs



### Package Delay



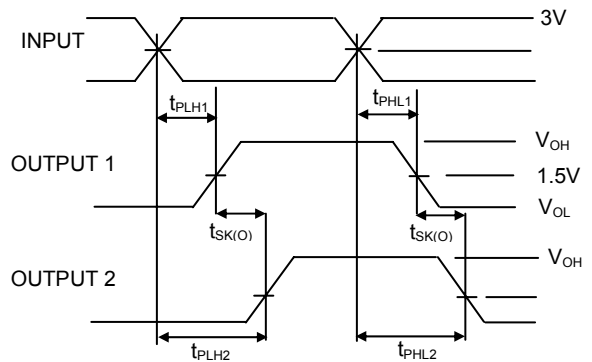
### Pulse Skew



### Enable and Disable Times

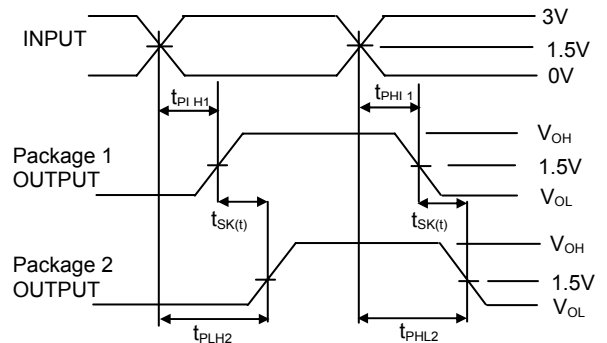
**Note:**

Diagram shown for input Control Enable-LOW and input Control Disable-HIGH



$$t_{SK(O)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

### Output Skew – $t_{SK(O)}$



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

### Package Skew – $t_{SK(t)}$

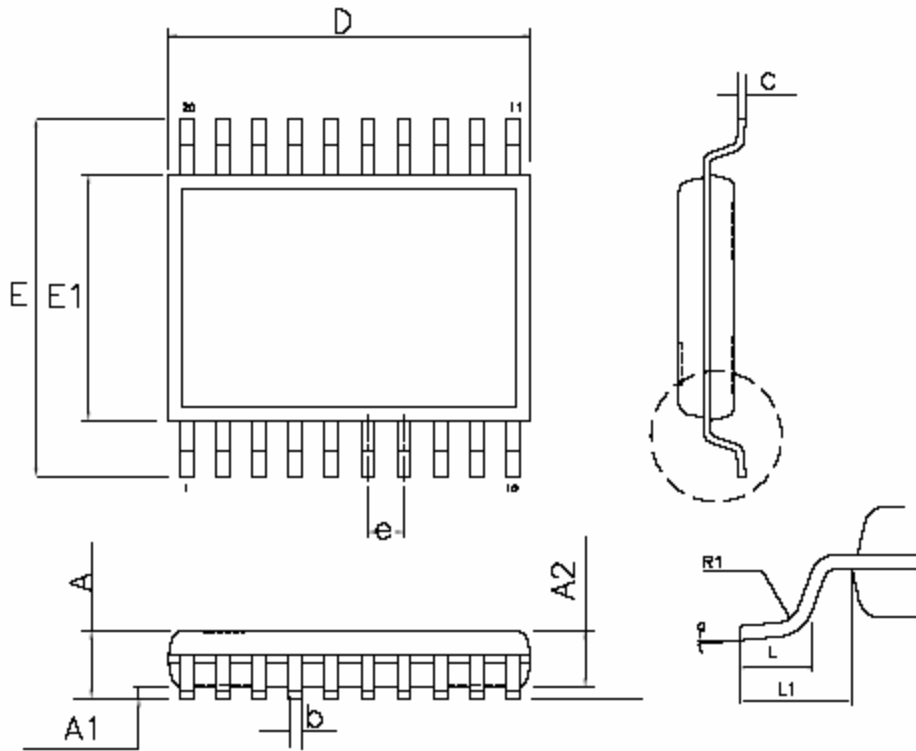
**Note:**

Pulse Generator for all Pulses:  $f \leq 10\text{MHz}$ ;  $t_r \leq 2.5\text{nS}$ ;  $t_f \leq 2.5\text{nS}$

rev 0.3

Package Information

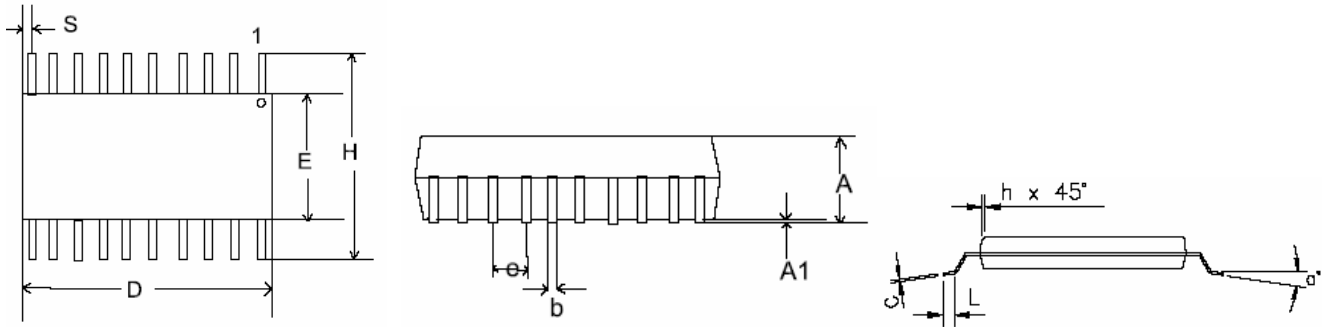
20-lead SSOP ( 209 mil )



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.079	...	2.0
A1	0.002	...	0.05	.....
A2	0.065	0.073	1.65	1.85
D	0.275	0.291	7.00	7.40
c	0.004	0.010	0.09	0.25
E	0.295	0.319	7.50	8.10
E1	0.197	0.220	5.00	5.60
L	0.021	0.037	0.55	0.95
L1	0.050 REF		1.25 REF	
b	0.009	0.015	0.22	0.38
R1	0.004	....	0.09	....
a	0°	8°	0°	8°
e	0.0197 BASE		0.65 BASE	

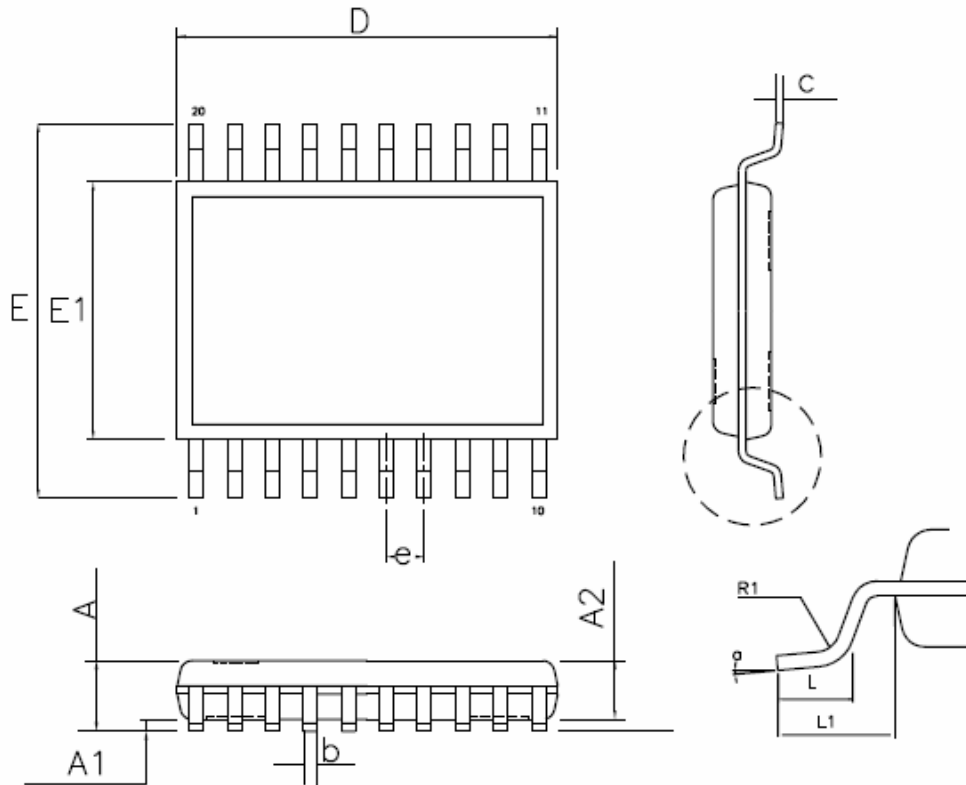


20-lead QSOP



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.060	0.068	1.52	1.73
A1	0.004	0.008	0.10	0.20
b	0.009	0.012	0.23	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	0.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
S	0.056	0.060	1.42	1.52
a	0°	8°	0°	8°

20L SOIC Package (300 mil)



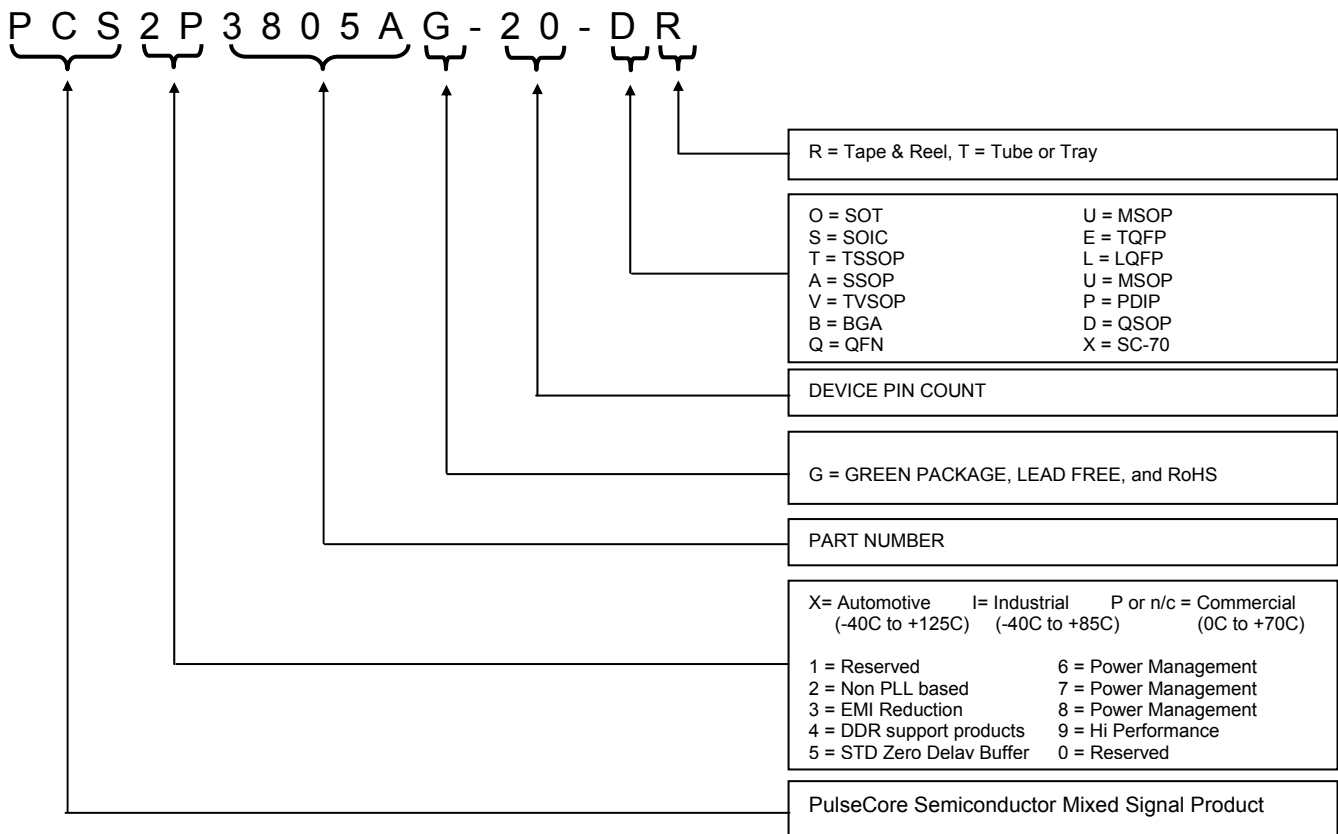
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.088	0.094	2.25	2.40
D	0.496	0.512	12.60	13.00
L	0.016	0.050	0.40	1.27
E1	0.291	0.299	7.40	7.60
R1	0.003	....	0.08	.....
b	0.013	0.022	0.33	0.56
c	0.009	0.015	0.23	0.38
E	0.394	0.419	10.00	10.65
e	0.050 BSC		1.27 BSC	
a	0°	8°	0°	8°

rev 0.3

Ordering Information

Part Number	Marking	Package Type	Temperature
PCS2P3805AG-20-AR	2P3805AG	20-Pin SSOP, TAPE & REEL, Green	Commercial
PCS2P3805AG-20-AT	2P3805AG	20-Pin SSOP, TUBE, Green	Commercial
PCS2P3805AG-20-DR	2P3805AG	20-Pin QSOP, TAPE & REEL, Green	Commercial
PCS2P3805AG-20-DT	2P3805AG	20-Pin QSOP, TUBE, Green	Commercial
PCS2P3805AG-20-SR	2P3805AG	20-Pin SOIC, TAPE & REEL, Green	Commercial
PCS2P3805AG-20-ST	2P3805AG	20-Pin SOIC, TUBE, Green	Commercial
PCS2I3805AG-20-AR	2I3805AG	20-Pin SSOP, TAPE & REEL, Green	Industrial
PCS2I3805AG-20-AT	2I3805AG	20-Pin SSOP, TUBE, Green	Industrial
PCS2I3805AG-20-DR	2I3805AG	20-Pin QSOP, TAPE & REEL, Green	Industrial
PCS2I3805AG-20-DT	2I3805AG	20-Pin QSOP, TUBE, Green	Industrial
PCS2I3805AG-20-SR	2I3805AG	20-Pin SOIC, TAPE & REEL, Green	Industrial
PCS2I3805AG-20-ST	2I3805AG	20-Pin SOIC, TUBE, Green	Industrial

Device Ordering Information



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



Giving you the edge

September 2006

PCS2P3805A

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Preliminary Information  
Part Number: PCS2P3805A  
Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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