

# SANYO Semiconductors **DATA SHEET**

# LC87F5ND0C

# CMOS IC FROM 128K byte, RAM 6144 byte on-chip 8-bit 1-chip Microcontroller

#### Overview

The SANYO LC87F5ND0C is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrate on a single chip a number of hardware features such as 128K-byte flash ROM (onboard rewritable), 6144-byte RAM, Onchip debugging function, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, two synchronous SIO ports (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), four 12-bit PWM channels, an 8-bit 15-channel AD converter, a system clock frequency divider, and a 29-source 10-vector interrupt feature.

#### **Features**

- ■Flash ROM
  - Capable of on-board-programing with wide range, 2.7 to 5.5V, of voltage source
  - Block-erase in 128 byte units
  - $131072 \times 8$  bits

#### $\blacksquare$ RAM

•  $6144 \times 9$  bits

■Minimum Bus Cycle Time

83.3ns (12MHz)
 125ns (8MHz)
 500ns (2MHz)
 VDD=2.8 to 5.5V
 VDD=2.5 to 5.5V
 VDD=2.2 to 5.5V

Note: Bus cycle time indicates the speed to read ROM.

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■Minimum Instruction Cycle Time (tCYC)

250ns (12MHz)
 375ns (8MHz)
 1.5μs (2MHz)
 VDD=2.8 to 5.5V
 VDD=2.5 to 5.5V
 VDD=2.2 to 5.5V

#### **■**Ports

• Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1-bit units 64 (P1n, P2n, P3n, P70 to P73, P8n, PAn, PBn, PCn,

S2Pn, PWM0, PWM1, XT2)

16 (PEn, PFn)

8 (P0n)

1 (XT1)

Ports whose I/O direction can be designated in 2-bit units

Ports whose I/O direction can be designated in 4-bit units

Normal withstand voltage input port

Dedicated oscillator ports
 Reset pins
 2 (<u>CF1</u>, CF2)
 1 (RES)

• Power pins 8 (VSS1 to VSS4, VDD1 to VDD4)

#### ■Timers

• Timer 0: 16-bit timer/counter with capture register

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) ×2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers)

+ 8-bit counter (with two 8-bit capture registers)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)

Mode 3: 16-bit counter (with two 16-bit capture registers)

• Timer 1: 16-bit timer/counter that supports PWM/toggle output

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter(with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also from the lower-order 8-bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  - 2) Interrupts programmable in 5 different time schemes.

## ■High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 24MHz (at a main clock of 12MHz).
- 2) Can generate output real-time.

#### **■**SIO

- SIO0: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)

Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

- SIO2: 8 bit synchronous serial interface
  - 1) LSB first mode
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 32 bytes)

#### ■UART: 2 channels

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bits in continuous transmission mode)
- Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

■AD Converter: 8 bits × 15 channels

■PWM: Multifrequency 12-bit PWM × 4 channels

- ■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
  - 1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
  - 2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

## ■Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

#### ■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

#### **■**Interrupts

- 29 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/UART2 receive
8	0003BH	H or L	SIO/UART1 transmit/UART2 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0/T4/T5/PWM0, PWM1

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- ■Subroutine Stack Levels: 3072 levels maximum (the stack is allocated in RAM)

## ■High-speed Multiplication/Division Instructions

• 16-bits  $\times$  8-bits (5 tCYC execution time)

• 24-bits × 16-bits (12 tCYC execution time)

• 16-bits ÷ 8-bits (8 tCYC execution time)

• 24-bits ÷ 16-bits (12 tCYC execution time)

#### **■**Oscillation Circuits

• RC oscillation circuit (internal) : For system clock

CF oscillation circuit
 Crystal oscillation circuit
 For system clock, with internal Rf
 For low-speed system clock

• Multifrequency RC oscillation circuit (internal) : For system clock

#### ■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0μs, 2.0μs, 4.0μs, 8.0μs, 16.0μs, 32.0μs, and 64.0μs (at a main clock rate of 12MHz).

#### ■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) Canceled by a system reset or occurrence of interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The CF, RC, and crystal oscillators automatically stop operation.
  - 2) There are three ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the low level.
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The CF and RC oscillators automatically stop operation.
  - 2) The state of crystal oscillation established when the HOLD mode is entered is retained.
  - 3) There are four ways of resetting the X'tal HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established in the base timer circuit

#### ■On-chip Debugger Function

• Permits software debugging with the test device installed on the target board.

#### ■Package Form

• QIP100E (14 × 20) : "Lead-free type"

#### ■Development Tools

• Evaluation (EVA) chip : LC87EV690

• Emulator : EVA62S + ECB876600D + SUB875C00 + POD100QFP

ICE-B877300 + SUB875C00 + POD100QFP

• On-chip-debugger : TCB87-TypeB + LC87F5ND0C

## **■**Programming Boards

Trogramming Dourds	,
Package	Programming boards
QIP100E (14 × 20)	W87F52256Q

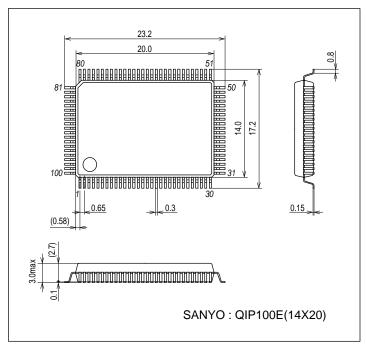
#### ■Flash ROM Programmer

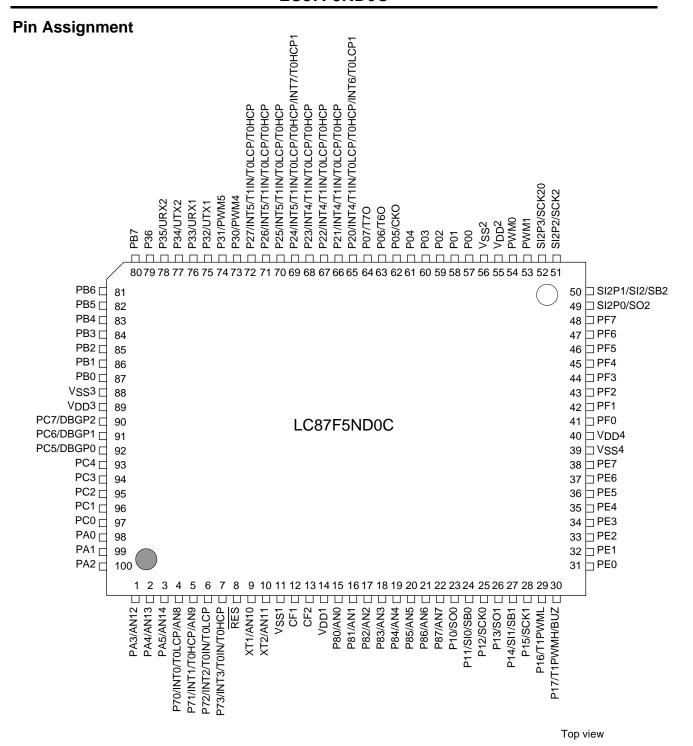
Maker	Model	Support version(Note)	Device	
Flash Support Group, Inc. (Single)	AF9708/09/09B (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.82	LC87F5NC8A	
Flash Support Group, Inc.	AF9723(Main body) (including product of Ando Electric Co.,Ltd)	Revision : After Rev.02.29	1.007551004	
(Gang)	AF9833(Unit) (including product of Ando Electric Co.,Ltd)	Revision : After Rev.01.88	LC87F5NC8A	
SANYO	SKK/SKK Type-B/SKK DBG Type-B (SANYO FWS)	Application Version: After 1.04 Chip Data Version: After2.10	LC87F5NC8A	

# **Package Dimensions**

unit: mm (typ)

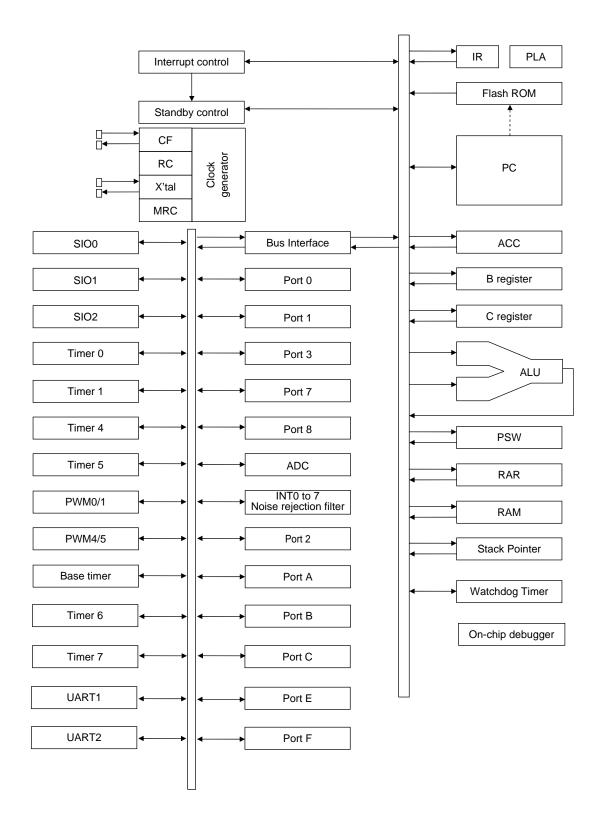
3151A





SANYO: QIP100E(14×20) "Lead-free Type"

# **System Block Diagram**



# **Pin Description**

Pin Name	I/O			Desc	cription			Option				
V <sub>SS</sub> 1, V <sub>SS</sub> 2	_	- Power supply pi	n		<u> </u>			No				
V <sub>SS</sub> 3, V <sub>SS</sub> 4												
V <sub>DD</sub> 1, V <sub>DD</sub> 2	-	+ Power supply p	in					No				
V <sub>DD</sub> 3, V <sub>DD</sub> 4		,										
Port 0	I/O	• 8-bit I/O port						Yes				
P00 to P07		I/O specifiable in	n 4-bit units									
		Pull-up resistor	can be turned or	and off in 4-bit	units							
		HOLD release in	nput									
		Port 0 interrupt i	nput									
		Pin functions	functions									
		P05: System clo	ock output (syste	m clock/subcloc	ck selectable)							
		P06: Timer 6 to	ggle output									
		P07: Timer 7 tog	ggle output									
Port 1	I/O	8-bit I/O port						Yes				
P10 to P17		I/O specifiable in	n 1-bit units									
		Pull-up resistor	can be turned or	and off in 1-bit	units							
		Pin functions										
		P10: SIO0 data	=									
		P11: SIO0 data	· ·									
		P12: SIO0 clock										
		P13: SIO1 data										
		P14: SIO1 data	· ·									
		P15: SIO1 clock P16: Timer 1 PV										
		P17: Timer 1 PV	•	ener outnut								
Port 2	I/O	• 8-bit I/O port	vivii i output, bei	eper output				Yes				
	1/0	I/O specifiable in	n 1-hit units					163				
P20 to P27		Pull-up resistor (		and off in 1-bit	units							
		Other functions										
		P20: INT4 input	/HOLD reset inp	ut/timer 1 event	input/timer 0L c	apture input/						
		-	apture input/INT		-							
		P21 to P23: INT	•	=		er 0L capture in	put/					
		timer 0H c	apture input									
		P24: INT5 input	/HOLD reset inp	ut/timer 1 event	input/timer 0L c	apture input/						
		timer 0H c	apture input/INT	7 input/timer 0H	capture 1 input							
		P25 to P27: INT	5 input/HOLD re	eset input/timer	1 event input/tim	er 0L capture in	put/					
		timer 0H c	apture input									
		Interrupt acknow	vledge type	Т	1	1						
			Rising	Falling	Rising/	H level	L level					
			_		Falling							
		INT4	enable	enable	enable	disable	disable					
		INT5	enable	enable	enable	disable	disable					
		INT6	enable	enable	enable	disable disable	disable					
		INT7	enable	enable	enable	disable	disable					
D-+0	1/0	7 54 1/2						V				
Port 3	I/O	<ul><li>7-bit I/O port</li><li>I/O specifiable ir</li></ul>	a 1-hit unite					Yes				
P30 to P36		Pull-up resistor		and off in 1 hit	unite							
		Pin functions	can be turried or	rand on in 1-bit	units							
		P30: PWM4 out	put									
		P31: PWM5 out	•									
		P32: UART1 tra	•									
			33: UART1 receive									
		P34: UART2 tra										
		P35: UART2 red	ceive									

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Pin Name	I/O		Description	on			Option
Port 7	I/O	• 4-bit I/O port					No
P70 to P73		I/O specifiable in 1-bit units					
		<ul> <li>Pull-up resistor can be turned on and of</li> </ul>	off in 1-bit units				
		Other functions					
		P70: INT0 input/HOLD release input/Ti	mer 0L capture	e input/Ou	tput for watchdo	g timer	
		P71: INT1 input/HOLD release input/Ti	mer 0H captur	e input			
		P72: INT2 input/HOLD release input/Ti	mer 0 event in	put/Timer	0L capture input		
		P73: INT3 input with noise filter/Timer	0 event input/T	imer 0H c	apture input		
		Interrupt acknowledge type					,
		Rising Fal	ling R	Rising/	H level	L level	
		ixisiiig i ai	'''' <sup>'</sup> F	alling	TTTEVE	L level	]
		INTO enable ena	able d	isable	enable	enable	
		INT1 enable ena	able d	isable	enable	enable	
		INT2 enable ena	able e	nable	disable	disable	
		INT3 enable ena	able e	nable	disable	disable	
		AD converter input port: AN8 (P70), All	N9 (P71)				·
Port 8	I/O	• 8-bit I/O port	. ,				No
	1/0	• I/O specifiable in 1-bit units					140
P80 to P87		Other functions					
		P80 to P87: AD converter input port					
Port A	I/O	6-bit I/O port					Yes
	1/0	I/O specifiable in 1-bit units					res
PA0 to PA5		<ul> <li>I/O specifiable in 1-bit units</li> <li>Pull-up resistor can be turned on and c</li> </ul>	off in 1-hit unita				
		<ul> <li>Pull-up resistor can be turned on and d</li> <li>Shared pins</li> </ul>	או ווו ו-טונ ערוונS				
		•	DAE(ANI4E)				
David D	1/0	AD converter input ports: PA3(AN12) to	5 PA5(AN15)				V
Port B	I/O	8-bit I/O port					Yes
PB0 to PB7		• I/O specifiable in 1-bit units	m: 4 1 2				
		Pull-up resistor can be turned on and control	off in 1-bit units				
Port C	I/O	• 8-bit I/O port					Yes
PC0 to PC7		I/O specifiable in 1-bit units					
		Pull-up resistor can be turned on and contains a second conta	off in 1-bit units				
		• Pin functions					
		DBGP0 to DBGP2 (PC5 to PC7): On-c	hip Debugger				
Port E	I/O	8-bit I/O port					No
PE0 to PE7		I/O specifiable in 2-bit units					
		<ul> <li>Pull-up resistor can be turned on and c</li> </ul>	ff in 1-bit units				
Port F	I/O	8-bit I/O port					No
PF0 to PF7		<ul> <li>I/O specifiable in 2-bit units</li> </ul>					
		<ul> <li>Pull-up resistor can be turned on and c</li> </ul>	ff in 1-bit units				
SIO2 Port	I/O	4-bit I/O port					No
SI2P0 to SI2P3		I/O specifiable in 1-bit units					
		Shared functions:					
		SI2P0: SIO2 data output					
		SI2P1: SIO2 data input, bus input/outp	ut				
		SI2P2: SIO2 clock input/output					
		SI2P3: SIO2 clock output					
PWM0, PWM1	I/O	PWM0, PWM1 output port		<del></del>	<u></u>		No
		General-purpose I/O available					
RES	I	Reset pin			·	·	No
XT1	1	<ul> <li>Input terminal for 32.768kHz X'tal oscil</li> </ul>	lation				No
	•	• Shared functions:					140
		AN10: AD converter input port					
		General-purpose input port					
		Must be connected to V <sub>DD</sub> 1 if not to be	م رادما				
VT2	1/0						NI_
XT2	I/O	Output terminal for 32.768kHz X'tal osc     Oh and fine stings:	illation				No
		Shared functions:     ANALAR and a state in the stat					
		AN11: AD converter input port					
		General-purpose I/O port		_			
		Must be set for oscillation and kept ope	en if not to be u	used.			
CF1	I	Ceramic resonator input pin					No
CF2	0	Ceramic resonator output pin					No

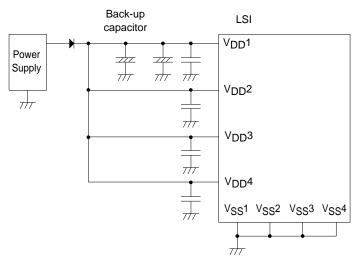
## **Port Output Types**

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port	Options Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P30 to P36	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P87	-	No	N-channel open drain	No
PA0 to PA5	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PB0 to PB7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PC0 to PC7	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PE0 to PE7	-	No	CMOS	Programmable
PF0 to PF7	-	No	CMOS	Programmable
SI2P0, SI2P2 SI2P3	-	No	CMOS	No
SI2P1	-	No	CMOS (when selected as ordinary port) N-channel open drain (When SIO2 data is selected)	No
PWM0, PWM1	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	Output for 32.768kHz quartz oscillator N-channel open drain (when in general-purpose No output mode)	No

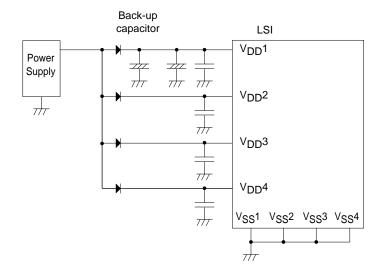
Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

(Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



<sup>\*1:</sup> Make the following connection to minimize the noise input to the  $V_{DD1}$  pin and prolong the backup time. Be sure to electrically short the  $V_{SS1}$ ,  $V_{SS2}$ ,  $V_{SS3}$  and  $V_{SS4}$  pins.

(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



# Absolute Maximum Ratings at $Ta=25^{\circ}C,\ V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

	Doromotor	Cumbal	Pins/Remarks	Conditions			Speci	fication	
	Parameter	Symbol	rins/Remarks	Conditions	۷ <sub>DD</sub> [۷]	min	typ	max	unit
	ximum Supply tage	V <sub>DD</sub> max	V <sub>DD</sub> 1, V <sub>DD</sub> 2, V <sub>DD</sub> 3, V <sub>DD</sub> 4	$V_{\mathrm{DD}}$ 1= $V_{\mathrm{DD}}$ 2= $V_{\mathrm{DD}}$ 3= $V_{\mathrm{DD}}$ 4		-0.3		+6.5	
Inp	ut voltage	V <sub>I</sub> (1)	XT1, CF1			-0.3		V <sub>DD</sub> +0.3	
Input/Output Voltage		V <sub>IO</sub> (1) Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1,XT2			-0.3		V <sub>DD</sub> +0.3	V	
	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin		-10			
		IOPH(2)	PWM0, PWM1	Per 1 application pin.		-20			
		IOPH(3)	P71 to P73	Per 1 application pin.		-5			
	Average output current (Note1-1)	IOM(1)	Ports 0, 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3	CMOS output select per 1 application pin		-7.5			
Į.		IOM(2)	PWM0, PWM1	Per 1 application pin.		-10			
ırren		IOM(3)	P71 to P73	Per 1 application pin.		-3			
ut cu	Total output	ΣΙΟΑΗ(1)	P71 to P73	Total of all applicable pins		-10			
High level output current	current	ΣΙΟΑΗ(2)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-25			mA
h le		ΣΙΟΑΗ(3)	Port 0	Total of all applicable pins		-25			
Hig		ΣΙΟΑΗ(4)	Port 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins		-45			
		ΣΙΟΑΗ(5)	Ports 2, 3, B	Total of all applicable pins		-25			
		ΣΙΟΑΗ(6)	Ports A, C	Total of all applicable pins	<u> </u>	-25		-	
		ΣΙΟΑΗ(7)	Ports 2, 3, A, B, C	Total of all applicable pins		-45			
		ΣΙΟΑΗ(8)	Port F	Total of all applicable pins		-25			
		ΣΙΟΑΗ(9)	Ports 1, E	Total of all applicable pins		-25			
		ΣΙΟΑΗ(10)	Ports 1, E, F	Total of all applicable pins		-45			

Note 1-1: Average output current is average of current in 100ms interval.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins/Remarks	Conditions			Specif	ication	
Faiametei	Symbol	Filis/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.				20	
	IOPL(2)	P00, P01	Per 1 application pin.				30	
	IOPL(3)	Ports 7, 8, XT2	Per 1 application pin.				10	
Average output current (Note1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3 Ports A, B, C, E, F SI2P0 to SI2P3 PWM0, PWM1	Per 1 application pin.				15	
ent	IOML(2)	P00, P01	Per 1 application pin.				20	
Total output current	IOML(3)	Ports 7, 8, XT2	Per 1 application pin.				7.5	
Total output	ΣIOAL(1)	Port 7, XT2	Total of all applicable pins				15	4
ਰ current	ΣIOAL(2)	Port 8	Total of all applicable pins				15	mA
/ lev	ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				20	
Low	ΣIOAL(4)	PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				45	
	ΣIOAL(5)	Port 0	Total of all applicable pins				45	
	ΣIOAL(6)	Port 0 PWM0, PWM1 SI2P0 to SI2P3	Total of all applicable pins				80	
	ΣIOAL(7)	Ports 2, 3, B	Total of all applicable pins				45	
	ΣIOAL(8)	Ports A, C	Total of all applicable pins				45	
	ΣIOAL(9)	Ports 2, 3, A, B, C	Total of all applicable pins				80	
	ΣIOAL(10)	Port F	Total of all applicable pins				45	
	ΣIOAL(11)	Ports 1, E	Total of all applicable pins				45	
	ΣIOAL(12)	Ports 1, E, F	Total of all applicable pins				80	
Maximum power dissipation	Pd max	QIP100E(14×20)	Ta=-40 to +85°C				320	mW
Operating ambient temperature	Topr				-40		+85	°C
Storage ambient temperature	Tstg				-55		+125	

Note 1-1: Average output current is average of current in 100ms interval.

 $\textbf{Recommended Operating Conditions} \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V_{SS} = 0 \ \ \text{and} \ \ \text{and} \ \ \text{and} \ \ \text{and} \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{and} \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}3 = V_{SS}3 = V_{SS}3 = V_{SS}3 = V_{SS}3 = V_{SS}4 = 0 \ \ \text{at } Ta = -40^{\circ}C \ \ \text{to} \ +85^{\circ}C, \ \ V_{SS}1 = V_{SS}3 = V_{SS}$ 

Parameter	Symbol	Pins/Remarks	Conditions			Specif	ication	1
. arameter	Gy	e/i telliame	- Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Operating	V <sub>DD</sub> (1)	V <sub>DD</sub> 1=V <sub>DD</sub> 2	0.245μs≤ tCYC≤200μs		2.8		5.5	
supply voltage (Note2-1)		=V <sub>DD</sub> 3=V <sub>DD</sub> 4	0.367μs≤ tCYC≤200μs		2.5		5.5	
(Note2-1)			1.470µs≤ tCYC≤200µs		2.2		5.5	
Memory sustaining supply voltage	VHD	V <sub>DD</sub> 1=V <sub>DD</sub> 2 =V <sub>DD</sub> 3=V <sub>DD</sub> 4	RAM and register contents in HOLD mode.		2.0		5.5	
High level input voltage	V <sub>IH</sub> (1)	Ports 1, 2, 3 SI2P0 to SI2P3 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	Ports 0, 8 Ports A, B, C, E, F PWM0, PWM1		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	V
	V <sub>IH</sub> (3)	P70 Watchdog timer side		2.2 to 5.5	0.9V <sub>DD</sub>		$V_{DD}$	
	V <sub>IH</sub> (4)	XT1, XT2, CF1, RES		2.2 to 5.5	0.75V <sub>DD</sub>		$V_{DD}$	
Low level input voltage	V <sub>IL</sub> (1)	Ports 1, 2, 3 SI2P0 to SI2P3 P71 to P73		4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
		P70 port input/ interrupt		2.2 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	Ports 0, 8 Ports A, B, C, E, F		4.0 to 5.5	V <sub>SS</sub>		0.15V <sub>DD</sub> +0.4	
		PWM0, PWM1		2.2 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (5)	Port 70 Watchdog Timer		2.2 to 5.5	V <sub>SS</sub>		0.8V <sub>DD</sub> -1.0	
	V <sub>IL</sub> (6)	XT1, XT2, CF1, RES		2.2 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
Instruction cycle	tCYC			2.8 to 5.5	0.245		200	
time (Note2-2)				2.5 to 5.5	0.367		200	μs
				2.2 to 5.5	1.470		200	
External system clock frequency	FEXCF(1)	CF1	CF2 pin open     System clock frequency	2.8 to 5.5	0.1		12	
			division rate=1/1 • External system clock	2.5 to 5.5	0.1		8	
			duty=50±5%	2.2 to 5.5	0.1		2	MHz
			CF2 pin open	2.8 to 5.5	0.2		24.4	
			System clock frequency	2.5 to 5.5	0.2		16	
			division rate=1/2	2.2 to 5.5	0.2		4	
Oscillation frequency	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.8 to 5.5		12		
Range (Note2-3)	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		MHz
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.2 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation. See Fig. 2.	2.2 to 5.5		32.768	_	kHz

Note 2-1: V<sub>DD</sub> must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

# **Electrical Characteristics** at $Ta = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V$

				100-	332	Specific	ation	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF V <sub>IN=VDD</sub> (including the off-leak current of the output Tr.)	2.2 to 5.5		21	1	
	I <sub>IH</sub> (2)	XT1, XT2	Using as an input port VIN=VDD	2.2 to 5.5			1	
	I <sub>IH</sub> (3)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	2.2 to 5.5			15	1
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 2 Ports 3, 7, 8 Ports A, B, C, E, F SI2P0 to SI2P3 RES PWM0, PWM1	Output disable Pull-up resistor OFF  VIN=VSS (including the off-leak current of the output Tr.)	2.2 to 5.5	-1			μΑ
	I <sub>IL</sub> (2)	XT1, XT2	Using as an input port VIN=VSS	2.2 to 5.5	-1			
	I <sub>IL</sub> (3)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	2.2 to 5.5	-15			
High level output	V <sub>OH</sub> (1)	Ports 0, 1, 2, 3	I <sub>OH</sub> =-1.0mA	4.5 to 5.5	V <sub>DD</sub> -1			
voltage	V <sub>OH</sub> (2)	Ports A, B, C, E, F SI2P0 to SI2P	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (4)	Ports 71, 72, 73	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (5)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (6)	PWM0, PWM1 P30, P31(PWM4, 5	I <sub>OH</sub> =-10mA	4.5 to 5.5	V <sub>DD</sub> -1.5			
	V <sub>OH</sub> (7)	output mode)	I <sub>OH</sub> =-1.6mA	3.0 to 5.5	V <sub>DD</sub> -0.4			V
	V <sub>OH</sub> (8)		I <sub>OH</sub> =-1.0mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
Low level output	V <sub>OL</sub> (1)	Ports 0, 1, 2, 3	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	
voltage	V <sub>OL</sub> (2)	Ports A, B, C, E, F	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (3)	SI2P0 to SI2P3 PWM0, PWM1,	I <sub>OL</sub> =1.0mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (4)	P00, P01	I <sub>OL</sub> =30mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (5)		I <sub>OL</sub> =5.0mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (6)		I <sub>OL</sub> =2.5mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (7)	Ports 7, 8, XT2	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (8)		I <sub>OL</sub> =1.0mA	2.2 to 5.5			0.4	
Pull-up resistation	Rpu(1)	Ports 0, 1, 2, 3	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	
	Rpu(2)	Port 7 Ports A, B, C, E, F		2.2 to 5.5	15	35	120	kΩ
Hysteresis voltage	VHYS	RES Ports 1, 2, 7 SI2P0 to SI2P3		2.2to 5.5		0.1V <sub>DD</sub>		V
Pin capacitance	СР	All pins	For pins other than that under test: V <sub>IN</sub> =V <sub>SS</sub> f=1MHz     Ta=25°C	2.2 to 5.5		10		pF

# Serial I/O Characteristics at Ta = -40°C to +85°C, $V_SS1 = V_SS2 = V_SS3 = V_SS4 = 0V$

# 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

	D	arameter	Cumbal	Pins	Conditions			Speci	fication			
	Pi	arameter	Symbol	/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit		
		Frequency	tSCK(1)	SCK0(P12)	• See Fig. 6.		2					
		Low level pulse width	tSCKL(1)						1			
		High level pulse width	tSCKH(1)				1					
	Input clock		tSCKHA(1a)		Continuous data transmission/reception mode SIO2 is not in use simultaneous. See Fig. 6. (Note 4-1-2)	2.2 to 5.5	4			tCYC		
Serial clock			tSCKHA(1b)		Continuous data transmission/reception mode SIO2 is in use simultaneous. See Fig. 6. (Note 4-1-2)		6					
Serial		Frequency	tSCK(2)	SCK0(P12)	CMOS output selected.     See Fig. 6.		4/3					
		Low level pulse width	tSCKL(2)					1/2		.0016		
		High level tSCKH(2) pulse width					1/2		tSCK			
	Output clock		tSCKHA(2a)		Continuous data transmission/reception mode SIO2 is not in use simultaneous. CMOS output selected. See Fig. 6.	2.2 to 5.5	tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC			
			tSCKHA(2b)		Continuous data transmission/reception mode SIO2 is in use simultaneous. CMOS output selected. See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(16/3) tCYC	tCYC		
nput	Da	ta setup time	tsDI(1)	SI0(P11), SB0(P11)	Must be specified with respect to rising edge of SIOCLK     See fig. 6.		0.03					
Serial input	Da	ta hold time	thDI(1)		· Gee rig. C.	2.2 to 5.5	0.03					
	clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11),	Continuous data transmission/reception mode     (Note 4-1-3)				(1/3)tCYC +0.05			
output	Serial output		tdD0(2)		• Synchronous 8-bit mode. • (Note 4-1-3)	224-55			1tCYC +0.05	μs		
Serial	Output clock		tdD0(3)		• (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05			

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

# 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

	П	arameter	Cumbal	Pins/	Conditions			Speci	fication	
	P	arameter	Symbol	Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	¥	Frequency	Tsck(3)	SCK1(P15)	• See Fig. 6.		2			
	Input clock	Low level pulse width	tSCKL(3)			2.2 to 5.5	1			.0)(0
Serial clock	ln	High level pulse width	tSCKH(3)				1			tCYC
	Output clock	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected.     See Fig. 6.		2			
		Low level pulse width	tSCKL(4)			2.2 to 5.5	1/2			10014
		High level pulse width	tSCKH(4)					1/2		tSCK
Serial input	Data setup time		tsDI(2)	SI1(P14), SB1(P14)	Must be specified with respect to rising edge of SIOCLK     See fig. 6.		0.03			
Serial	Data hold time		thDI(2)			2.2 to 5.5	0.03			
Serial output	Ou	tput delay e	tdD0(4)	SO1(P13), SB1(P14)	Must be specified with respect to falling edge of SIOCLK     Must be specified as the time to the beginning of output state change in open drain output mode.     See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	μѕ

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

## 3. SIO2 Serial I/O Characteristics (Note 4-3-1)

	Da	arameter	Symbol	Pins/	Conditions			Spec	cification	
		arameter	Symbol	Remarks	Conditions	V <sub>DD</sub> [V]	min.	typ	max.	unit
		Frequency	tSCK(5)	SCK2 (SI2P2)	• See Fig. 6.		2			
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
	Input clock		tSCKHA(5a)		Continuous data transmission/ reception mode of SIO0 is not in use simultaneous.  See Fig. 6.  (Note 4-3-2)	2.2 to 5.5	4			tCYC
Serial clock			tSCKHA(5b)		Continuous data transmission/ reception mode of SIO0 is in use simultaneous.  See Fig. 6.  (Note 4-3-2)		7			
Seria		Frequency	tSCK(6)	SCK2 (SI2P2),	CMOS output selected.     See Fig. 6.		4/3			
		Low level pulse width	tSCKL(6)	SCK2O (SI2P3)	-			1/2		tSCK
		High level pulse width	tSCKH(6)					1/2		ISCK
	Output clock		tSCKHA(6a)	Continuous data transmission/ reception mode of SIO0 is not in use simultaneous.  CMOS output selected.  See Fig. 6.	2.2 to 5.5	tSCKH(6) +(5/3)tCYC		tSCKH(6) +(10/3)tCYC	101/0	
			tSCKHA(6b)		Continuous data transmission/reception mode of SIO0 is in use simultaneous.  CMOS output selected.  See Fig. 6.		tSCKH(6) +(5/3)tCYC		tSCKH(6) +(19/3)tCYC	tCYC
input	Da	ta setup time	tsDI(3)	SI2(SI2P1), SB2(SI2P1)	Must be specified with respect to rising edge of SIOCLK     See fig. 6.		0.03			
Serial input	Da	ta hold Time	thDI(3)			2.2 to 5.5	0.03			
Serial output		Output delay tdD0(5) SO2 (SI2P0), SB2(SI2P1)		Must be specified with respect to falling edge of SIOCLK     Must be specified as the time to the beginning of output state change in open drain output mode.     See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	нѕ µѕ	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input, a time from SI2RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

# Pulse Input Conditions at Ta = -40°C to +85°C, $V_SS1 = V_SS2 = V_SS3 = V_SS4 = 0V$

Parameter	Symbol	Pins/Remarks	Conditions		Specification			
Farameter	Symbol	FIIIS/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High/low level	h/low level tPIH(1) INT0(P70), • Interrupt source flag can be set.		Interrupt source flag can be set.					
pulse width	tPIL(1)	INT1(P71),	Event inputs for timer 0 or 1 are					
		INT2(P72)	enabled.					
		INT4(P20 to P23),	2.2 to 5.		1			
		INT5(P24 to P27),						
		INT6(P20)						
		INT7(P24)						tCYC
	tPIH(2)	INT3(P73) when noise filter	Interrupt source flag can be set.	2.2 to 5.5	2			
	tPIL(2)	time constant is 1/1.	Event inputs for timer 0 are enabled.	2.2 10 3.3	2			
	tPIH(3)	INT3(P73)(The noise rejection	Interrupt source flag can be set.	2.2 to 5.5	64			
	tPIL(3)	clock is selected to 1/32.)	Event inputs for timer 0 are enabled.	2.2 10 5.5	64			
			Interrupt source flag can be set.	2.2 to 5.5	256			
			Event inputs for timer 0 are enabled.	2.2 (0 5.5	256			
	tPIL(5)	RES	Reset acceptable.	2.2 to 5.5	200			μs

# AD Converter Characteristics at Ta = -40°C to +85°C, $V_SS1 = V_SS2 = V_SS3 = V_SS4 = 0V$

			2 111			Specifi	cation	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN7(P87), AN8(P70),	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1), AN11(XT2),	AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	11.74 (tCYC= 0.367μs)		97.92 (tCYC= 3.06μs)	
		AN12(PA3), AN13(PA4), AN14(PA5)		3.0 to 5.5	23.53 (tCYC= 0.735μs)		97.92 (tCYC= 3.06μs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.245μs)		97.92 (tCYC= 1.53μs)	μѕ
				3.0 to 5.5	23.49 (tCYC= 0.367μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	٧
Analog port	IAINH		VAIN=V <sub>DD</sub>	3.0 to 5.5			1	^
input current	IAINL		VAIN=V <sub>SS</sub>	3.0 to 5.5	-1			μΑ

Note 6-1: The quantization error ( $\pm 1/2$  LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the complete digital value corresponding to the analog input value is loaded in the required register.

 $\textbf{Consumption Current Characteristics} \ \, \text{at Ta} = -40^{\circ}\text{C to} \ \, +85^{\circ}\text{C}, \ \, V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0V_{SS} = V_{SS} = V_{SS$ 

Parameter	Symbol	Pins/Remarks	Conditions			Specifi	cation	T
i arameter	Symbol	1 III3/Nemarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3 =V <sub>DD</sub> 4	FmCF=12MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation mode     System clock set to 12MHz side	4.5 to 5.5		10.9	21.5	
(Note 7 1)		,00,	Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/1 frequency division ratio.	2.8 to 4.5		6.1	15.8	
	IDDOP(2)		FmCF=8MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode  System clock set to 8MHz side	4.5 to 5.5		8.1	16.5	
	IDDOP(3)		Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/1 frequency division ratio.	2.5 to 4.5		4.4	11.5	
	IDDOP(4)		FmCF=4MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation mode     System clock set to 4MHz side.	4.5 to 5.5		3.0	7.8	mA
	IDDOP(5)		System clock set to 4MHz side     Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/1 frequency division ratio.	2.2 to 4.5		1.7	4.5	
	IDDOP(6)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode  FmCF=0Hz (oscillation stopped)	4.5 to 5.5		1.1	5.0	
	IDDOP(7)		System clock set to internal RC oscillation     frequency variable RC oscillation stopped     1/2 frequency division ratio.	2.2 to 4.5		0.65	3.5	
	IDDOP(8)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode.	4.5 to 5.5		1.45	6.0	
	IDDOP(9)		System clock set to 1MHz with frequency variable RC oscillation     Internal RC oscillation stopped     1/2 frequency division ratio.	2.2 to 4.5		0.78	4.8	
	IDDOP(10)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode.  Content to the content of 20.768kHz side.	4.5 to 5.5		45	125	^
	IDDOP(11)		System clock set to 32.768kHz side.     Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/2 frequency division ratio.	2.2 to 4.5		23	80	μΑ
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3 =V <sub>DD</sub> 4	HALT mode     FmCF=12MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		3.6	8.3	
(Note 7-1)			System clock set to 12MHz side     Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/1 frequency division ratio.	2.8 to 5.5		2.1	4.4	
	IDDHALT(2)		HALT mode     FmCF=8MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		2.7	5.8	mA
	IDDHALT(3)		System clock set to 8MHz side     Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/1 frequency division ratio.	2.5 to 4.5		1.4	3.1	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pins/Remarks	Conditions			Specifi	cation	1
T didiliotoi	Cymbol	T IIIO/T COMAINO	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(4)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3 =V <sub>DD</sub> 4	HALT mode     FmCF=4MHz ceramic oscillation mode     FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		1.1	2.6	
	IDDHALT(5)		System clock set to 4MHz side     Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/1 frequency division ratio.	2.2 to 4.5		0.57	1.5	
	IDDHALT(6)		HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode	4.5 to 5.5		0.38	1.0	mA
	IDDHALT(7)		System clock set to internal RC oscillation     frequency variable RC oscillation stopped     1/2 frequency division ratio.	2.2 to 4.5		0.19	0.8	IIIA
	IDDHALT(8)		HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode.	4.5 to 5.5		1.15	4.2	
	IDDHALT(9)		System clock set to 1MHz with frequency variable RC oscillation     Internal RC oscillation stopped     1/2 frequency division ratio.	2.2 to 4.5		0.57	3.0	
	IDDHALT(10)		HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode.	4.5 to 5.5		21	77	
	IDDHALT(11)		System clock set to 32.768kHz side.     Internal RC oscillation stopped     frequency variable RC oscillation stopped     1/2 frequency division ratio.	2.2 to 4.5		6	70	μΑ
HOLD mode	IDDHOLD(1)	V <sub>DD</sub> 1	HOLD mode	4.5 to 5.5		0.05	22	
consumption current	IDDHOLD(2)		CF1=V <sub>DD</sub> or open (External clock mode)	2.2 to 4.5		0.02	16	
Timer HOLD mode	IDDHOLD(3)		Timer HOLD mode CF1=VDD or open (External clock mode)	4.5 to 5.5		19	72	
consumption current	IDDHOLD(4)		FmX'tal=32.768kHz by crystal oscillation mode	2.2 to 4.5		5	58	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

# **F-ROM Programming Characteristics** at $Ta = +10^{\circ}C$ to $+55^{\circ}C$ , VSS1 = VSS2 = VSS3 = VSS4 = 0V

Daramatar	Cumbal	Dina/Damarka	Conditions		Specification				
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Onboard programming current	IDDFW(1)	V <sub>DD</sub> 1	Without CPU current	2.7 to 5.5		5	10	mA	
Programming	tFW(1)		Erasing	2.7 to 5.5		20	30	ms	
time	tFW(2)		programming	2.7 to 5.5		40	60	μs	

## **UART (Full Duplex) Operating Conditions** at $Ta = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0\text{V}$

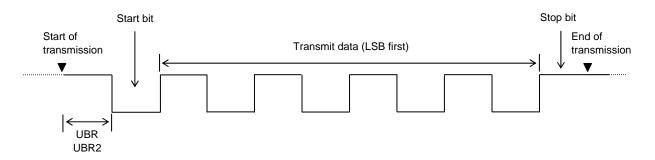
Deremeter	Cumple of	Dia a /D a ma a nice	Conditions		Specificati			ation	
Parameter	Symbol	Pins/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Transfer rate	UBR, UBR2	UTX1(P32), RTX1(P33), UTX2(P33),		2.5 to 5.5	16/3		8192/3	tCYC	
		RTX2(P34)							

Data length: 7/8/9 bits (LSB first)

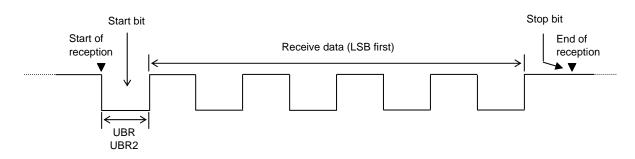
Stop bits : 1-bit (2-bit in continuous data transmission)

Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



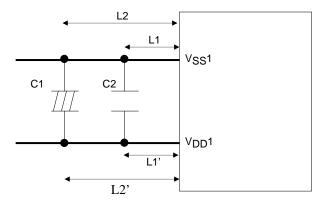
Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



## **VDD1, VSS1 Terminal Condition**

It is necessary to place capacitors between  $V_{\mbox{\scriptsize DD}}1$  and  $V_{\mbox{\scriptsize SS}}1$  as describe below.

- Place capacitors as close to V<sub>DD</sub>1 and V<sub>SS</sub>1 as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- $\bullet$  Capacitance of C2 must be more than 0.1  $\mu F.$
- Use thicker pattern for V<sub>DD</sub>1 and V<sub>SS</sub>1.



## Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1	Characteristics (	of a Sami	ole Main Sv	stem Clock	Oscillator	Circuit with	a Ceramic Oscillator
I auto I	Characteristics t	лаванц	oic iviaili o y	Stelli Ciock	Oscillator	Circuit with	a Ceranne Oscinator

Nominal	Vendor	Oscillator Name	Circuit Constant				Operating Voltage	Oscillation Stabilization Time		Damada							
Frequency	Name		C1	C2	Rf1	Rd1	Range	typ	max	Remarks							
			[pF]	[pF]	[Ω]	[Ω]	[V]	[ms]	[ms]								
12MHz		CSTCE12M0G52-R0	(10)	(10)	Open	470	2.5 to 5.5	0.03	0.5	Internal C1,C2							
10MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	Open	680	2.4 to 5.5	0.03	0.5	Internal C1,C2							
TUIVITZ		CSTLS10M0G53-B0	(15)	(15)	Open	680	2.5 to 5.5	0.03	0.5	Internal C1,C2							
8MHz		MURATA	MURATA	MURATA	MURATA	MURATA	MURATA	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	1k	2.3 to 5.5	0.03	0.5	Internal C1,C2
OIVITZ									-	CSTLS8M00G53-B0	(15)	(15)	Open	1k	2.5 to 5.5	0.03	0.5
45411		CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.03	0.5	Internal C1,C2							
4MHz		CSTLS4M00G53-B0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.03	0.5	Internal C1,C2							

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V<sub>DD</sub> goes above the operating voltage lower limit (see Fig. 4).

## **Characteristics of a Sample Subsystem Clock Oscillator Circuit**

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor	Ossillator Nama	Circuit Constant			Operating Voltage	Oscillation Stabilization Time		Remarks	
	Name	Oscillator Name	C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]	Range [V]	typ [s]	max [s]	Remarks
32.768kHz	EPSON TOYOCOM	MC-306	18	18	Open	560k	2.2 to 5.5	1.5	3.0	Applicable CL value=12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure. 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

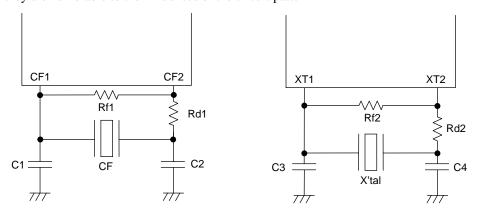
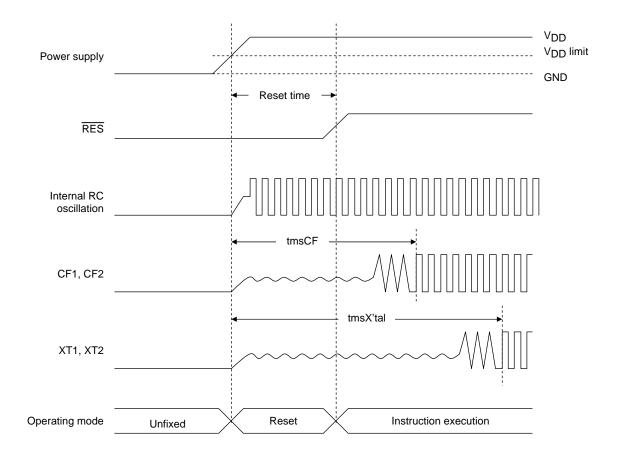


Figure 1 Ceramic Oscillator Circuit

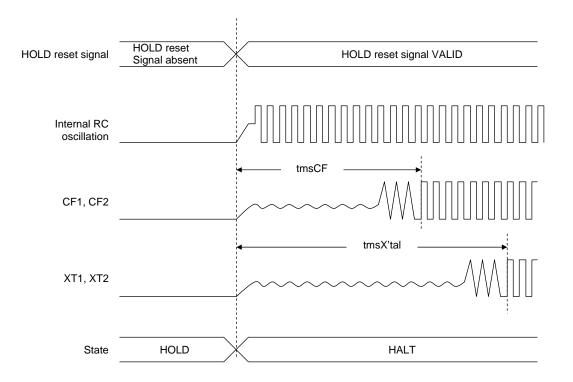
Figure 2 Crystal Oscillator Circuit



Figure 3 AC Timing Measurement Point

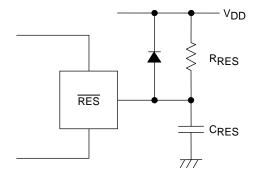


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



#### Note:

Select  $C_{RES}$  and  $R_{RES}$  value to assure that at least 200 $\mu$ s reset time is generated after the  $V_{DD}$  becomes higher than the minimum operating voltage..

Figure 5 Reset Circuit

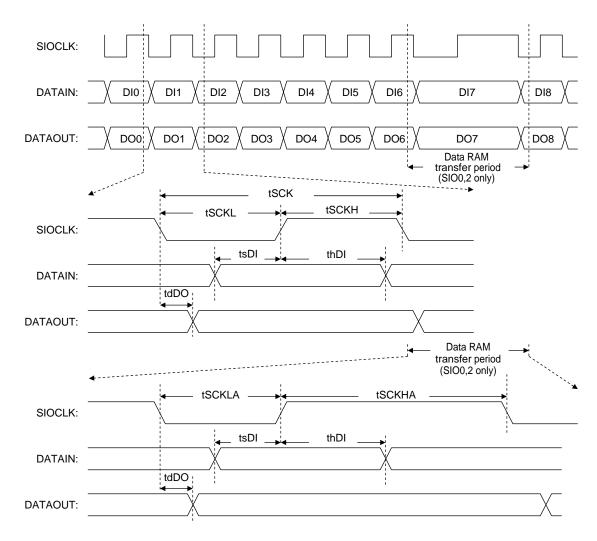


Figure 6 Serial I/O Waveforms

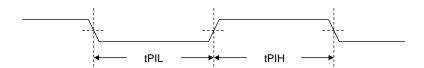


Figure 7 Pulse Input Timing Signal Waveform

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