FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16706-1E

32-bit Microcontroller

CMOS

FR60 MB91313 Series

MB91F313

■ DESCRIPTION

The FR family* is a line of microcontrollers based on a high-performance 32-bit RISC CPU that contains a variety of built-in I/O resources for embedded control applications which require high-performance, high-speed CPU processing.

MB91313 series has multiple communication macro channels, suitable for embedded control applications such as TV control.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURES

1. FR CPU

- 32-bit RISC load/store architecture with a five-stage pipeline
- Operating frequency 33 MHz (oscillator frequency: 16.5 MHz; oscillator frequency multiplier: 2 (PLL clock multiplication method))
- 16-bit fixed length instructions (basic instructions)
- Instruction execution speed : 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions : Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock functions : Facilitates assembly-language coding

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

FUJITSU

- On-chip multiplier supported at the instruction level
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture enabling program access and data access to be executed simultaneously
- Instruction prefetch feature implemented using a 4-word queue in the CPU
- Instruction compatible with the FR family

2. Simple External Bus Interface

- Function as an 8-bit or 16-bit multiplexed bus through programmatic settings
- Operating frequency : Max 16.5 MHz
- Multiplexed I/O for 8/16-bit data/address
- Capable of chip-select signal output for 4 completely independent areas configurable in minimum units of 64 Kbytes
- Basic bus cycle : 3 cycles
- Automatic wait cycle generation function to be programmed for each area
- Unused data/address/control signal pins can serve as general-purpose I/O

3. Built-in Memory

Flash : 544 Kbytes, RAM : 32 Kbytes

4. DMAC (DMA Controller)

- 5 channels
- Two transfer sources : Internal peripheral/software
- Addressing modes : 20/24-bit address selectable (increment/decrement/fixed)
- Transfer modes : Burst transfer/step transfer/block transfer
- Transfer data size : Selectable from 8, 16, or 32 bits

5. Bit Search Module (for REALOS)

Function to search from the MSB (most significant bit) for the position of the first “0”, “1”, or changed bit in a word

6. 16-bit Reload Timer (Including 1 Channel for REALOS)

- 6 channels
- Internal clock: Frequency division selectable from 2, 8, and 32

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7. Serial Interface

- 11 channels
- Full duplex double buffer
- Communication mode : Asynchronous (start-stop synchronization) communication, clock synchronous communication (8.25 Mbps Max), I²C* standard mode (100 kbps Max), high-speed mode (400 kbps Max)
- Parity on/off selectable
- Baud rate generators for each channel
- Extensive error detection functions : Parity, frame, and overrun
- External clock can be used as transfer clock
- Ch.0 to ch.2 : DMA transfers/each equipped with a pair of 16-byte transmit and receive FIFOs
- Ch.8 to ch.10 : 5 V tolerant
- Ch.8 : Open drain outputs
- I²C bridge function (bridges between channels 0, 1, and 2)
- SPI mode

8. Interrupt Controller

- External interrupt lines: Total of 24 lines (INT23 to INT0)
- Interrupts from internal peripherals
- Programmable 16 priority levels
- Capable of using wakeup from STOP mode

9. 10-bit A/D Converter

- 10 channels
- Successive approximation type : Conversion time : About 7.94 µs
- Conversion mode : Single-shot conversion mode, scan conversion mode
- Activation sources : Software/external trigger

10. PPG

- 4 channels
- 16-bit down counter, 16-bit data register with cycle setting buffer
- Internal clock : Frequency division selected from 1, 4, 16, and 64
- Support for automatic cycle setting by DMA transfer
- Function for supporting remote control transmission
- Open drain outputs

11. PWC

- 1 channel (1 input)
- 16-bit up counter
- Simple digital lowpass filter

12. Multi-function Timer

- 4 channels
- Lowpass filter eliminating noise below a pre-set clock frequency
- Capable of pulse width measurement using seven types of clock signals
- Pin input event count function
- Interval timer function using seven types of clock signals and external input clock
- Internal HSYNC counter mode

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13. HDMI-CEC/Remote Control Receiver

- 2 channels
- HDMI-CEC receiver function (with automatic ACK response function)
- Remote control receiver function (built-in 4-byte receive buffer)

14. Other Interval Timers

- Watch timer (32 kHz, counts up to a maximum of 60 seconds)
- Watchdog timer

15. I/O Ports

Max 86 ports

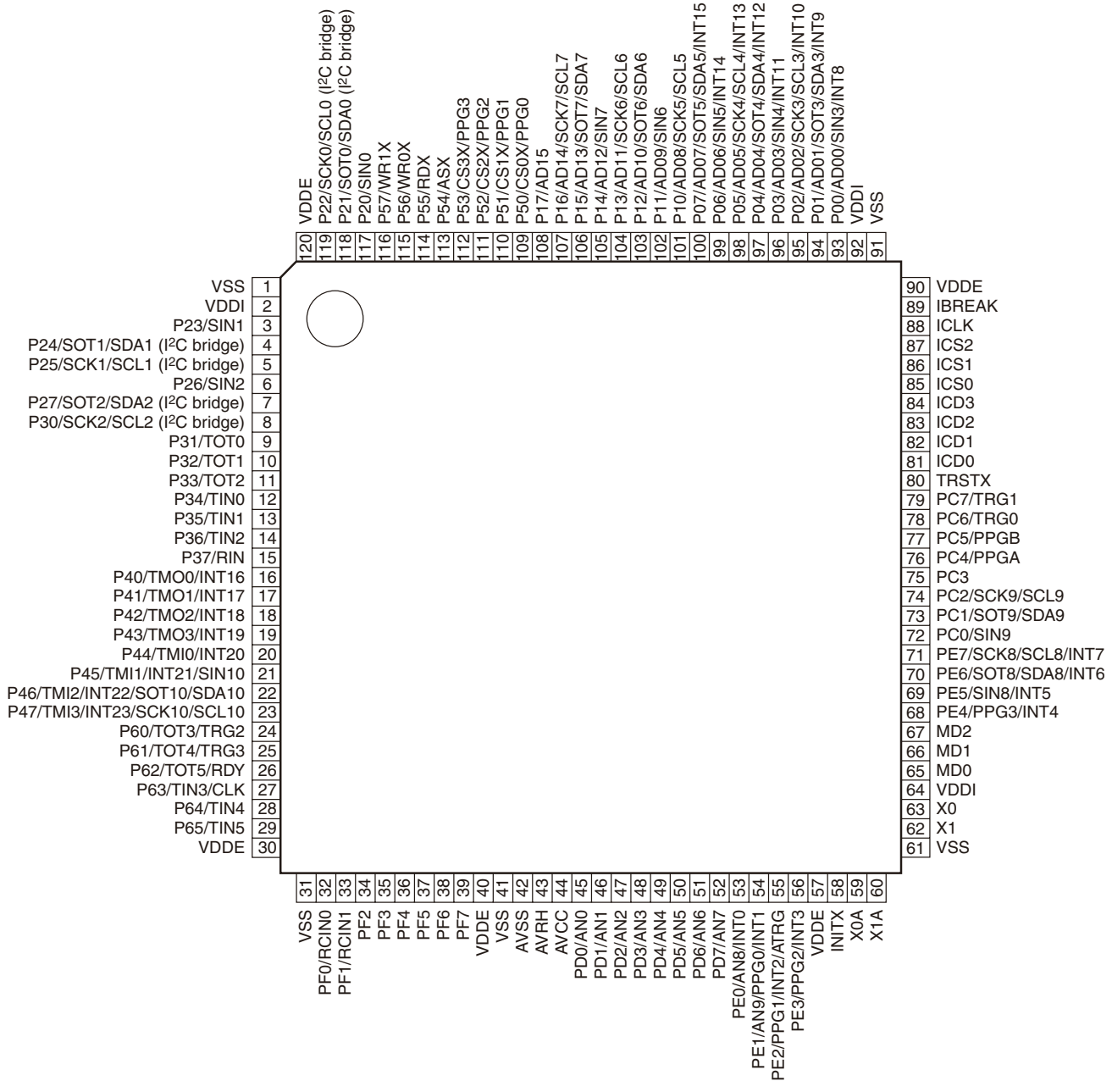
16. Other Features

- Internal oscillator circuit as a clock source
- INITX provided as a reset pin
- Watchdog timer reset and software reset are available
- Stop and sleep modes supported as low-power consumption modes
- Gear function
  - Time-base timer
  - 5 V tolerant I/O (some pins)
- Package LQFP-120, 0.50 mm pitch, 16.0 mm × 16.0 mm
- CMOS technology (0.18μm)
- Power supply voltage 3.3 V ± 0.3 V, 1.8 V ± 0.15 V dual power supply

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-120P-M21)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Description
1	VSS	—	GND pin
2	VDDI	—	1.8 V power supply pin
3	P23	D	General-purpose port
	SIN1		Serial data input pin
4	P24	L	General-purpose port
	SOT1/SDA1 (I^2C bridge)		Serial data output pin/I^2C data I/O pin
5	P25	L	General-purpose port
	SCK1/SCL1 (I^2C bridge)		Serial communication clock I/O pin/I^2C clock I/O pin
6	P26	D	General-purpose port
	SIN2		Serial data input pin
7	P27	L	General-purpose port
	SOT2/SDA2 (I^2C bridge)		Serial data output pin/I^2C data I/O pin
8	P30	L	General-purpose port
	SCK2/SCL2 (I^2C bridge)		Serial communication clock I/O pin/I^2C clock I/O pin
9	P31	D	General-purpose port
	TOT0		Reload timer output pin
10	P32	D	General-purpose port
	TOT1		Reload timer output pin
11	P33	D	General-purpose port
	TOT2		Reload timer output pin
12	P34	D	General-purpose port
	TIN0		Event input pin for reload timer
13	P35	D	General-purpose port
	TIN1		Event input pin for reload timer
14	P36	D	General-purpose port
	TIN2		Event input pin for reload timer
15	P37	D	General-purpose port
	RIN		PWC input pin
16	P40	B	General-purpose port
	TMO0		Multi-function timer output pin
	INT16		External interrupt request input pin

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Pin no.	Pin name	I/O circuit type*	Description
17	P41	B	General-purpose port
	TMO1		Multi-function timer output pin
	INT17		External interrupt request input pin
18	P42	B	General-purpose port
	TMO2		Multi-function timer output pin
	INT18		External interrupt request input pin
19	P43	B	General-purpose port
	TMO3		Multi-function timer output pin
	INT19		External interrupt request input pin
20	P44	B	General-purpose port
	TMI0		Multi-function timer input pin
	INT20		External interrupt request input pin
21	P45	B	General-purpose port
	TMI1		Multi-function timer input pin
	INT21		External interrupt request input pin
	SIN10		Serial data input pin
22	P46	B	General-purpose port
	TMI2		Multi-function timer input pin
	INT22		External interrupt request input pin
	SOT10/SDA10		Serial data output pin/I²C data I/O pin
23	P47	B	General-purpose port
	TMI3		Multi-function timer input pin
	INT23		External interrupt request input pin
	SCK10/SCL10		Serial communication clock I/O pin/I²C clock I/O pin
24	P60	C	General-purpose port
	TOT3		Reload timer output pin
	TRG2		PPG trigger input pin
25	P61	C	General-purpose port
	TOT4		Reload timer output pin
	TRG3		PPG trigger input pin
26	P62	C	General-purpose port
	TOT5		Reload timer output pin
	RDY		External ready input pin

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Pin no.	Pin name	I/O circuit type*	Description
27	P63	C	General-purpose port
	TIN3		Event input pin for reload timer
	CLK		External clock output pin
28	P64	C	General-purpose port
	TIN4		Event input pin for reload timer
29	P65	C	General-purpose port
	TIN5		Event input pin for reload timer
30	VDDE	—	3.3 V power supply pin
31	VSS	—	GND pin
32	PF0	D	General-purpose port
	RCIN0		HDMI-CEC/Remote control 0 I/O pin
33	PF1	D	General-purpose port
	RCIN1		HDMI-CEC/Remote control 1 I/O pin
34	PF2	D	General-purpose port
35	PF3	D	General-purpose port
36	PF4	D	General-purpose port
37	PF5	D	General-purpose port
38	PF6	D	General-purpose port
39	PF7	D	General-purpose port
40	VDDE	—	3.3 V power supply pin
41	VSS	—	GND pin
42	AVSS	—	A/D converter GND pin
43	AVRH	—	A/D converter reference voltage pin
44	AVCC	—	A/D converter power supply pin
45	PD0	L	General-purpose port
	AN0		A/D converter analog input pin
46	PD1	L	General-purpose port
	AN1		A/D converter analog input pin
47	PD2	L	General-purpose port
	AN2		A/D converter analog input pin
48	PD3	L	General-purpose port
	AN3		A/D converter analog input pin
49	PD4	L	General-purpose port
	AN4		A/D converter analog input pin
50	PD5	L	General-purpose port
	AN5		A/D converter analog input pin

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Pin no.	Pin name	I/O circuit type*	Description
51	PD6	L	General-purpose port
	AN6		A/D converter analog input pin
52	PD7	L	General-purpose port
	AN7		A/D converter analog input pin
53	PE0	L	General-purpose port
	AN8		A/D converter analog input pin
	INT0		External interrupt request input pin
54	PE1	L	General-purpose port
	AN9		A/D converter analog input pin
	PPG0		PPG output pin
	INT1		External interrupt request input pin
55	PE2	B	General-purpose port
	PPG1		PPG output pin
	INT2		External interrupt request input pin
	ATRG		A/D converter trigger input pin
56	PE3	B	General-purpose port
	PPG2		PPG output pin
	INT3		External interrupt request input pin
57	VDDE	—	3.3 V power supply
58	INITX	G	Initial reset pin
59	X0A	A	Sub clock input pin
60	X1A	A	Sub clock output pin
61	VSS	—	GND pin
62	X1	A	Main clock output pin
63	X0	A	Main clock input pin
64	VDDI	—	1.8 V power supply pin
65	MD0	F	Mode pin
66	MD1	F	Mode pin
67	MD2	F	Mode pin
68	PE4	B	General-purpose port
	PPG3		PPG output pin
	INT4		External interrupt request input pin
69	PE5	B	General-purpose port
	SIN8		Serial data input pin
	INT5		External interrupt request input pin

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Pin no.	Pin name	I/O circuit type*	Description
70	PE6	B	General-purpose port
	SOT8/SDA8		Serial data output pin/I²C data I/O pin
	INT6		External interrupt request input pin
71	PE7	B	General-purpose port
	SCK8/SCL8		Serial communication clock I/O pin/I²C clock I/O pin
	INT7		External interrupt request input pin
72	PC0	B	General-purpose port
	SIN9		Serial data input pin
73	PC1	B	General-purpose port
	SOT9/SDA9		Serial data output pin/I²C data I/O pin
74	PC2	B	General-purpose port
	SCK9/SCL9		Serial communication clock I/O pin/I²C clock I/O pin
75	PC3	B	General-purpose port
76	PC4	B	General-purpose port
	PPGA		PPG output pin
77	PC5	B	General-purpose port
	PPGB		PPG output pin
78	PC6	B	General-purpose port
	TRG0		PPG trigger input pin
79	PC7	B	General-purpose port
	TRG1		PPG trigger input pin
80	TRSTX	G	Development tool reset pin
81	ICD0	K	Development tool data pin
82	ICD1	K	Development tool data pin
83	ICD2	K	Development tool data pin
84	ICD3	K	Development tool data pin
85	ICS0	H	Development tool status pin
86	ICS1	H	Development tool status pin
87	ICS2	H	Development tool status pin
88	ICLK	H	Development tool clock pin
89	IBREAK	I	Development tool break pin
90	VDDE	—	3.3 V power supply pin
91	VSS	—	GND pin
92	VDDI	—	1.8 V power supply pin

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Pin no.	Pin name	I/O circuit type*	Description
93	P00	O	General-purpose port
	AD00		External address/data bus I/O pin
	SIN3		Serial data input pin
	INT8		External interrupt request input pin
94	P01	O	General-purpose port
	AD01		External address/data bus I/O pin
	SOT3/SDA3		Serial data output pin/I²C data I/O pin
	INT9		External interrupt request input pin
95	P02	O	General-purpose port
	AD02		External address/data bus I/O pin
	SCK3/SCL3		Serial communication clock I/O pin/I²C clock I/O pin
	INT10		External interrupt request input pin
96	P03	O	General-purpose port
	AD03		External address/data bus I/O pin
	SIN4		Serial data input pin
	INT11		External interrupt request input pin
97	P04	O	General-purpose port
	AD04		External address/data bus I/O pin
	SOT4/SDA4		Serial data output pin/I²C data I/O pin
	INT12		External interrupt request input pin
98	P05	O	General-purpose port
	AD05		External address/data bus I/O pin
	SCK4/SCL4		Serial communication clock I/O pin/I²C clock I/O pin
	INT13		External interrupt request input pin
99	P06	O	General-purpose port
	AD06		External address/data bus I/O pin
	SIN5		Serial data input pin
	INT14		External interrupt request input pin
100	P07	O	General-purpose port
	AD07		External address/data bus I/O pin
	SOT5/SDA5		Serial data output pin/I²C data I/O pin
	INT15		External interrupt request input pin
101	P10	O	General-purpose port
	AD08		External address/data bus I/O pin
	SCK5/SCL5		Serial communication clock I/O pin/I²C clock I/O pin

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Pin no.	Pin name	I/O circuit type*	Description
102	P11	O	General-purpose port
	AD09		External address/data bus I/O pin
	SIN6		Serial data input pin
103	P12	O	General-purpose port
	AD10		External address/data bus I/O pin
	SOT6/SDA6		Serial data output pin/I²C data I/O pin
104	P13	O	General-purpose port
	AD11		External address/data bus I/O pin
	SCK6/SCL6		Serial communication clock I/O pin/I²C clock I/O pin
105	P14	O	General-purpose port
	AD12		External address/data bus I/O pin
	SIN7		Serial data input pin
106	P15	O	General-purpose port
	AD13		External address/data bus I/O pin
	SOT7/SDA7		Serial data output pin/I²C data I/O pin
107	P16	O	General-purpose port
	AD14		External address/data bus I/O pin
	SCK7/SCL7		Serial communication clock I/O pin/I²C clock I/O pin
108	P17	O	General-purpose port
	AD15		External address/data bus I/O pin
109	P50	C	General-purpose port
	CS0X		External chip select pin
	PPG0		PPG output pin
110	P51	C	General-purpose port
	CS1X		External chip select pin
	PPG1		PPG output pin
111	P52	C	General-purpose port
	CS2X		External chip select pin
	PPG2		PPG output pin
112	P53	C	General-purpose port
	CS3X		External chip select pin
	PPG3		PPG output pin
113	P54	C	General-purpose port
	ASX		External address strobe output pin

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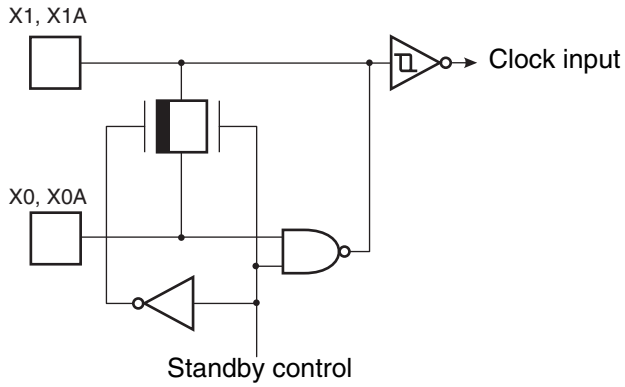
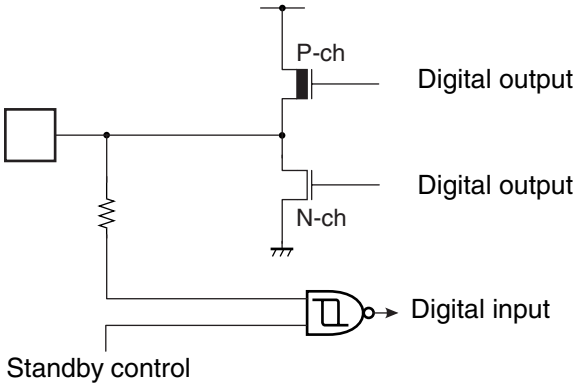
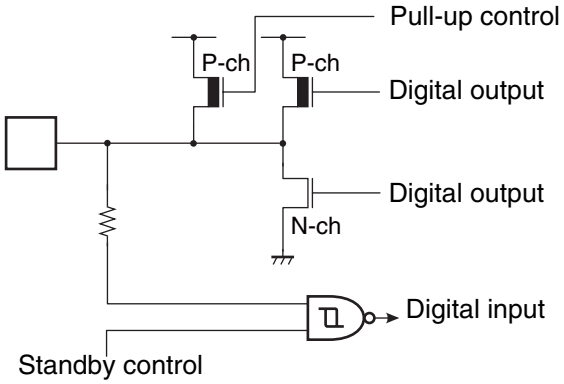
Pin no.	Pin name	I/O circuit type*	Description
114	P55	C	General-purpose port
	RDX		External read strobe output pin
115	P56	C	General-purpose port
	WR0X		External data bus write strobe output pin
116	P57	C	General-purpose port
	WR1X		External data bus write strobe output pin
117	P20	D	General-purpose port
	SIN0		Serial data input pin
118	P21	L	General-purpose port
	SOT0/SDA0 (I^2C bridge)		Serial data output pin/I^2C data I/O pin
119	P22	L	General-purpose port
	SCK0/SCL0 (I^2C bridge)		Serial communication clock I/O pin/I^2C clock I/O pin
120	VDDE	—	3.3 V power supply pin

* : For the details of the I/O circuit types. Refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		Oscillator circuit Internal feedback resistance X0 : 1 MΩ X0A : No
B		• CMOS level output I_{OH} = 4 mA • CMOS level hysteresis input $V_{IH} = 0.7 \times V_{DDE}$ • With standby control • 5 V tolerant
C		• CMOS level output I_{OH} = 4 mA • CMOS level hysteresis input $V_{IH} = 0.8 \times V_{DDE}$ • With standby control • With pull-up control • With pull-up resistor (33 kΩ)

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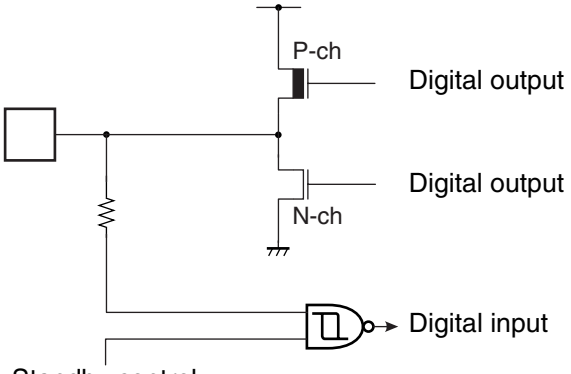
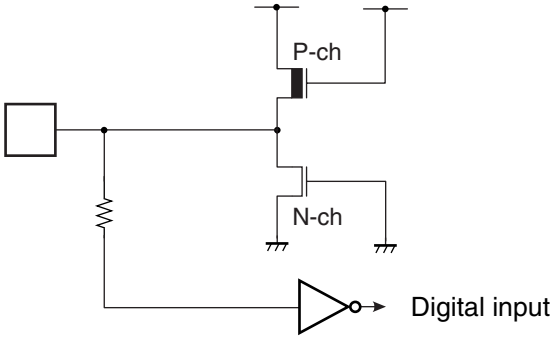
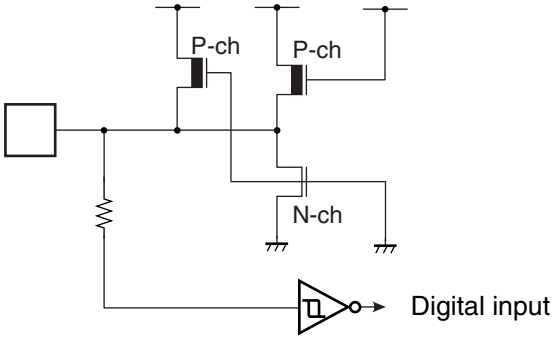
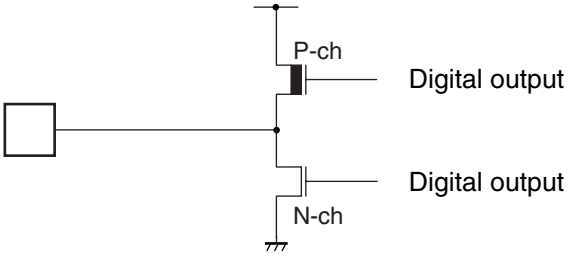
Type	Circuit type	Remarks
D		• CMOS level output I_{OH} = 4 mA • CMOS level hysteresis input V_{IH} = 0.8 × V_{DDE} With standby control Without pull-up resistor
F		• CMOS level input • Without standby control
G		• CMOS hysteresis input • With pull-up resistor
H		CMOS level output

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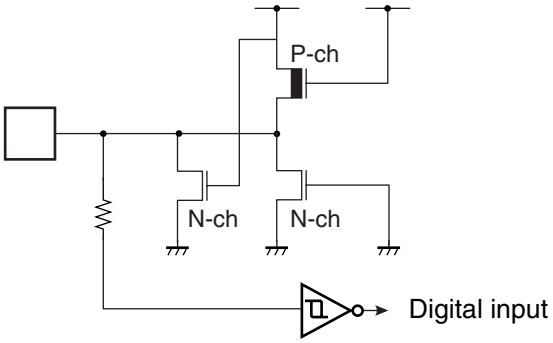
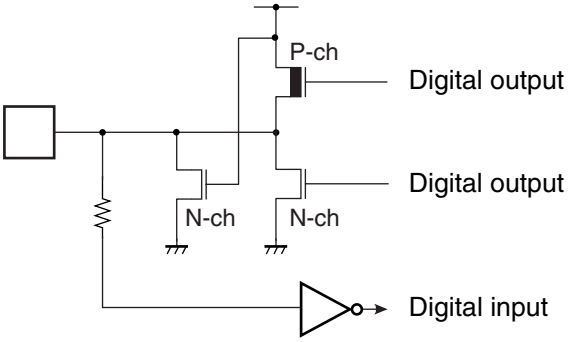
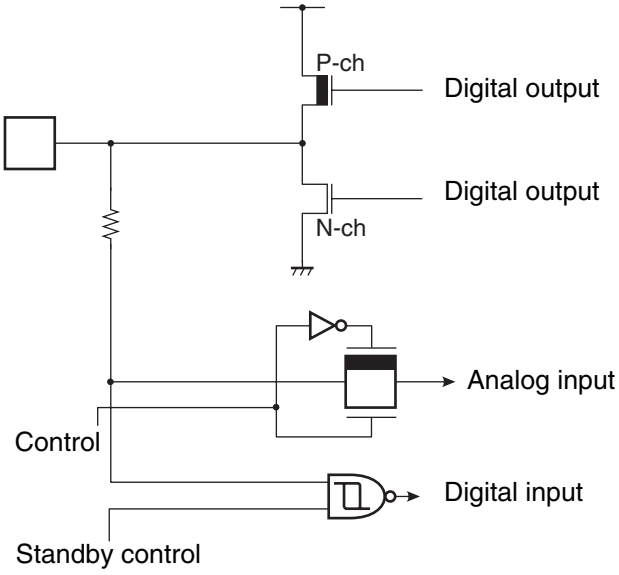
Type	Circuit type	Remarks
I		• CMOS hysteresis input • With pull-down resistor • Without standby control
K		• CMOS level output • CMOS level input • Without standby control • With pull-down resistor
L		• CMOS level output • CMOS level hysteresis input • With standby control • Analog input with switch

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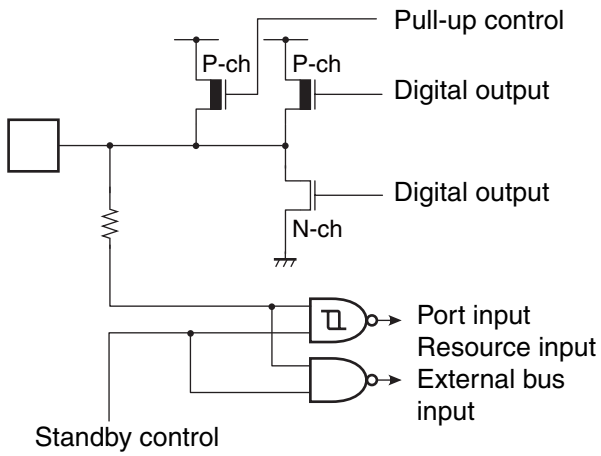
Type	Circuit type	Remarks
O		• CMOS level output I_{OH} = 4 mA • CMOS input (external bus interface) CMOS level hysteresis input (port, resource) $V_{IH} = 0.8 \times V_{DDE}$ • With standby control • With pull-up control • With pull-up resistor (33 kΩ)

■ HANDLING DEVICES

• Preventing latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{DDE} or V_{DDI}, or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rating is applied between VDDE and VSS, or VDDI and VSS. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

• Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor.

• Power supply pins

In MB91313 series, devices including multiple of VDDE pins, VDDI pins and VSS pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pin and GND pin must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the VDDE pins, VDDI pins and VSS pins of the MB91313 series must be connected to the current supply source via a low impedance. It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between VDDE pins, VDDI pins and VSS pins near this device.

• Crystal oscillator circuit

Noise in proximity to the X0 and X1 (X0A, X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

It is recommended that the printed circuit board artwork be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

• Mode pins (MD0 to MD2)

When using mode pins, connect them directly to power supply pin or GND pin. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or GND pin on the printed circuit board as possible and connect them with low impedance.

• Operation at power-on

Ensure that the INITX pin is reset and the settings are initialized (INIT) immediately after the power is turned on.

Maintain the “L” level input to the INITX pin during the stabilization wait time immediately after the power on to ensure the stabilization wait time as required by the oscillator circuit (the stabilization wait time is reset to the minimum value when INIT is asserted using the INITX pin).

• Note on oscillator input at power-on

At power-on, ensure that the clock is input until the oscillator stabilization wait time has elapsed.

• Notes on the turning on/off VDDI pin (1.8 V internal power supply) and VDDE pin (3.3 V external pin power supply)

Do not apply only VDDE pin (external power supply) voltage continuously (more than one minute) while the VDDI pin (internal power supply) is disconnected as it will adversely affect the reliability of the LSI.

When the VDDE pin (external power supply) returns from the off state to the on state, the circuit may not be able to maintain its internal state, for example, due to power supply noise.

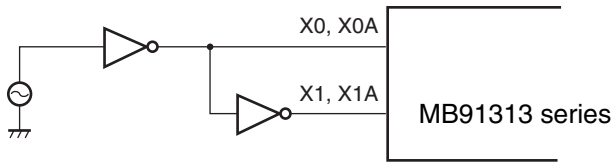
Power on	VDD pin (internal power supply) → VDDE pin (external power supply) → Analog→ Signal
Power off	Signal → Analog→ VDDE pin (external power supply) → VDDI pin (internal power supply)

When the power is turned on, the states of the output pins may remain undefined until the internal power supply becomes stable.

• Notes on using an external clock

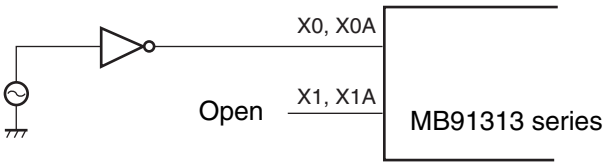
When using the external clock as a general rule you should simultaneously supply X0 (X0A) and X1 (X1A) pins. And also, the clock signal to X0 (X0A) should be supplied a clock signal with the reverse phase to X1 (X1A) pins. However, in this case the stop mode (oscillation stop mode) must not be used (This is because the X1 (X1A) pin stops at “H” output in STOP mode). Furthermore, supply a clock to X0 (X0A) pin only if the device is operating in less than 12.5 MHz.

Using an External Clock (Normal Method)



Cannot be used in STOP mode (oscillation stop mode).

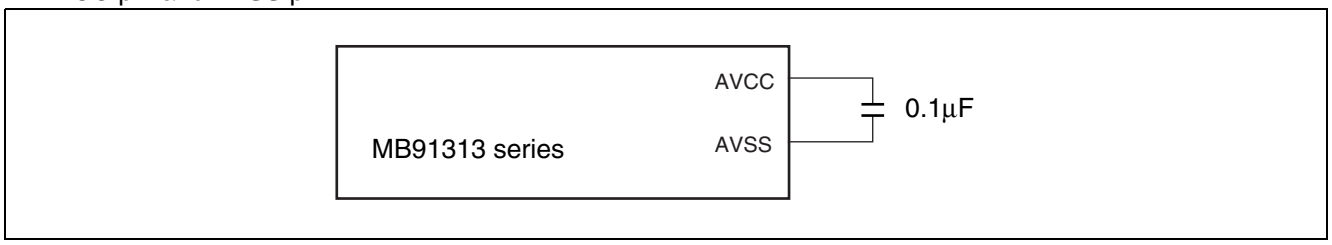
Using an External Clock (available at 12.5 MHz or less)



Note : When operating at a frequency of 10 MHz, the delay between the X0 (X0A) and X1 signals should be less than 15 ns.

• AVCC pin

The MB91313 has a built-in A/D converter. A capacitor of approximately 0.1μF must be connected between the AVCC pin and AVSS pin.



• Notes when not using the emulator

To operate the evaluation MCU on the user system without connecting the emulator, treat each input pin on the evaluation MCU connected to the emulator interface on the user system as shown below.

Note that switching circuits or other measures may be needed on the user system.

Emulator Interface Pin Treatment

Evaluation MCU Pin Name	Pin Connection
TRSTX	Connect to the reset output circuit on the user system.
INITX	Connect to the reset output circuit on the user system.
Other Pins	Open

• Notes on selecting PLL clocks

If the crystal oscillator is disconnected or the clock input stops while the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit within the PLL. However, this operation is not guaranteed.

■ RESTRICTIONS

1) Clock control block

When an “L” level is input to the INITX pin, ensure that it is maintained for the duration of the oscillation stabilization wait time.

2) Bit Search Module

The bit search data register for 0-detection (BSD0), bit search data register for 1-detection (BSD1), and bit search data register for change point detection (BSDC) can be accessed in word.

3) I/O Ports

Ports can only be accessed in byte.

4) Low Power Consumption Mode

- To place the device in standby mode, use the synchronous standby mode (set with bit 8 (SYNCS bit) of the timebase counter control register, TBCR) and be sure to use the following sequence :

```
(LDI#value_of_standby, r0)  ; value_of_standby is the data to write to STCR
(LDI#_STCR, R12)            ; _STCR is the address of STCR (481H)
STB     R0, @R12            ; Write to the standby control register (STCR)
LDUB    @R12, R0            ; Read STCR for synchronous standby
LDUB    @R12, R0            ; Perform an additional dummy read of STCR
NOP                         ; 5 × NOP for timing adjustment
NOP
NOP
NOP
NOP
```

- Do not perform any of the following actions when using the monitor debugger.
  - Set a breakpoint within the sequence of instructions shown above
  - Perform step execution of the sequence of instructions shown above

5) Notes on the PS register

Some instructions write to the PS register in advance before executing. When a debugger is being used, execution may break within an interrupt handler routine, or the values of the flags within the PS register may be updated due to exception processing. However, the microcontroller is designed to reprocess correctly after returning from the EIT, and to execute before and after the EIT proceeds according to the specifications.

- In any following situation, the previous instructions before a DIV0U or DIV0S instruction may take the processing in (1) to (3).

  - A user interrupt or NMI is accepted
  - Step execution is performed
  - A break occurs due to a data event or by being selected from the emulator menu

  (1) The D0 and D1 flags are updated in advance.

  (2) The EIT handling routine (user interrupt/NMI or emulator) is executed.

  (3) Upon returning from the EIT, the DIV0U or DIV0S instruction is executed and the D0/D1 flags are updated back to the same value as in step (1).

- If any of the OR CCR, ST ILM, or MOV Ri, PS instructions are executed to enable a user interrupt or NMI interrupt source when that interrupt has occurred, the following operation will be performed.

  (1) The PS register is updated in advance.

  (2) The EIT handling routine (user interrupt/NMI or emulator) is executed.

  (3) Upon returning from the EIT, the above instructions are executed and the PS registers are updated back to the same value as in step (1).

6) Watchdog timer

The watchdog timer has a function to monitors the program to check that it delays a reset within a certain period of time, and resets the CPU if the program runs out of control and fails to delay the reset. Once the watchdog timer has been enabled, it keeps running until reset. As an exception, the reset is automatically delayed in conditions where the execution of the CPU program stops. It is possible that the watchdog timer will not be triggered if these conditions arise as a result of the system running out of control. In that case, please reset (INIT) using the external INITX pin.

7) Notes on using the A/D converter

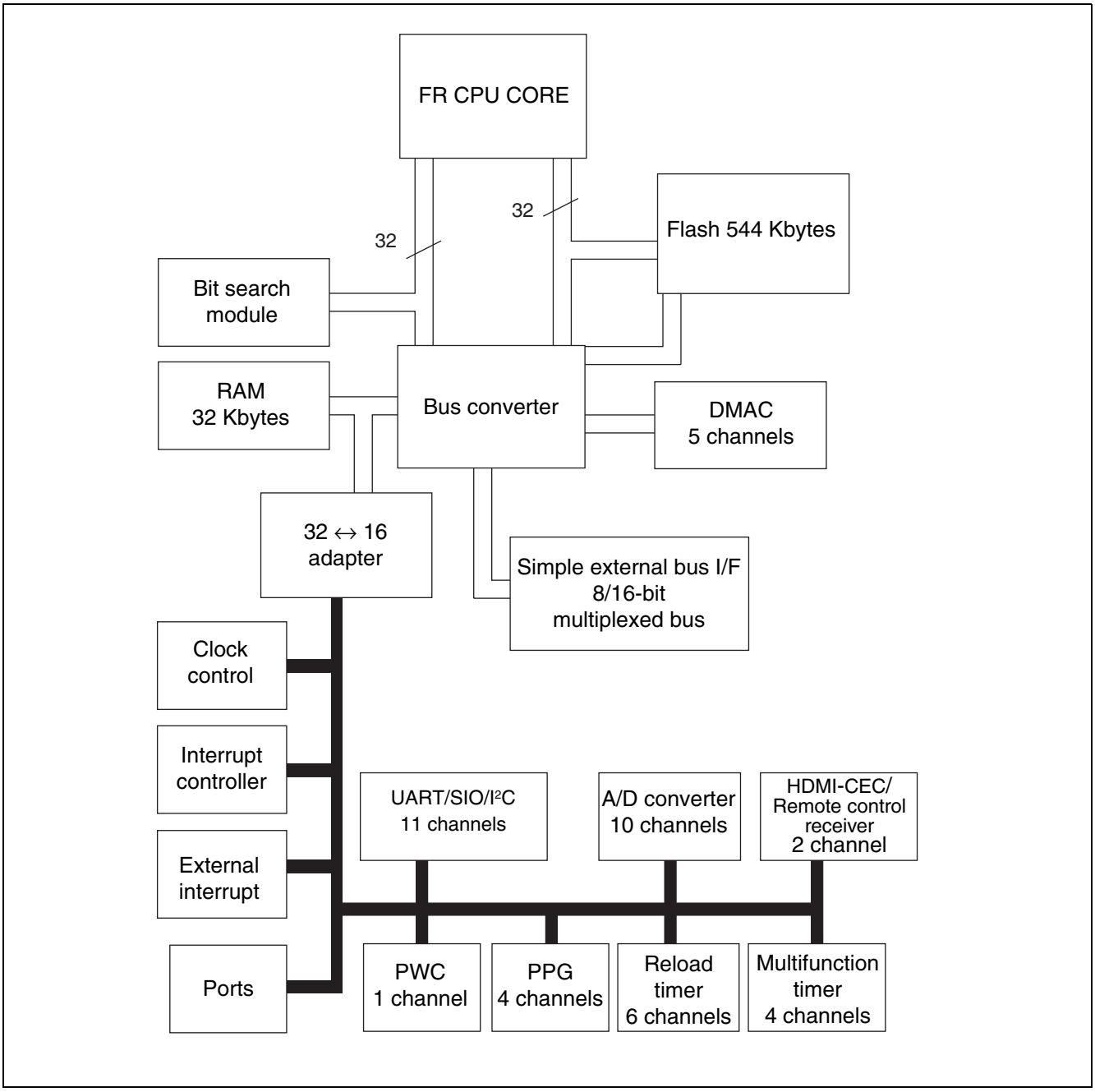
Do not supply a voltage higher than the VDDE pin to the AVCC pin.

8) Software reset in synchronous mode

When using the software reset in synchronous mode, the following two conditions should be satisfied before setting the SRST bit in STCR (standby control register) to “0”.

- The interrupt enable flag (I-Flag) is set to interrupts disabled (I-Flag = 0) .
- The NMI is not being used.

■ BLOCK DIAGRAM



■ CPU AND CONTROL UNIT

Internal architecture

The FR family of CPUs is a line of high-performance cores providing advanced instructions for embedded applications based on the RISC architecture.

1. Features

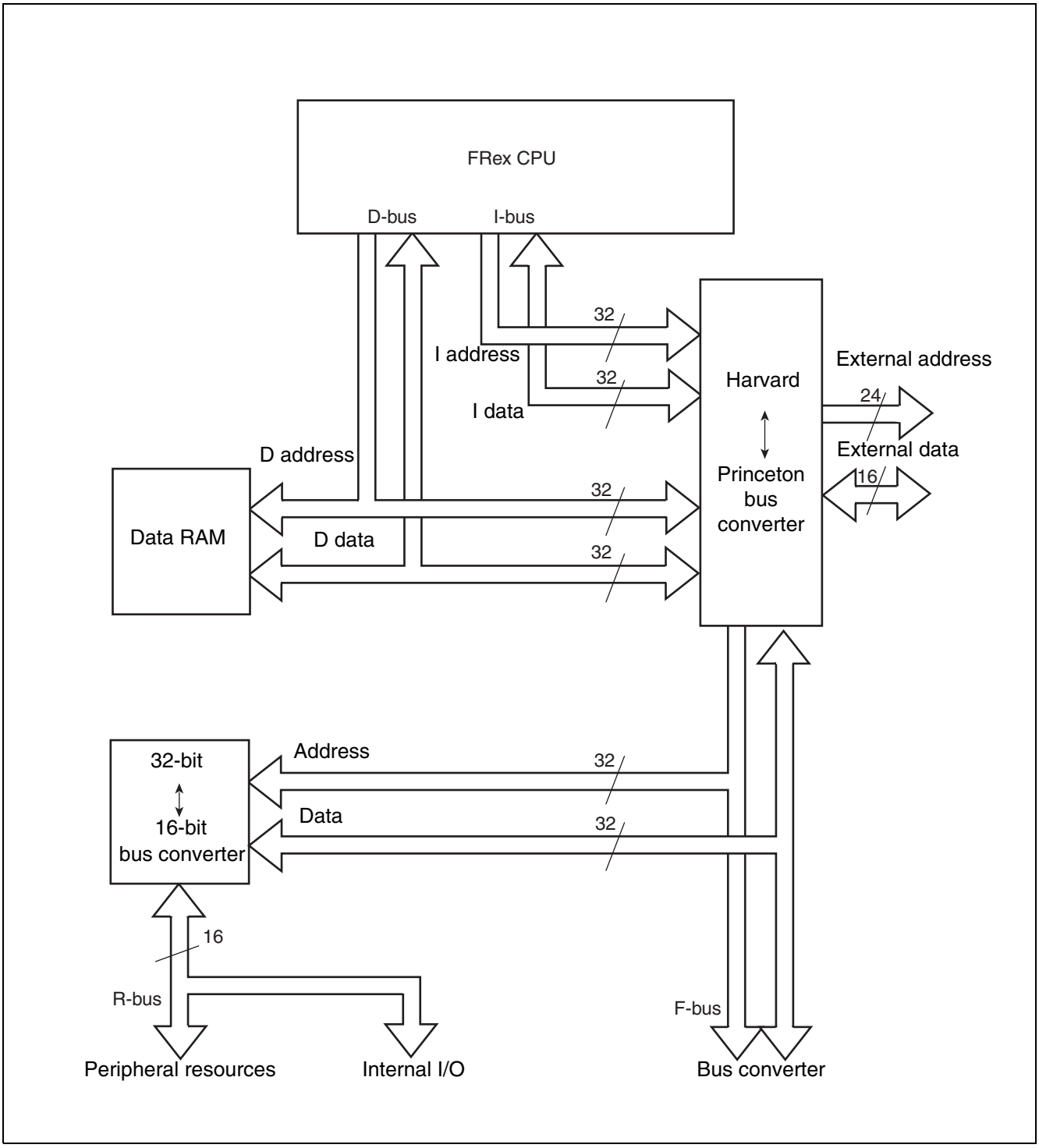
- RISC architecture Basic instructions : Execute at one instruction per cycle
- 32-bit architecture
  General purpose registers : 32 bits × 16
- 4 Gbytes of linear memory space
- Built-in multiplier
  32-bit × 32-bit multiplication : 5 cycles
  16-bit × 16-bit multiplication : 3 cycles
- Enhanced interrupt servicing
  High-speed response (6 cycles)
  Multi-level interrupt support
  Level mask feature (16 levels)
- Enhanced I/O manipulation instructions
  Memory-to-memory transfer instructions
  Bit manipulation instructions
- Basic instruction word length : 16 bits
- Lower-power consumption
  Sleep mode/stop mode
  Gear function

2. Internal architecture

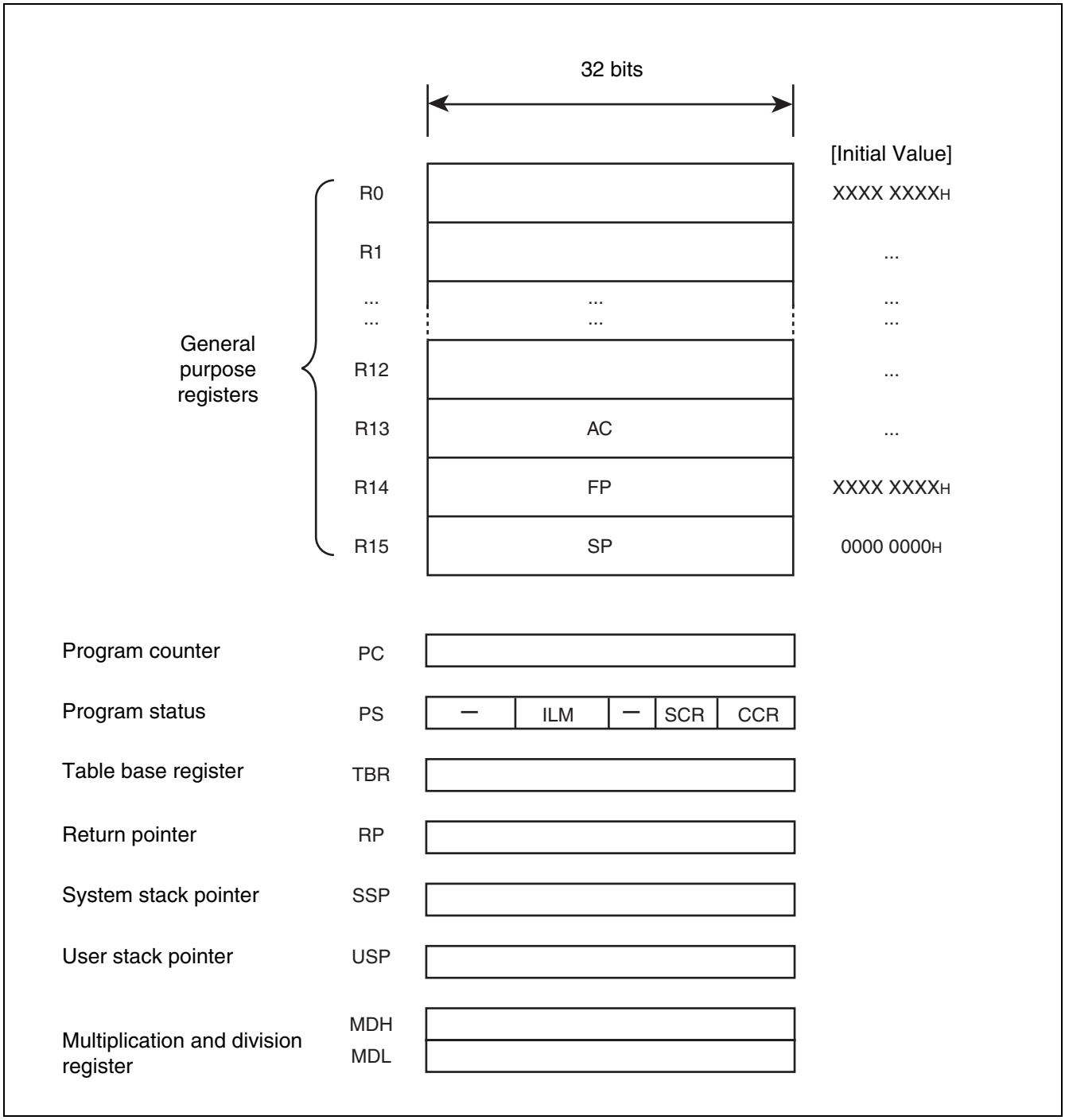
The FR family of CPUs uses a Harvard architecture in which the instruction bus and data bus are separated.

A 32-bit ↔ 16-bit bus converter is connected to the 32-bit bus (F-bus) to provide an interface between the CPU and peripheral resources.

A Harvard ↔ Princeton bus converter is connected to both of the I-bus and D-bus, providing an interface between the CPU and the bus controller.

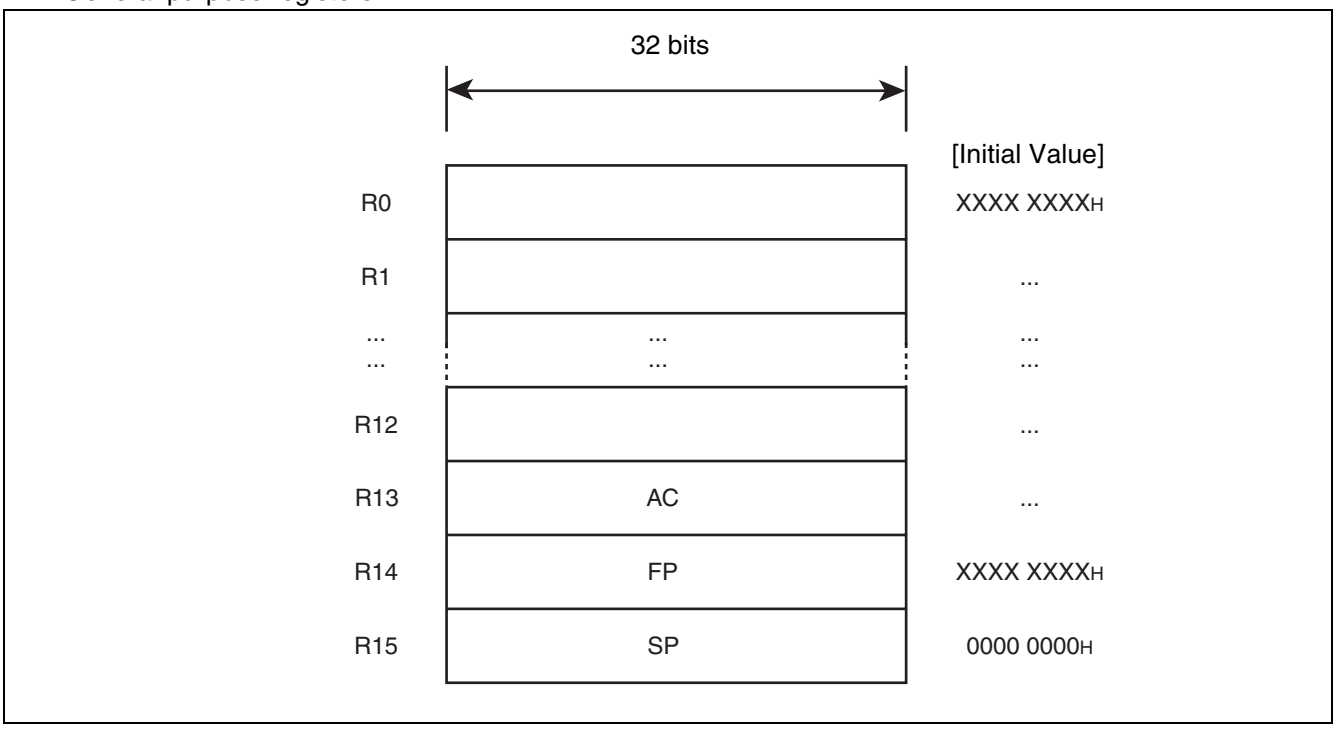


3. Programming model



4. Register

- General-purpose registers



Registers R0 to R15 are general-purpose registers. These registers are used as the accumulator and memory access pointers in CPU operations.

Of these 16 registers, the registers listed below are intended for special applications, for which some instructions are enhanced.

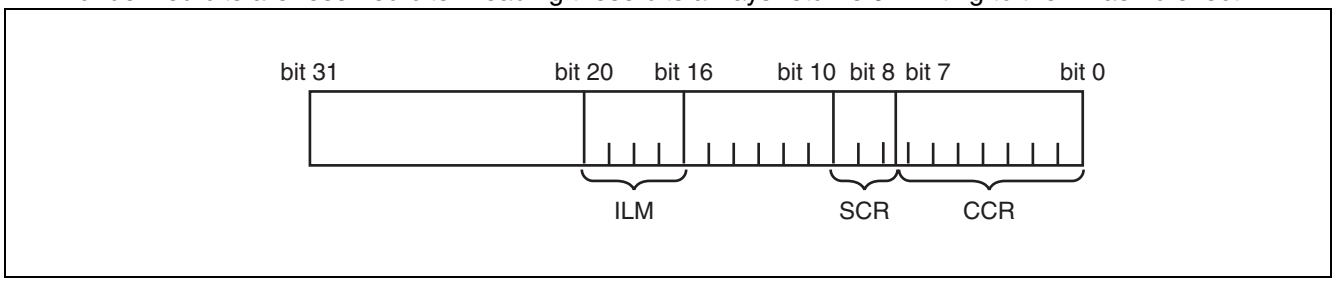
- R13 : Virtual accumulator (AC)
- R14 : Frame pointer (FP)
- R15 : Stack pointer (SP)

The initial values of R0 to R14 after a reset are indeterminate. R15 is initialized to 00000000H (SSP value).

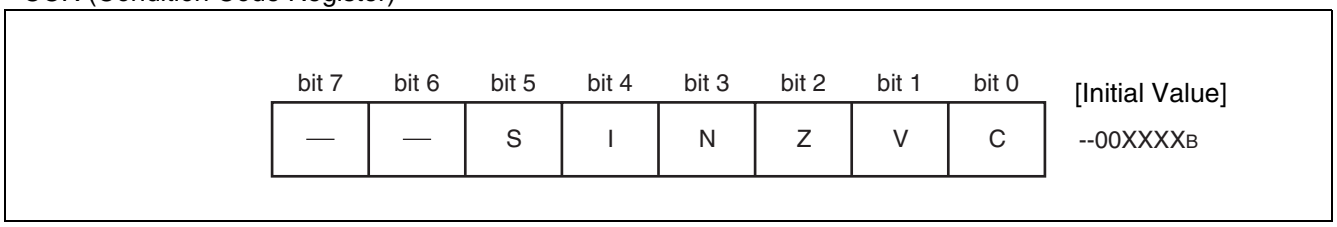
- PS (Program Status)

This register holds the program status and is divided into the ILM, SCR, and CCR.

All undefined bits are reserved bits. Reading these bits always returns 0. Writing to them has no effect.

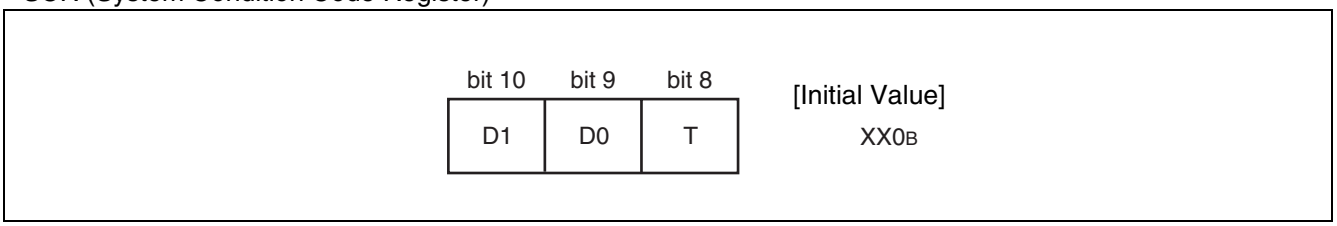


• CCR (Condition Code Register)



S : Stack flag
I : Interrupt Enable flag
N : Negative flag
Z : Zero flag
V : Overflow flag
C : Carrying flag

• SCR (System Condition Code Register)



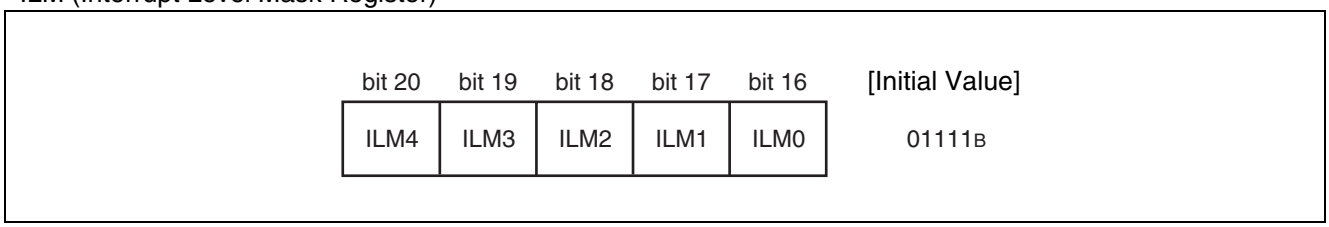
D1, D0 : Flag for step division

This flag stores interim data during execution of step multiplication.

T : Step trace trap flag

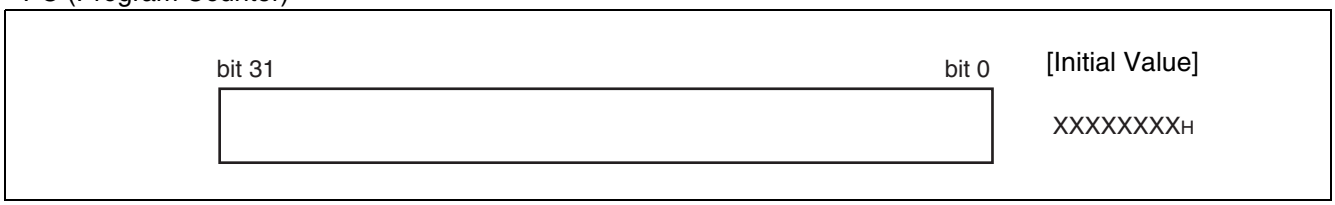
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. This function therefore cannot be used within a user program when an emulator is being used.

• ILM (Interrupt Level Mask Register)



This register stores the value of the interrupt level mask, with the value stored in the ILM used as the interrupt level mask.
The register is initialized to “01111B” on reset.

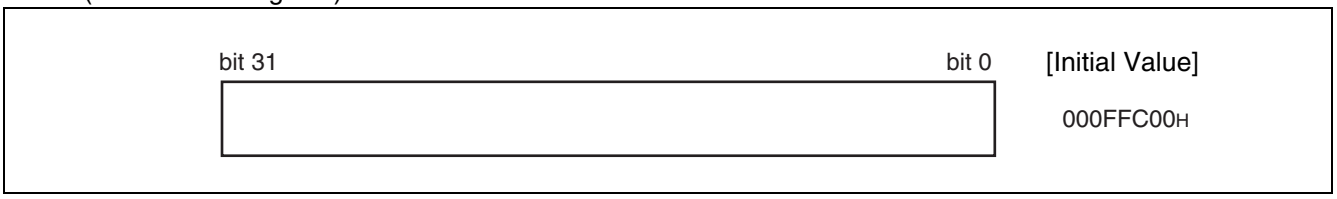
• PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value on reset is undefined.

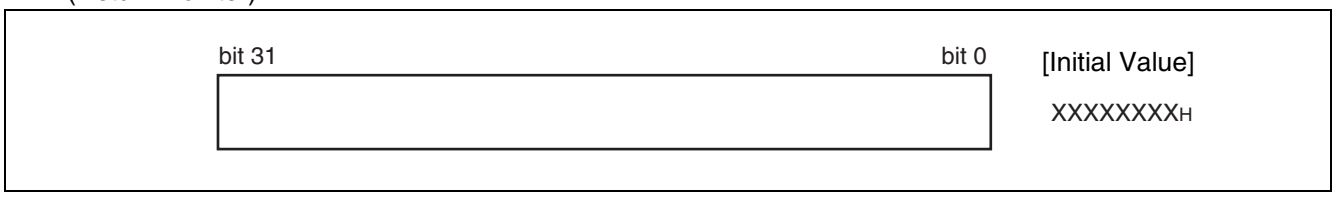
• TBR (Table Base Register)



The table base register stores the starting address of the vector table used for EIT processing.

The initial value on reset is 000FFC00H.

• RP (Return Pointer)



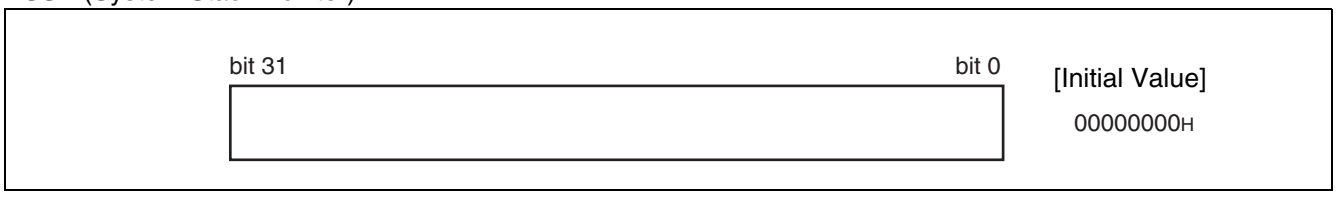
The return pointer stores the address to return from a subroutine.

When the CALL instruction is executed, the value of the PC is transferred to the RP register.

When the RET instruction is executed, the value of the RP is transferred to the PC register.

The initial value on reset is undefined.

• SSP (System Stack Pointer)



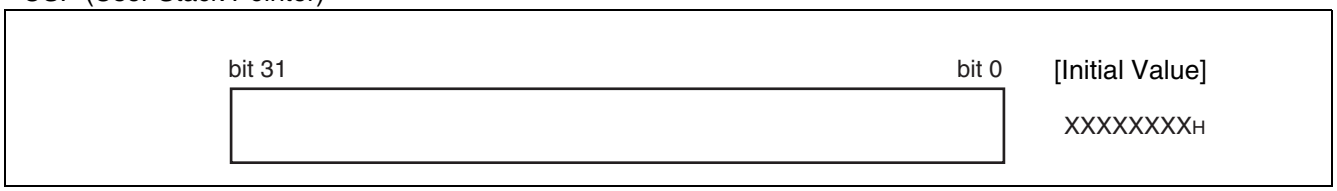
The SSP is the system stack pointer.

The SSP functions as R15 when the S flag is “0”.

The SSP can be explicitly specified. The SSP is also used as the stack pointer that specifies the stack for saving the PS and PC when an EIT event occurs.

The initial value after a reset is 00000000H.

• USP (User Stack Pointer)



The USP is the user stack pointer.

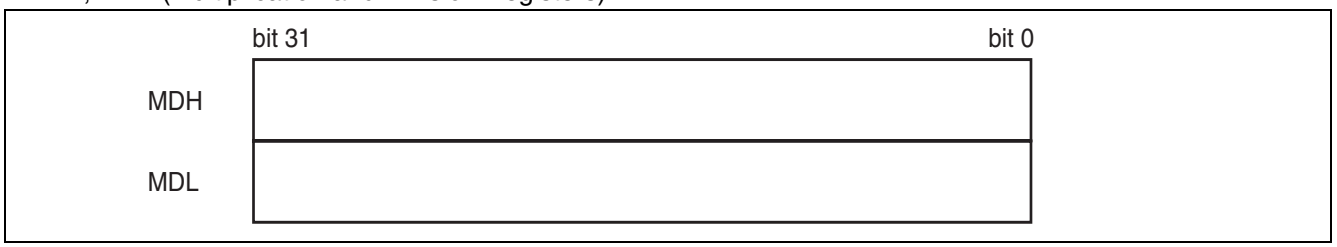
The USP functions as R15 when the S flag is “1”.

The USP can be explicitly specified.

The initial value after a reset is indeterminate.

This pointer cannot be used by the RETI instruction.

• MDH, MDL (Multiplication and Division Registers)



These registers are used for multiplications and divisions and are each 32 bits long.

The initial value after a reset is indeterminate.

■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) linearly accessible to the CPU.

Direct Addressing Areas

The following areas in the address space are used as I/O areas.

These areas are called direct addressing areas. The addresses of operands in these areas can be specified directly within some instructions.

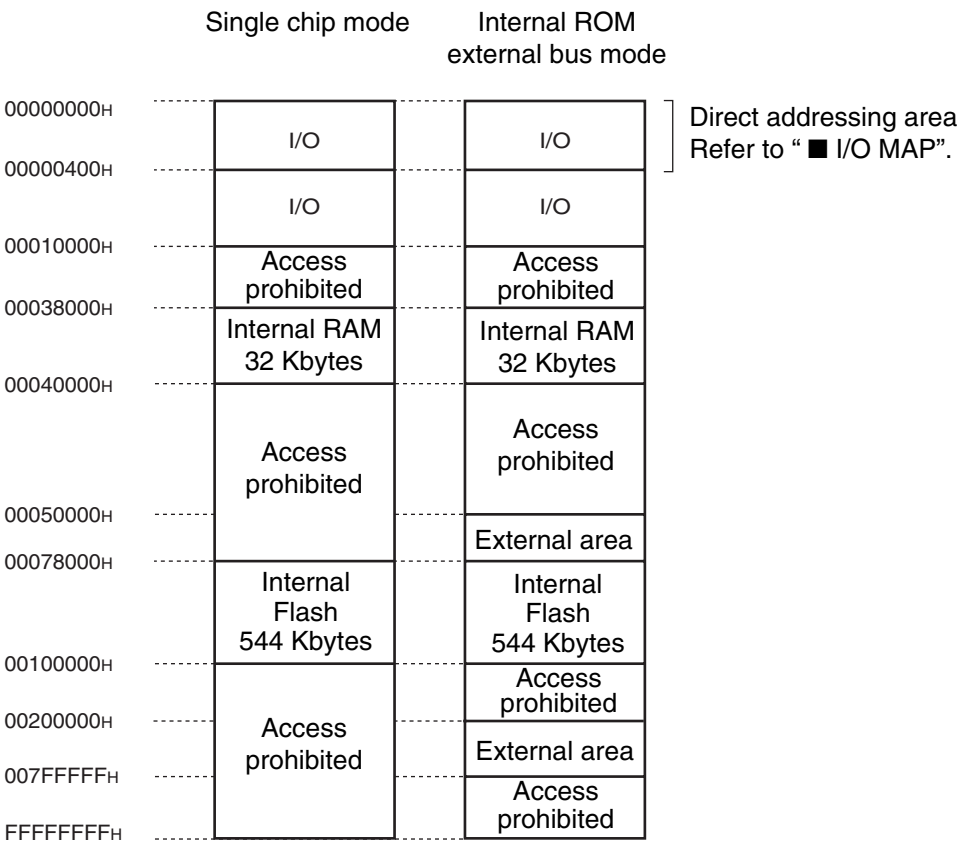
The direct addressing area varies depending on the size of data to be accessed as follows :

→ Byte data access : 000H to 0FFH

→ Half word data access : 000H to 1FFH

→ Word data access : 000H to 3FFH

2. Memory Map

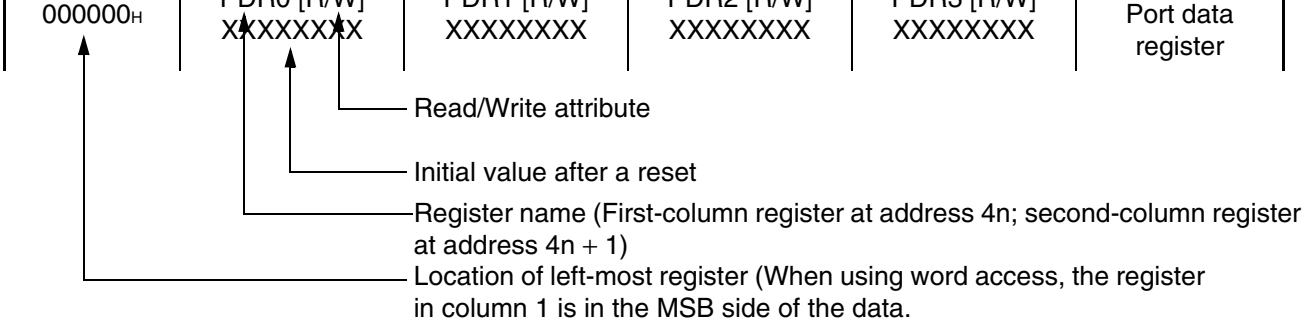


■ I/O MAP

The following table shows the correspondence between the memory space area and each of the peripheral resource registers.

[How to read the table]

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit Port data register



Note : The bit values in the register represent the following initial values :

- “1” : Initial value “1”
- “0” : Initial value “0”
- “X” : Initial value “Undefined”
- “-” : No physical register at this location

Access is prohibited for data access attributes that are not listed.

Address	Register				Block
	0	1	2	3	
000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	Port data register
000004H	PDR4 [R/W] XXXXXXXX	PDR5 [R/W] XXXXXXXX	PDR6 [R/W] --XXXXXX	Reserved	
000008H	Reserved				
00000CH	PDRC [R/W] XXXXXXXX	PDRD [R/W] XXXXXXXX	PDRE [R/W] XXXXXXXX	PDRF [R/W] XXXXXXXX	
000010H to 00001CH	Reserved				Reserved
000020H	ADCTH[R/W] 00000000	ADCTL[R/W] 00000000	ADCH[R/W] 00000000 00000000		10-bit A/D converter
000024H	ADAT0[R] XXXXXX00 00000000		ADAT1[R] XXXXXX00 00000000		
000028H	ADAT2[R] XXXXXX00 00000000		ADAT3[R] XXXXXX00 00000000		
00002CH	ADAT4[R] XXXXXX00 00000000		ADAT5[R] XXXXXX00 00000000		
000030H	ADAT6[R] XXXXXX00 00000000		ADAT7[R] XXXXXX00 00000000		
000034H	ADAT8[R] XXXXXX00 00000000		ADAT9[R] XXXXXX00 00000000		
000038H, 00003CH	Reserved				Reserved
000040H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt 0 to 7
000044H	DICR [R/W] -------0	HRCL [R, R/W] ---11111	Reserved		Delayed/I-unit
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload timer 0
00004CH	Reserved		TMCSR0 [R, RW] 00000000 00000000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload timer 1
000054H	Reserved		TMCSR1 [R, RW] 00000000 00000000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload timer 2
00005CH	Reserved		TMCSR2 [R, RW] 00000000 00000000		

(Continued)

Address	Register				Block
	0	1	2	3	
000060H	SCR0 [R, R/W] 0--00000	SMR0 [W, R/W] 000-0000	SSR0 [R, R/W] 0-000011	ESCR0 [R/W] --000000	Serial interface 0 FIFO 0
000064H	RDR0/TRD0 [R/W] -------- 00000000 : RDR0 -------- 11111111 : TRD0		BGR01 [R/W] 00000000	BGR00 [R/W] 00000000	
000068H	ISMK0 [R/W] 01111110	IBSA [R/W] 00000000	FCR01 [R/W] 00-00100	FCR00 [R/W] 00000000	
00006CH	FBYTE01 [R/W] 00000000	FBYTE00 [R/W] 00000000	Reserved		
000070H	SCR1 [R, R/W] 0--00000	SMR1 [W, R/W] 000-0000	SSR1 [R, R/W] 0-000011	ESCR1 [R/W] --000000	Serial interface 1 FIFO 1
000074H	RDR1/TRD1 [R/W] -------- 00000000 : RDR1 -------- 11111111 : TRD1		BGR11 [R/W] 00000000	BGR10 [R/W] 00000000	
000078H	ISMK1 [R/W] 01111110	IBSA1 [R/W] 00000000	FCR11 [R/W] 00-00100	FCR10 [R/W] 00000000	
00007CH	FBYTE11 [R/W] 00000000	FBYTE10 [R/W] 00000000	Reserved		
000080H	SCR2 [R, R/W] 0--00000	SMR2 [W, R/W] 000-0000	SSR2 [R, R/W] 0-000011	ESCR2 [R/W] --000000	Serial interface 2
000084H	RDR2/TRD2 [R/W] -------- 00000000 : RDR2 -------- 11111111 : TRD2		BGR21 [R/W] 00000000	BGR20 [R/W] 00000000	
000088H	ISMK2 [R/W] 01111110	IBSA2 [R/W] 00000000	FCR21 [R/W] 00-00100	FCR20 [R/W] 00000000	
00008CH	FBYTE21 [R/W] 00000000	FBYTE20 [R/W] 00000000	Reserved		
000090H	SCR3 [R, R/W] 0--00000	SMR3 [W, R/W] 000-0000	SSR3 [R, R/W] 0-000011	ESCR3 [R/W] --000000	Serial interface 3
000094H	RDR3/TRD3 [R/W] -------- 00000000 : RDR3 -------- 11111111 : TRD3		BGR31 [R/W] 00000000	BGR30 [R/W] 00000000	
000098H	ISMK3 [R/W] 01111110	IBSA3 [R/W] 00000000	Reserved		
00009CH	Reserved				
0000A0H	SCR4 [R, R/W] 0--00000	SMR4 [W, R/W] 000-0000	SSR4 [R, R/W] 0-000011	ESCR4 [R/W] --000000	Serial interface 4
0000A4H	RDR4/TRD4 [R/W] -------- 00000000 : RDR4 -------- 11111111 : TRD4		BGR41 [R/W] 00000000	BGR40 [R/W] 00000000	
0000A8H	ISMK4 [R/W] 01111110	IBSA4 [R/W] 00000000	Reserved		
0000ACH	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
0000B0H	SCR5 [R, R/W] 0--00000	SMR5 [W, R/W] 000-0000	SSR5 [R, R/W] 0-000011	ESCR5 [R/W] --000000	Serial interface 5
0000B4H	RDR5/TRD5 [R/W] -------- 00000000 : RDR5 -------- 11111111 : TRD5		BGR51 [R/W] 00000000	BGR50 [R/W] 00000000	
0000B8H	ISMK5 [R/W] 01111110	IBSA5 [R/W] 00000000	Reserved		
0000BCH	Reserved				
0000C0H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt 8 to 15
0000C4H	EIRR2 [R/W] 00000000	ENIR2 [R/W] 00000000	ELVR2 [R/W] 00000000 00000000		External interrupt 16 to 23
0000C8H, 0000CCH	Reserved				Reserved
0000D0H	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	Reserved		PWC
0000D4H	PWCD[R] XXXXXXXX XXXXXXXX		Reserved		
0000D8H	PWCC2[R/W] 000-----	Reserved			
0000DCH	PWCUD[R/W] XXXXXXXX XXXXXXXX		Reserved		
0000E0H to 0000ECH	Reserved				Reserved
0000F0H	T0LPCR [R/W] -----000	T0CCR [R/W] 0-000000	T0TCR [R/W] 00000000	T0R [R/W] ---00000	Multi-function timer
0000F4H	T0DRR [R/W] XXXXXXXX XXXXXXXX		T0CRR [R/W] XXXXXXXX XXXXXXXX		
0000F8H	T1LPCR [R/W] -----000	T1CCR [R/W] 0-000000	T1TCR [R/W] 00000000	T1R [R/W] ---00000	
0000FCH	T1DRR [R/W] XXXXXXXX XXXXXXXX		T1CRR [R/W] XXXXXXXX XXXXXXXX		
000100H	T2LPCR [R/W] -----000	T2CCR [R/W] 0-000000	T2TCR [R/W] 00000000	T2R [R/W] ---00000	
000104H	T2DRR [R/W] XXXXXXXX XXXXXXXX		T2CRR [R/W] XXXXXXXX XXXXXXXX		
000108H	T3LPCR [R/W] -----000	T3CCR [R/W] 0-000000	T3TCR [R/W] 00000000	T3R [R/W] ---00000	
00010CH	T3DRR [R/W] XXXXXXXX XXXXXXXX		T3CRR [R/W] XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	0	1	2	3	
000110H	TMODE [R/W] 00000000 00000000		Reserved		Multi-function timer
000114H to 00011CH	Reserved				Reserved
000120H	PDUT0[W] XXXXXXXX XXXXXXXX		PCSR0[W] XXXXXXXX XXXXXXXX		PPG0
000124H	PTMR0[R] 11111111 11111111		PCNH0[R/W] 0000000-	PCNL0[R/W] 000000-0	
000128H	PDUT1[W] XXXXXXXX XXXXXXXX		PCSR1[W] XXXXXXXX XXXXXXXX		PPG1
00012CH	PTMR1[R] 11111111 11111111		PCNH1[R/W] 0000000-	PCNL1[R/W] 000000-0	
000130H	PDUT2[W] XXXXXXXX XXXXXXXX		PCSR2[W] XXXXXXXX XXXXXXXX		PPG2
000134H	PTMR2[R] 11111111 11111111		PCNH2[R/W] 0000000-	PCNL2[R/W] 000000-0	
000138H	PDUT3[W] XXXXXXXX XXXXXXXX		PCSR3[W] XXXXXXXX XXXXXXXX		PPG3
00013CH	PTMR3[R] 11111111 11111111		PCNH3[R/W] 0000000-	PCNL3[R/W] 000000-0	
000140H, 000144H	Reserved				Reserved
000148H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload timer 3
00014CH	Reserved		TMCSR3 [R, RW] 00000000 00000000		
000150H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload timer 4
000154H	Reserved		TMCSR4 [R, RW] 00000000 00000000		
000158H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload timer 5
00015CH	Reserved		TMCSR5 [R, RW] 00000000 00000000		
000160H to 00017CH	Reserved				Reserved

(Continued)

Address	Register				Block
	0	1	2	3	
000180H	RCCR0 [R/W] 0---0000	RCST0 [R/W] 00000000	RCSHW0 [R/W] 00000000	RCDAHW0 [R/W] 00000000	Remote controller 0
000184H	RCDBHW0 [R/W] 00000000	Reserved	RCADR01 [R/W] 00000000	RCADR02 [R/W] 00000000	
000188H	RCDT0HH [R] 00000000	RCDT0HL [R] 00000000	RCDT0LH [R] 00000000	RCDT0LL [R] 00000000	
00018CH	RCCKD0 [R/W] 00000000 00000000		Reserved		
000190H	RCCR1 [R/W] 0---0000	RCST1 [R/W] 00000000	RCSHW1 [R/W] 00000000	RCDAHW1 [R/W] 00000000	Remote controller 1
000194H	RCDBHW1 [R/W] 00000000	Reserved	RCADR11 [R/W] 00000000	RCADR12 [R/W] 00000000	
000198H	RCDT1HH [R] 00000000	RCDT1HL [R] 00000000	RCDT1LH [R] 00000000	RCDT1LL [R] 00000000	
00019CH	RCCKD1 [R/W] 00000000 00000000		Reserved		
0001A0H to 0001ACH	Reserved				Reserved
0001B0H	SCR6 [R, R/W] 0--00000	SMR6 [W, R/W] 000-0000	SSR6 [R, R/W] 0-000011	ESCR6 [R/W] --000000	Serial interface 6
0001B4H	RDR6/TRD6 [R/W] -------- 00000000 : RDR6 -------- 11111111 : TRD6		BGR61 [R/W] 00000000	BGR60 [R/W] 00000000	
0001B8H	ISMK6 [R/W] 01111110	IBSA6 [R/W] 00000000	Reserved		
0001BCH	Reserved				
0001C0H	SCR7 [R, R/W] 0--00000	SMR7 [W, R/W] 000-0000	SSR7 [R, R/W] 0-000011	ESCR7 [R/W] --000000	Serial interface 7
0001C4H	RDR7/TRD7 [R/W] -------- 00000000 : RDR7 -------- 11111111 : TRD7		BGR71 [R/W] 00000000	BGR70 [R/W] 00000000	
0001C8H	ISMK7 [R/W] 01111110	IBSA7 [R/W] 00000000	Reserved		
0001CCH	Reserved				

(Continued)

Address	Register				Block
	0	1	2	3	
0001D0H	SCR8 [R, R/W] 0--00000	SMR8 [W, R/W] 000-0000	SSR8 [R, R/W] 0-000011	ESCR8 [R/W] --000000	Serial interface 8
0001D4H	RDR8/TRD8 [R/W] -------- 00000000 : RDR8 -------- 11111111 : TRD8		BGR81 [R/W] 00000000	BGR80 [R/W] 00000000	
0001D8H	ISMK8 [R/W] 01111110	IBSA8 [R/W] 00000000	Reserved		
0001DCH	Reserved				
0001E0H	SCR9 [R, R/W] 0--00000	SMR9 [W, R/W] 000-0000	SSR9 [R, R/W] 0-000011	ESCR9 [R/W] --000000	Serial interface 9
0001E4H	RDR9/TRD9 [R/W] -------- 00000000 : RDR9 -------- 11111111 : TRD9		BGR91 [R/W] 00000000	BGR90 [R/W] 00000000	
0001E8H	ISMK9 [R/W] 01111110	IBSA9 [R/W] 00000000	Reserved		
0001ECH	Reserved				
0001F0H	SCRA[R, R/W] 0--00000	SMRA [W, R/W] 000-0000	SSRA [R, R/W] 0-000011	ESCRA[R/W] --000000	Serial interface 10
0001F4H	RDRA/TRDA [R/W] -------- 00000000 : RDRA -------- 11111111 : TRDA		BGRA1 [R/W] 00000000	BGRA0 [R/W] 00000000	
0001F8H	ISMKA [R/W] 01111110	IBSAA [R/W] 00000000	Reserved		
0001FCH	Reserved				
000200H	DMACA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208H	DMACA1 [R/W] 00000000 00000000 00000000 00000000				
00020CH	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210H	DMACA2 [R/W] 00000000 00000000 00000000 00000000				
000214H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218H	DMACA3 [R/W] 00000000 00000000 00000000 00000000				
00021CH	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220H	DMACA4 [R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	0	1	2	3	
000224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				DMAC
000228H to 00023CH	Reserved				
000240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				
000244H to 0003ECH	Reserved				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDR0 [R/W] 00000000	DDR1 [R/W] 00000000	DDR2 [R/W] 00000000	DDR3 [R/W] 00000000	Data direction register
000404H	DDR4 [R/W] 00000000	DDR5 [R/W] 00000000	DDR6 [R/W] --000000	Reserved	
000408H	Reserved				
00040CH	DDRC [R/W] 00000000	DDRD [R/W] 00000000	DDRE [R/W] 00000000	DDRF [R/W] 00000000	
000410H	Reserved				
000414H to 00041CH	Reserved				Reserved
000420H	PFR0 [R/W] 00000000	PFR1 [R/W] 00000000	PFR2 [R/W] 00000000	PFR3 [R/W] 00000000	Port function register
000424H	PFR4 [R/W] 00000000	PFR5 [R/W] 00000000	PFR6 [R/W] --000000	Reserved	
000428H	Reserved				
00042CH	PFRC [R/W] 00000000	PFRD [R/W] 00000000	PFRE [R/W] 00000000	PFRF [R/W] 00000000	
000430H	Reserved				
000434H to 00043CH	Reserved				Reserved

(Continued)

Address	Register				Block
	0	1	2	3	
000440H	ICR00 [R, R/W] ---11111	ICR01 [R, R/W] ---11111	ICR02 [R, R/W] ---11111	ICR03 [R, R/W] ---11111	Interrupt control unit
000444H	ICR04 [R, R/W] ---11111	ICR05 [R, R/W] ---11111	ICR06 [R, R/W] ---11111	ICR07 [R, R/W] ---11111	
000448H	ICR08 [R, R/W] ---11111	ICR09 [R, R/W] ---11111	ICR10 [R, R/W] ---11111	ICR11 [R, R/W] ---11111	
00044CH	ICR12 [R, R/W] ---11111	ICR13 [R, R/W] ---11111	ICR14 [R, R/W] ---11111	ICR15 [R, R/W] ---11111	
000450H	ICR16 [R, R/W] ---11111	ICR17 [R, R/W] ---11111	ICR18 [R, R/W] ---11111	ICR19 [R, R/W] ---11111	
000454H	ICR20 [R, R/W] ---11111	ICR21 [R, R/W] ---11111	ICR22 [R, R/W] ---11111	ICR23 [R, R/W] ---11111	
000458H	ICR24 [R, R/W] ---11111	ICR25 [R, R/W] ---11111	ICR26 [R, R/W] ---11111	ICR27 [R, R/W] ---11111	
00045CH	ICR28 [R, R/W] ---11111	ICR29 [R, R/W] ---11111	ICR30 [R, R/W] ---11111	ICR31 [R, R/W] ---11111	
000460H	ICR32 [R, R/W] ---11111	ICR33 [R, R/W] ---11111	ICR34 [R, R/W] ---11111	ICR35 [R, R/W] ---11111	
000464H	ICR36 [R, R/W] ---11111	ICR37 [R, R/W] ---11111	ICR38 [R, R/W] ---11111	ICR39 [R, R/W] ---11111	
000468H	ICR40 [R, R/W] ---11111	ICR41 [R, R/W] ---11111	ICR42 [R, R/W] ---11111	ICR43 [R, R/W] ---11111	
00046CH	ICR44 [R, R/W] ---11111	ICR45 [R, R/W] ---11111	ICR46 [R, R/W] ---11111	ICR47 [R, R/W] ---11111	
000470H to 00047CH	Reserved				Reserved
000480H	RSRR [R, R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock control unit
000484H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H	Reserved		OSCCR [R/W] XXXXXXX0	Reserved	
00048CH	WPCR [R/W] 00000000	Reserved			Clock timer
000490H	OSCR [R/W] 00000000	OSCT [R/W] XXXXXXXX	Reserved		Stabilization wait timer
000494H to 0004FCH	Reserved				Reserved

(Continued)

Address	Register				Block
	0	1	2	3	
000500H	PCR0 [R/W] 00000000	PCR1 [R/W] 00000000	Reserved		Port pull-up control registers
000504H	Reserved	PCR5 [R/W] 00000000	PCR6 [R/W] --000000	Reserved	
000508H to 000510H	Reserved				
000514H to 00051CH	Reserved				Reserved
000520H	EPFR0 [R/W] 00000000	EPFR1 [R/W] 00000000	EPFR2 [R/W] 11111111	EPFR3 [R/W] 11111111	External port function register
000524H	EPFR4 [R/W] 11111111	EPFR5 [R/W] 11111111	EPFR6 [R/W] --001000	Reserved	
000528H	Reserved				
00052CH	EPFRC [R/W] 00000000	EPFRD [R/W] 00000000	EPFRE [R/W] 00000000	EPFRF [R/W] 00000000	
000530H	Reserved				
000534H to 00056CH	Reserved				Reserved
000570H	ADER[R/W] 00000011 11111111		Reserved		EXT/I²C/ A/D
000574H	Reserved				Reserved
000578H	NSF[R/W] -----000 00000000		Reserved		I²C Noise filter
00057CH to 00063CH	Reserved				Reserved
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 00110X00 00000000		External bus interface
000644H	ASR1 [R/W] 00000000 XXXXXXXX		ACR1 [R/W] 00XX0X00 00X0XXXX		
000648H	ASR2 [R/W] 00000000 XXXXXXXX		ACR2 [R/W] 00XX0X00 00X0XXXX		
00064CH	ASR3 [R/W] 00000000 XXXXXXXX		ACR3 [R/W] 00XX0X00 00X0XXXX		
000650H to 00065CH	Reserved				
000660H	AWR0 [R/W] 01110000 01011011		AWR1 [R/W] 0XXX0000 0X0X1XXX		

(Continued)

Address	Register				Block
	0	1	2	3	
000664H	AWR2 [R/W] 0XXX0000 0X0X1XXX		AWR3 [R/W] 0XXX0000 0X0X1XXX		External bus interface
000668H to 00067CH	Reserved				
000680H	CSER[R/W] 00000001	Reserved			
000684H	Reserved				
000688H to 0007F8H	Reserved				Unused
0007FCH	Reserved	MODR [W] XXXXXXXX	Reserved		—
000800H to 000AFCH	Reserved				Unused
000B00H to 000FFCH	Reserved				Reserved
001000H	DMASA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
001004H	DMADA0 [R/W] 00000000 00000000 00000000 00000000				
001008H	DMASA1 [R/W] 00000000 00000000 00000000 00000000				
00100CH	DMADA1 [R/W] 00000000 00000000 00000000 00000000				
001010H	DMASA2 [R/W] 00000000 00000000 00000000 00000000				
001014H	DMADA2 [R/W] 00000000 00000000 00000000 00000000				
001018H	DMASA3 [R/W] 00000000 00000000 00000000 00000000				
00101CH	DMADA3 [R/W] 00000000 00000000 00000000 00000000				
001020H	DMASA4 [R/W] 00000000 00000000 00000000 00000000				
001024H	DMADA4 [R/W] 00000000 00000000 00000000 00000000				
001028H to 006FFCH	Reserved				Reserved

(Continued)

Address	Register				Block
	0	1	2	3	
007000_H	FLCR[R/W] 0000X000	Reserved			Flash I/F
007004_H	FLWC[R/W] 00011011	Reserved			

■ VECTOR TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer	DMAC STOP source
	Decimal	Hexadecimal					
Reset	0	00	—	$3FC_H$	$000FFFFC_H$	—	—
Mode vector	1	01	—	$3F8_H$	$000FFFF8_H$	—	—
System reserved	2	02	—	$3F4_H$	$000FFFF4_H$	—	—
System reserved	3	03	—	$3F0_H$	$000FFFF0_H$	—	—
System reserved	4	04	—	$3EC_H$	$000FFFEC_H$	—	—
System reserved	5	05	—	$3E8_H$	$000FFFE8_H$	—	—
System reserved	6	06	—	$3E4_H$	$000FFFE4_H$	—	—
Coprocessor absent trap	7	07	—	$3E0_H$	$000FFFE0_H$	—	—
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$	—	—
INTE instruction	9	09	—	$3D8_H$	$000FFFD8_H$	—	—
System reserved	10	0A	—	$3D4_H$	$000FFFD4_H$	—	—
System reserved	11	0B	—	$3D0_H$	$000FFFD0_H$	—	—
Step trace trap	12	0C	—	$3CC_H$	$000FFFCC_H$	—	—
NMI request (tool)	13	0D	—	$3C8_H$	$000FFFC8_H$	—	—
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$	—	—
System reserved	15	0F	15 (F_H) fixed	$3C0_H$	$000FFFC0_H$	—	—
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$	—	—
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	—	—
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$	—	—
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$	—	—
External interrupt 4	20	14	ICR04	$3AC_H$	$000FFFAC_H$	—	—
External interrupt 5	21	15	ICR05	$3A8_H$	$000FFFA8_H$	—	—
External interrupt 6	22	16	ICR06	$3A4_H$	$000FFFA4_H$	—	—
External interrupt 7	23	17	ICR07	$3A0_H$	$000FFFA0_H$	—	—
Reload timer 0	24	18	ICR08	$39C_H$	$000FFF9C_H$	—	—
Reload timer 1	25	19	ICR09	398_H	$000FFF98_H$	—	—
Reload timer 2	26	1A	ICR10	394_H	$000FFF94_H$	—	—
UART0 RX/I^2C status	27	1B	ICR11	390_H	$000FFF90_H$	○	STOP
UART0 TX	28	1C	ICR12	$38C_H$	$000FFF8C_H$	○	—
UART1 RX/I^2C status	29	1D	ICR13	388_H	$000FFF88_H$	○	STOP
UART1 TX	30	1E	ICR14	384_H	$000FFF84_H$	○	—
UART2 RX/I^2C status	31	1F	ICR15	380_H	$000FFF80_H$	○	STOP
UART2 TX	32	20	ICR16	$37C_H$	$000FFF7C_H$	○	—
UART3 RX/TX/I^2C status	33	21	ICR17	378_H	$000FFF78_H$	—	—

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer	DMAC STOP source
	Decimal	Hexadecimal					
UART4 RX/TX/I²C status	34	22	ICR18	374H	000FFF74H	—	—
UART5 RX/TX/I²C status	35	23	ICR19	370H	000FFF70H	—	—
UART6 RX/TX/I²C status	36	24	ICR20	36CH	000FFF6CH	—	—
UART7 RX/TX/I²C status	37	25	ICR21	368H	000FFF68H	—	—
UART8 RX/TX/I²C status	38	26	ICR22	364H	000FFF64H	—	—
UART9 RX/TX/I²C status	39	27	ICR23	360H	000FFF60H	—	—
UART10 RX/TX/I²C status	40	28	ICR24	35CH	000FFF5CH	—	—
A/D converter	41	29	ICR25	358H	000FFF58H	—	—
PPG0	42	2A	ICR26	354H	000FFF54H	○	—
PWC	43	2B	ICR27	350H	000FFF50H	—	—
HDMI-CEC/Remote controller 0, 1	44	2C	ICR28	34CH	000FFF4CH	—	—
Watch timer	45	2D	ICR29	348H	000FFF48H	—	—
Main oscillation wait	46	2E	ICR30	344H	000FFF44H	—	—
Timebase timer	47	2F	ICR31	340H	000FFF40H	—	—
Reload timer 3	48	30	ICR32	33CH	000FFF3CH	—	—
Reload timer 4	49	31	ICR33	338H	000FFF38H	—	—
Reload timer 5	50	32	ICR34	334H	000FFF34H	—	—
PPG1	51	33	ICR35	330H	000FFF30H	○	—
PPG2	52	34	ICR36	32CH	000FFF2CH	○	—
PPG3	53	35	ICR37	328H	000FFF28H	○	—
DMAC0	54	36	ICR38	324H	000FFF24H	—	—
DMAC1	55	37	ICR39	320H	000FFF20H	—	—
DMAC2	56	38	ICR40	31CH	000FFF1CH	—	—
DMAC3	57	39	ICR41	318H	000FFF18H	—	—
DMAC4	58	3A	ICR42	314H	000FFF14H	—	—
External interrupt 8 to 15	59	3B	ICR43	310H	000FFF10H	—	—
External interrupt 16 to 23	60	3C	ICR44	30CH	000FFF0CH	—	—
Multi-function timer 0, 1	61	3D	ICR45	308H	000FFF08H	—	—
Multi-function timer 2, 3	62	3E	ICR46	304H	000FFF04H	—	—
Delay interrupt	63	3F	ICR47	300H	000FFF00H	—	—
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH	—	—
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H	—	—
System reserved	66	42	—	2F4H	000FFEF4H	—	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer	DMAC STOP source
	Decimal	Hexadecimal					
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$	—	—
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$	—	—
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$	—	—
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$	—	—
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$	—	—
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$	—	—
System reserved	73	49	—	$2D8_H$	$000FFED8_H$	—	—
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$	—	—
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$	—	—
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$	—	—
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$	—	—
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$	—	—
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$	—	—
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$	—	—

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DDE} (3.3 V)	Vss – 0.5	Vss + 4.0	V	
	V_{DDI} (1.8 V)	Vss – 0.3	Vss + 2.5	V	
Analog power supply voltage*1	AV_{CC}	Vss – 0.5	Vss + 4.0	V	
	AVRH	Vss – 0.5	Vss + 4.0	V	
Input voltage*1	V_I	Vss – 0.5	V_{DDE} + 0.5	V	
		Vss – 0.5	Vss + 6.0	V	5 V tolerant pin
Analog pin input voltage*1	V_{IA}	Vss – 0.5	AVcc + 0.5	V	
Output voltage*1	V_O	Vss – 0.5	V_{DDE} + 0.5	V	
“L” level maximum output current*2	I_{OL}	—	8	mA	
“L” level average output current*3	I_{OLAV}	—	4	mA	
“L” level total maximum output current	ΣI_{OL}	—	60	mA	
“L” level total average output current*4	ΣI_{OLAV}	—	30	mA	
“H” level maximum output current*2	I_{OH}	—	– 8	mA	
“H” level average output current*3	I_{OHAV}	—	– 4	mA	
“H” level total maximum output current	ΣI_{OH}	—	– 60	mA	
“H” level total average output current*4	ΣI_{OHAV}	—	– 30	mA	
Power consumption	P_D	—	300	mW	
Storage temperature	Tstg	– 40	+ 125	°C	

*1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V

*2 : The maximum output current is the peak value for a single pin.

*3 : The average output current is the average current for a single pin over a period of 100 ms.

*4 : The total average output current is the average current for all pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(VSS = AVSS = 0.0 V)

Parameter	Symbol	Value		Unit
		Min	Max	
Operating temperature	Ta	− 40	+ 85	°C
Power supply voltage	V_{DDE} (3.3 V)	3.0	3.6	V
	V_{DDI} (1.8 V)	1.65	1.95	
Analog power supply voltage	AV_{CC}	3.0	V_{DDE}	V
5 V tolerant pin input voltage	V_I	—	V_{SS} + 5.5	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Current Consumption (upper : 1.8 V lower : 3.3 V)	I_{CCT}	—	Clock mode Ta = + 25 °C, fclk = 32 kHz	—	200	400	µA
		—		—	100	300	
	I_{CC}	—	During normal operation Ta = + 25 °C, fcp = 33 MHz, fcpp = 33 MHz	—	55	80	mA
		—		—	25	40	
	I_{CCS}	—	Main sleep mode Ta = + 25 °C, fcp = 33 MHz, fcpp = 33 MHz	—	30	50	mA
		—		—	15	30	
	I_{CCL}	—	Sub RUN mode Ta = + 25 °C, fclk = 32 kHz	—	250	450	µA
		—		—	150	400	
	I_{CCH}	—	Main Stop mode Ta = + 25 °C, fclk = 0	—	150	300	µA
		—		—	40	80	
		—	Main Stop mode Ta = + 70 °C, fclk = 0	—	400	800	µA
		—		—	100	200	
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60 to P65, PD0 to PD7, PE0, PE1, PF0 to PF7	V_{DDE} = 3.3 V	$V_{DDE} \times 0.8$	—	V_{DDE}	V
		PE2 to PE7, PC0 to PC7, P40 to P47		$V_{DDE} \times 0.7$	—	V_{DDE}	V
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60 to P65, PD0 to PD7, PE0, PE1, PF0 to PF7	V_{DDE} = 3.3 V	V_{SS}	—	$V_{DDE} \times 0.2$	V
		PE2 to PE7, PC0 to PC7, P40 to P47		V_{SS}	—	$V_{DDE} \times 0.3$	V
"H" level output voltage	V_{OH}	All port pins	V_{DDE} = 3.3 V, I_{OH} = − 4 mA	V_{DDE} − 0.5	—	V_{DDE}	V
"L" level output voltage	V_{OL}	All port pins	V_{DDE} = 3.3 V, I_{OL} = 4 mA	V_{SS}	—	0.4	V

(Continued)

(Continued)

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Input leak current	I_{IL}	Other than PD0 to PD7, PE0, PE1	—	− 5	—	+ 5	µA
		PD0 to PD7, PE0, PE1		− 10	—	+ 10	µA
Pull-up/ Pull-down resistance	R_P	Pull-up : P00 to P07, P10 to P17, P50 to P57, P60 to P65, INITX, TRSTX Pull-down : ICD0 to ICD3, IBREAK	Pull-up : V_{IL} = 0 V Pull-down : $V_{IH} = V_{DDE}$	10	33	80	kΩ
I^2C bus switch connection resistance	R_{BS}	Between P21 and P24 Between P22 and P25 Between P24 and P27 Between P25 and P30	—	—	—	130	Ω

4. AC Characteristics

(1) Clock Timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0, X1	—	10	16.5	33	MHz	PLL clock (self-oscillation 16.5 MHz doubled via PLL : internal operation at 33 MHz max.)
Sub clock frequency	fclk	X0A, X1A	—	—	32.768	—	kHz	
Internal operating clock frequency	f_{CP}	—	—	—	—	33	MHz	CPU
	f_{CPP}			—	—	33	MHz	Peripheral
	f_{CPT}			—	—	16.5	MHz	External bus

(2) Clock Output Timing

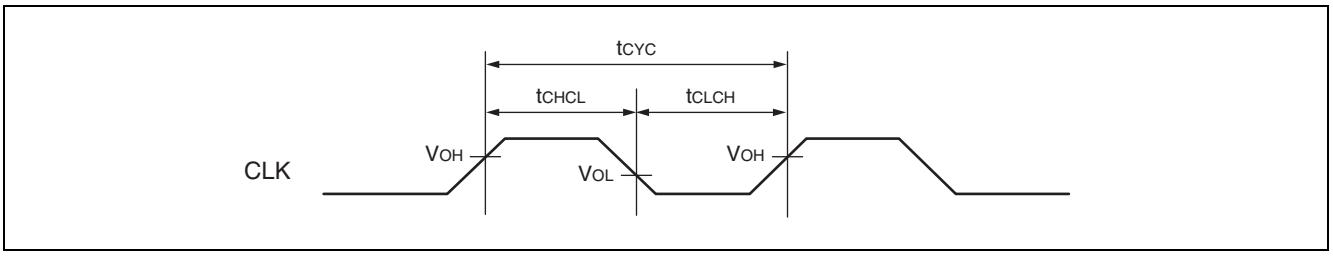
(V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	60.7	—	ns	*1
CLK ↑ → CLK ↓	t_{CHCL}	CLK		1/2 × t_{CYC} − 5	1/2 × t_{CYC} + 5	ns	*2
CLK ↓ → CLK ↑	t_{CLCH}	CLK		1/2 × t_{CYC} − 5	1/2 × t_{CYC} + 5	ns	*3

*1 : t_{CYC} is the frequency of one clock cycle after gearing.

*2 : These ratings are for the gear ratio set to × 1.
For the ratings when the gear ratio is set to between 1/2, 1/4 and 1/8, substitute 1/2, 1/4 or 1/8 for n in the following equation.
(1/2 × 1/n) × t_{CYC} − 10

*3 : These ratings are for the gear ratio set to × 1.



(3) PLL Oscillation Stabilization Wait Time

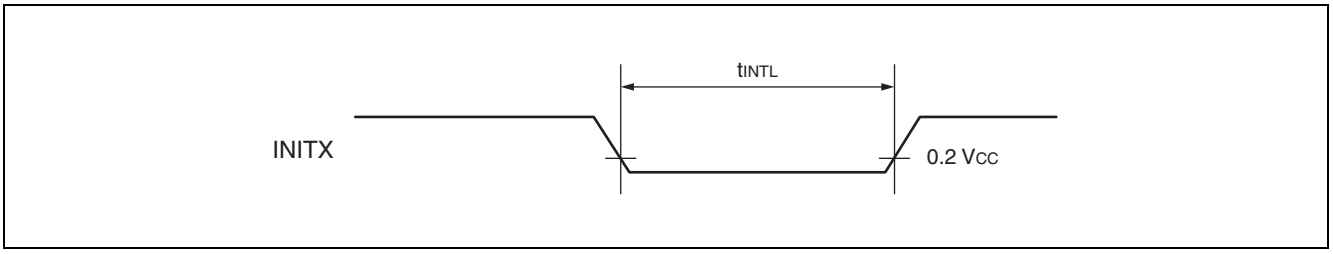
(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
PLL oscillation stabilization wait time	t_{LOCK}	600	—	µs	The length of time to wait for the PLL oscillations to stabilize.

(4) Reset Input

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	Oscillation stabilization delay time of oscillator + tcp × 10	—	µs
INITX input time (other than power-on)				tcp × 10	—	ns
INITX input time (Stop recovery time)				Oscillation stabilization delay time of oscillator + tcp × 10	—	µs



(5) Normal Access Read/Write Operation

(V_{DDE} = AV_{CC} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
CS0X to CS3X setup	t_{CSLCH}	CLK CS0X to CS3X	AWRxL : WO2 = 0	3	—	ns	*1
	t_{CSDLCH}		AWRxL : WO2 = 1	−3	—	ns	*1
CS0X to CS3X hold	t_{CHCSH}		—	3	1/2 × t_{CYC} + 6	ns	
Address setup time	t_{ASCH}	CLK AD15 to AD00		3	—	ns	
Address hold time	t_{CHAX}			3	1/2 × t_{CYC} + 6	ns	
WR0X, WR1X delay time	t_{CHWL}	CLK WR0X, WR1X		—	6	ns	
WR0X, WR1X delay time	t_{CHWH}			—	6	ns	
WR0X, WR1X minimum pulse width	t_{WLWH}	WR0X, WR1X		12	—	ns	
Data setup → WRxX ↑	t_{DSWH}	WR0X, WR1X AD15 to AD00		t_{CYC}	—	ns	
WRxX ↑ → Data hold time	t_{WHDX}			3	—	ns	
RDX delay time	t_{CHRL}	CLK RDX		—	6	ns	
RDX delay time	t_{CHRH}			—	6	ns	
RDX ↓ → Valid data input time	t_{RLDV}	RDX AD15 to AD00		—	t_{CYC} − 30	ns	*2
Data setup → RDX ↑ Time	t_{DSRH}			30	—	ns	
RDX ↑ → Data hold time	t_{RHDX}			0	—	ns	
RDX minimum pulse width	t_{RLRH}	RDX		12	—	ns	
ASX setup	t_{ASLCH}	CLK ASX		3	—	ns	
ASX hold	t_{ASHCH}			3	1/2 × t_{CYC} + 6	ns	

*1 : AWRxL : Area Wait Register

*2 : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.

(6) Multiplexed Bus Access Read/Write Operation

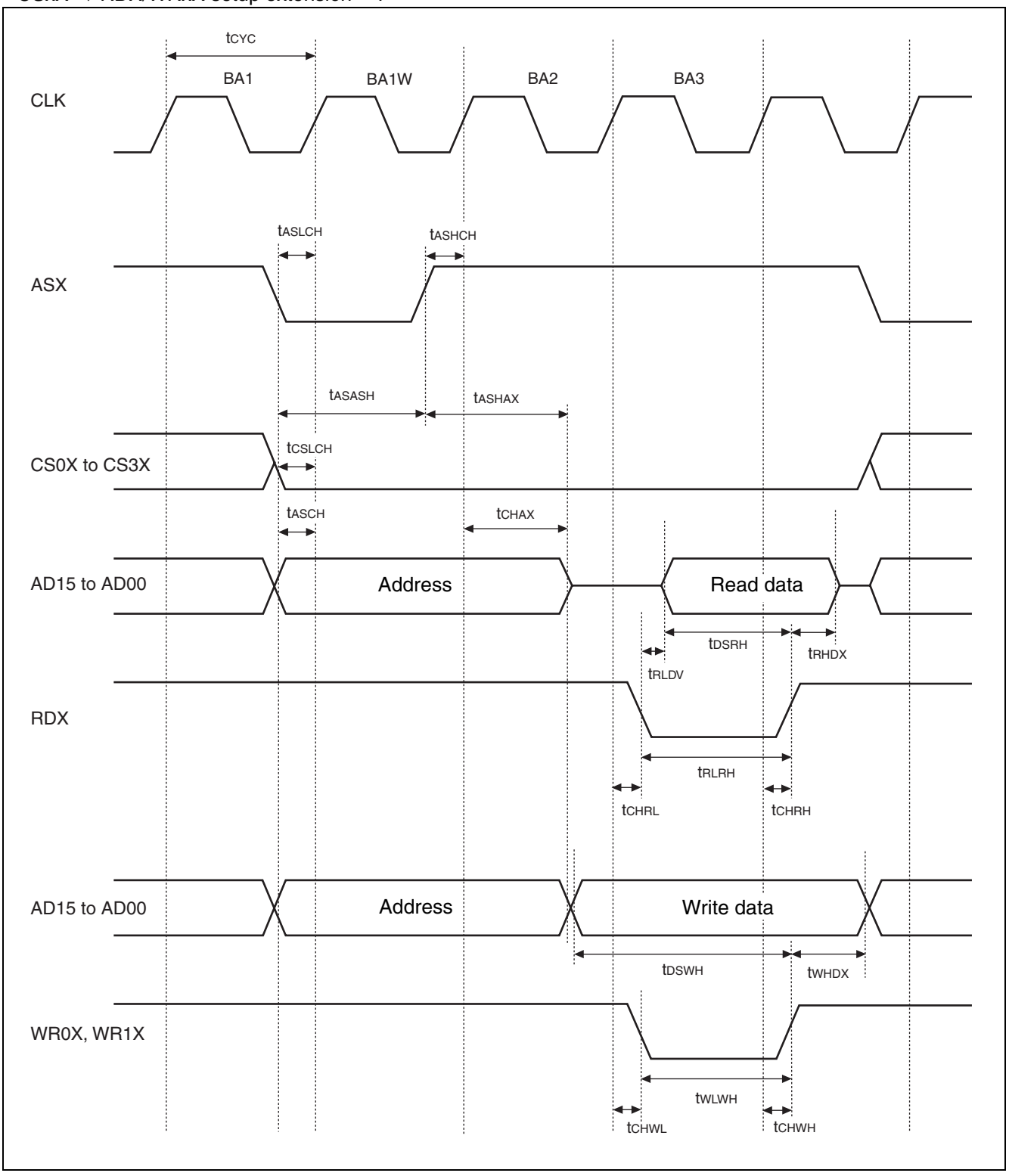
(V_{DDE} = 3.3 ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
AD15 to AD00 address setup time → CLK ↑	t_{ASCH}	CLK AD15 to AD00	—	3	—	ns	
CLK ↑→ AD15 to AD00 address setup time	t_{CHAX}			3	1/2 × t_{CYC} + 6	ns	
AD15 to AD00 address setup time → ASX ↑	t_{ASASH}	ASX AD15 to AD00		12	—	ns	*
ASX ↑→ AD15 to AD00 address setup time	t_{ASHAX}			t_{CYC} – 3	t_{CYC} + 3	ns	*

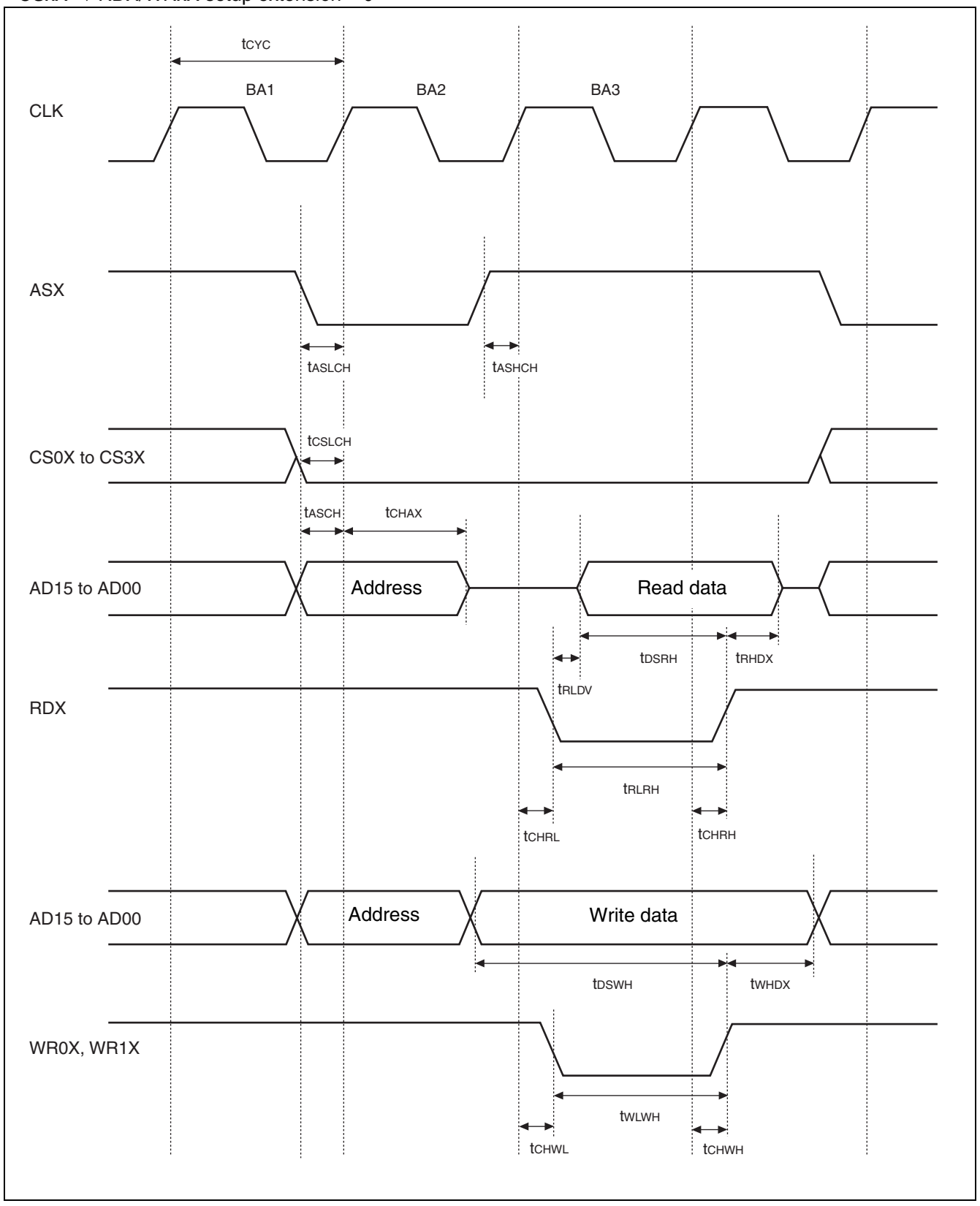
* : CSxX → RDX/WRxX setup extension = 1

Note : Use the same rating as normal bus interface except for this rating.

• CSxX → RDX/WRxX setup extension = 1



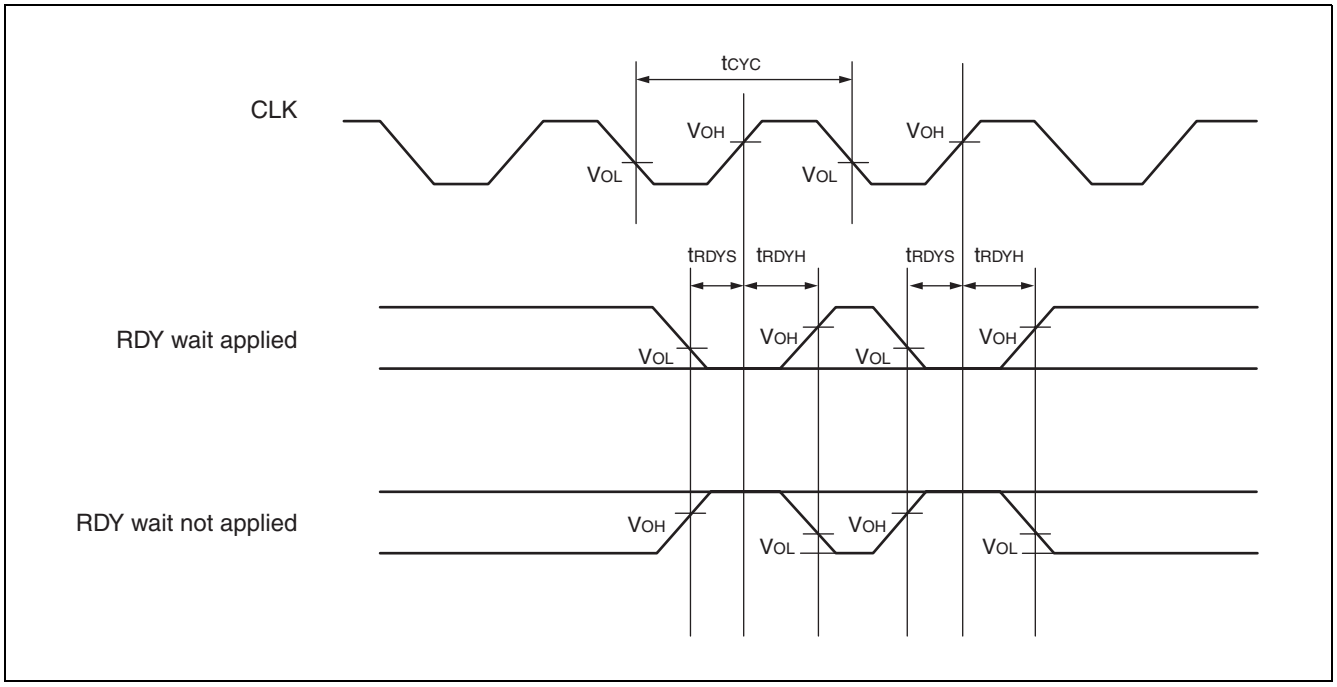
• CSxX → RDX/WRxX setup extension = 0



(7) Ready Input Timings

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
RDY setup time → CLK ↓	t_{RDYS}	CLK, RDY	—	25	—	ns
CLK ↓ → RDY hold time	t_{RDYH}	CLK, RDY	—	0	—	ns



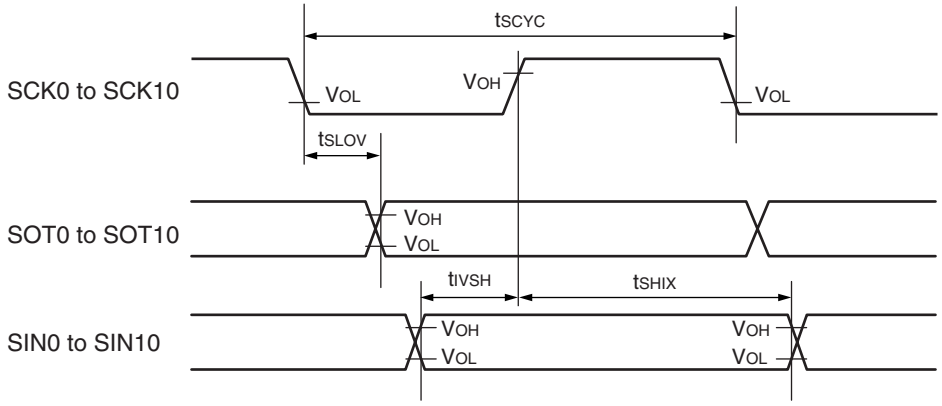
(8) UART timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

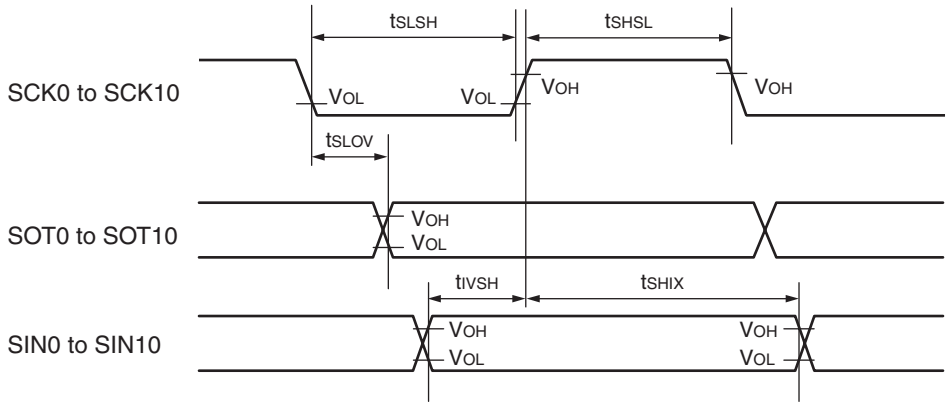
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK10	Internal shift clock operation	4 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK10 SOT0 to SOT10		– 20	+ 20	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK10 SIN0 to SIN10		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK10 SIN0 to SIN10		20	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK10	External shift clock operation	2 t_{CYCP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK10		2 t_{CYCP}	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK10 SOT0 to SOT10		—	30	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK10 SIN0 to SIN10		20	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK10 SIN0 to SIN10		20	—	ns

Notes : • The above standards apply to the CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.

• Internal shift clock mode



• External shift clock mode

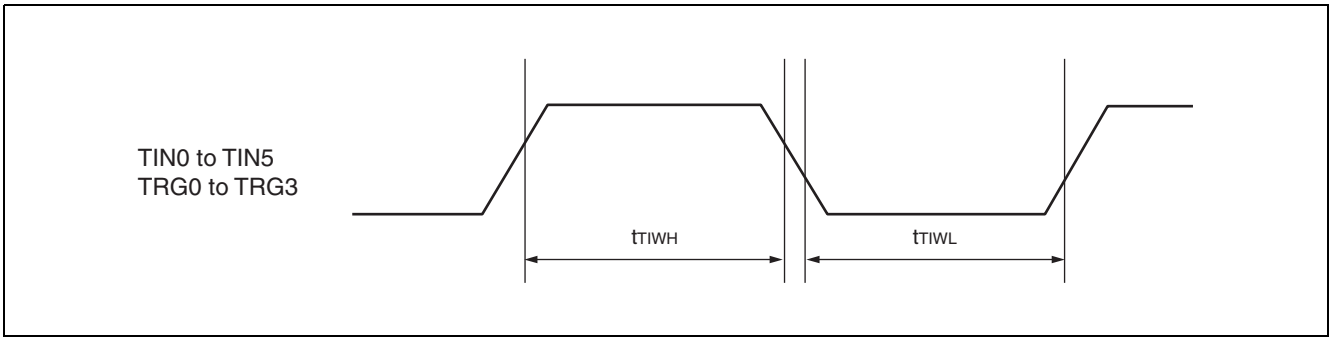


(9) Reload timer clock, PPG timer input, multi-function timer input timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN5 TRG0 to TRG3	—	2 t_{CYCP}	—	ns

Note : t_{CYCP} is the cycle time of the peripheral clock.

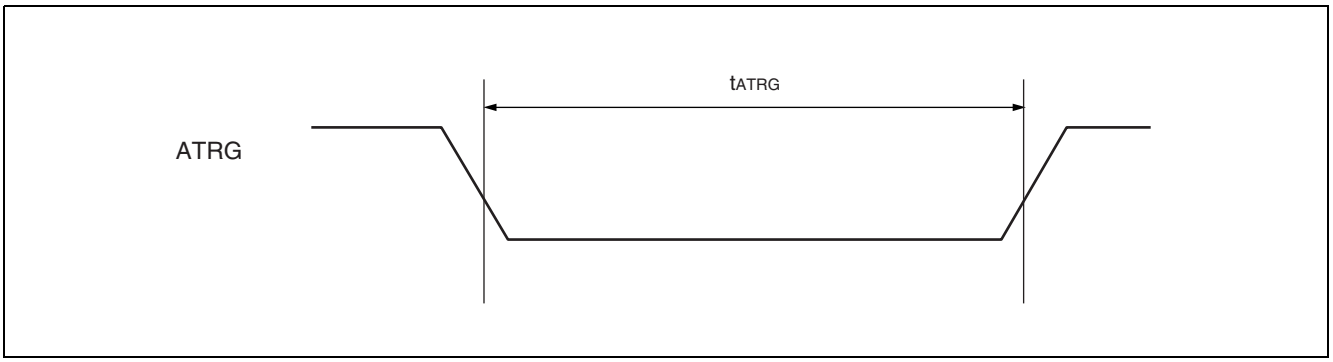


(10) Trigger Input Timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
A/D activation trigger input time	t_{ATRG}	ATRG	—	5 t_{CYCP}	—	ns

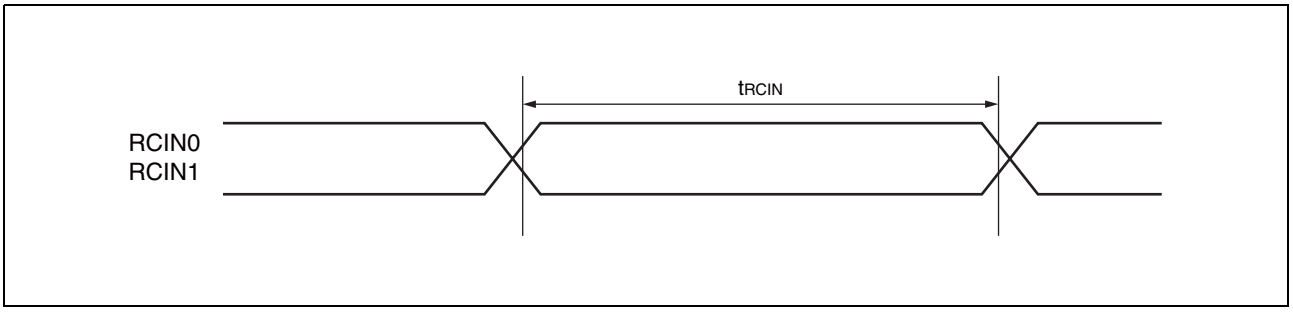
Note : t_{CYCP} is the cycle time of the peripheral clock.



(11) Remote control signal input timing

(V_{DDE} = 3.3 V + 0.3 V, V_{DDI} = 1.8 V + 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Parameter
				Min	Max		
Remote control input pulse width	t_{RCIN}	RCIN0 RCIN1	At 32.768 kHz	62	—	µs	Count 2 clocks or more



(12) I²C timing

- When operating in master mode

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*1		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 kΩ, C = 50 pF*2	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	—	1.3	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}		—	5 × M*3	—	5 × M*3	ns	
"Repeated START condition" setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs	
"Repeated START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs	The first clock pulse is generated after this.
"STOP condition" setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs	
SDA data input hold time (vs. SCL ↓)	t_{HDDAT}		2 × M*3	—	2 × M*3	—	µs	
SDA data input setup time (vs. SCL ↑)	t_{SUDAT}		250	—	100*4	—	ns	

*1 : For use at over 100 kHz, set the resource clock to 6 MHz or higher.

*2 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

*3 : M = Resource clock cycle (ns)

*4 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".
When a device does not extend the "L" period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) from when the SCL line is released.

• When operating in slave mode

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*1		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 kΩ, C = 50 pF*2	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	—	1.3	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}		—	5 × M*3	—	5 × M*3	ns	
"Repeated START condition" setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs	
"Repeated START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs	The first clock pulse is generated after this.
"STOP condition" setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs	
SDA data input hold time (vs. SCL ↓)	t_{HDDAT}		2 × M*3	—	2 × M*3	—	µs	
SDA data input setup time (vs. SCL↑)	t_{SUDAT}		250	—	100*4	—	ns	

*1 : For use at over 100 kHz, set the resource clock to 6 MHz or higher.

*2 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

*3 : M = Resource clock cycle (ns)

*4 : A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".
When a device does not extend the "L" period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) from when the SCL line is released.

5. Electrical Characteristics for the A/D Converter

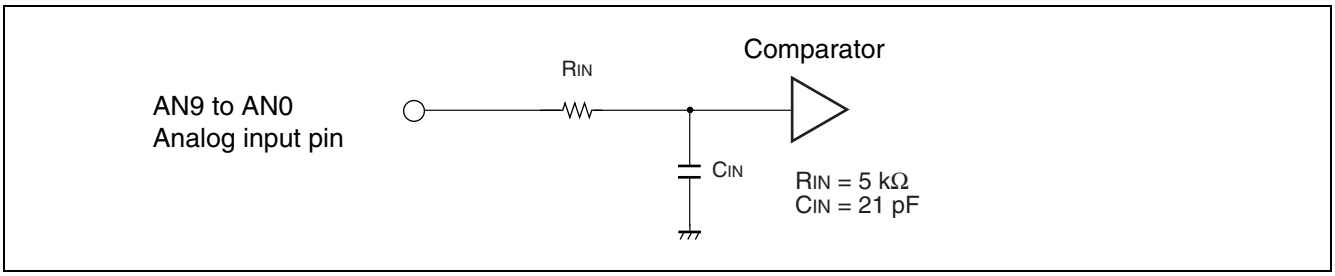
(1) Electrical Characteristics

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = –40 °C to + 85 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	—	—	± 5.5	LSB	AVcc = 3.3 V, AVRH = 3.3 V (CPU sleep)
Nonlinear error*1	—	—	± 3.5	LSB	
Differential linear error*1	—	—	± 2.0	LSB	
Zero transition voltage*1	– 4.0	—	+ 6.0	LSB	
Full transition voltage*1	AVRH – 5.5	—	AVRH + 3.0	LSB	
Conversion time	7.94*2	—	—	µs	
Power supply current (analog + digital)	—	—	3	mA	
Reference power supply current (between AVRH and AVSS)	—	—	100	µA	AVRH = 3.0 V, AV_{SS} = 0.0 V
Analog input capacitance	—	—	21	pF	
Interchannel disparity	—	—	4	LSB	

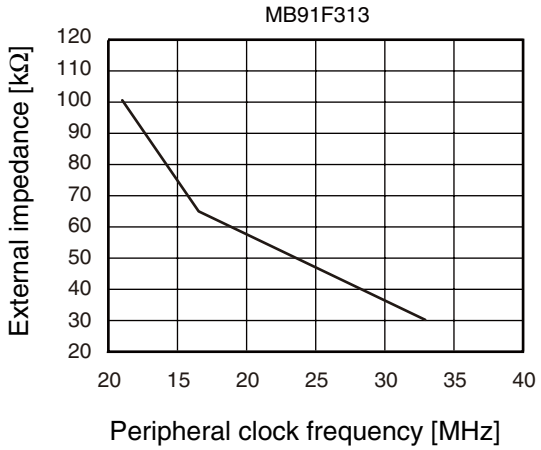
*1 : Measured in the CPU sleep state

*2 : Depending on the clock cycle supplied to peripheral resources

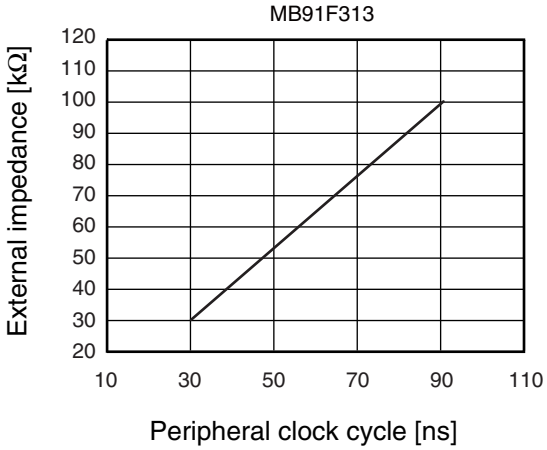


- The relationship between peripheral clock and external impedance

(Peripheral clock frequency and external impedance)

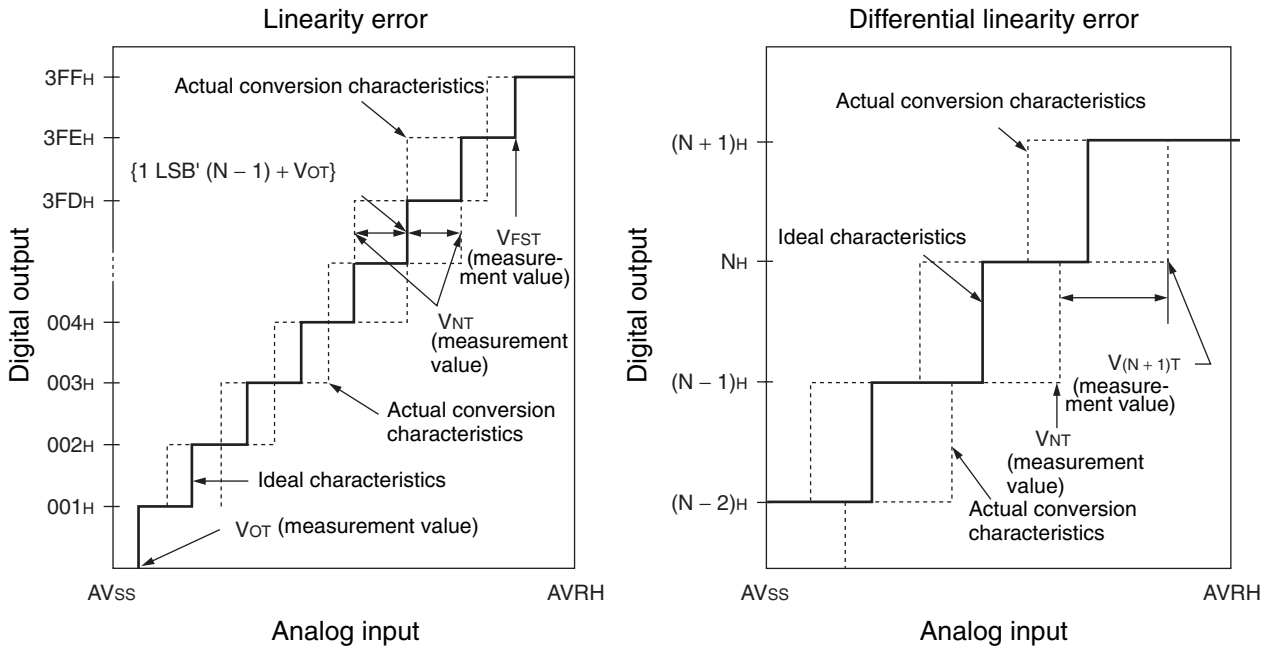


(Peripheral clock cycle and external impedance)



(2) Definition of terms

Resolution	: Analog variation that is recognized by an A/D converter.
Linearity error	: The deviation between the actual conversion characteristics and a straight line connecting the device's zero transition point ("00 0000 0000$_B$" ⟷ "00 0000 0001$_B$") and full scale transition point ("11 1111 1110$_B$" ⟷ "11 1111 1111$_B$").
Differential linear error	: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
Total error	: This error indicates the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + V_{OT}\}}{1\ LSB'}\ [LSB]$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB'} - 1[LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

N : A/D converter digital output value
V_{OT} : The voltage at which digital output changes from (000)$_H$ to (001)$_H$
V_{FST} : The voltage at which digital output changes from (3FE)$_H$ to (3FF)$_H$
V_{NT} : The voltage at which digital output changes from (N + 1)$_H$ to N_H

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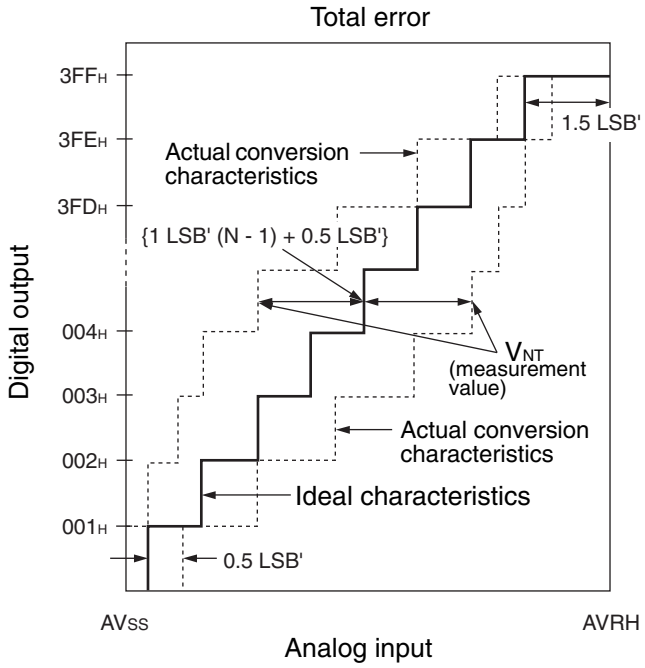


$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}}{1024} [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{NT} : The voltage at which digital output changes from $(N + 1)_H$ to N_H
V_{OT}' (ideal value) = AV_{SS} + 0.5 LSB' [V]
V_{FST}' (ideal value) = AVRH – 1.5 LSB' [V]

6. Flash Memory Write/Erase Characteristics

(V_{DDE} = 3.3 V, V_{DDI} = 1.8 V, Ta = + 25 °C)

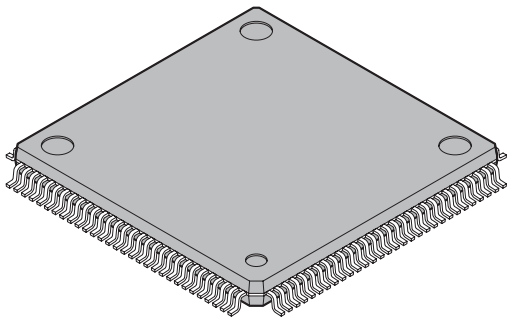
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.9	3.6	s	Excludes internal programming prior erasure.
Word write time	—	23	370	µs	Excludes system-level overhead.
Chip write time	—	6.2	102	s	Excludes system-level overhead.
Erase/write cycle	10000	—	—	cycle	
Data retention time	20*	—	—	year	Average Ta = + 85 °C

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

■ ORDERING INFORMATION

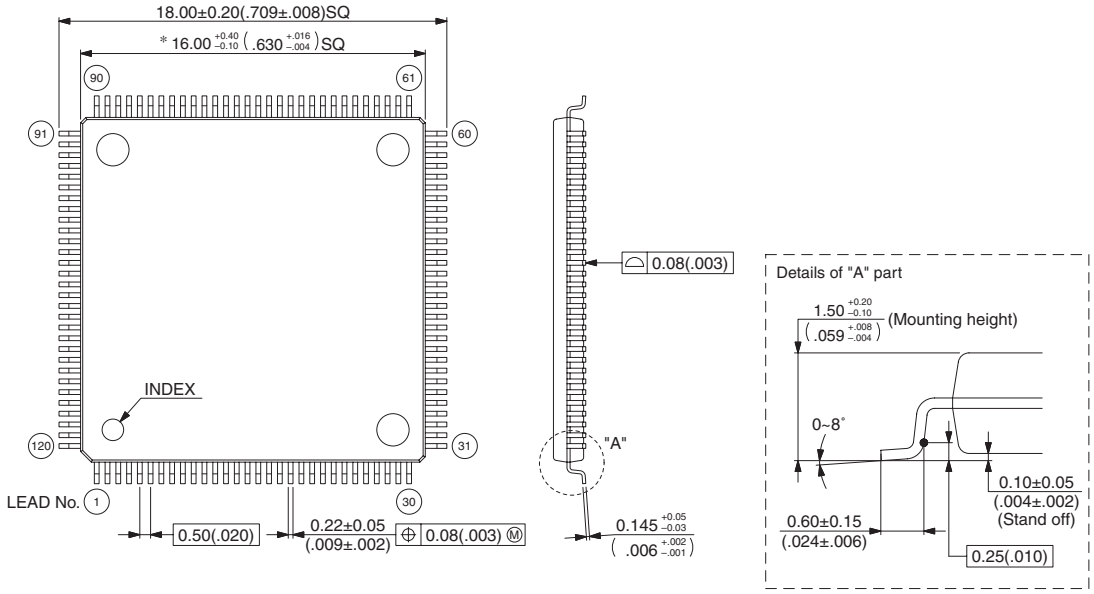
Part number	Package
MB91F313PMC-GE1	120-pin plastic LQFP (FPT-120P-M21)

■ PACKAGE DIMENSION

120-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
(FPT-120P-M21)	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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