FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16705-1E

32-bit Proprietary Microcontrollers

CMOS

FR60 MB91319R Series

MB91316/316A/F318R/F318S/FV319R

■ DESCRIPTION

The MB91319R series is the microcontrollers which use a high-performance 32-bit RISC-CPU and contains various types of I/O resources for the embedded control that requires high-performance and high-speed CPU processing.

It is suitable for the embedded control in TV or PDP, requiring high-performance CPU processing power.

This product is one of the FR60* family based on the FR30/40 family CPU with enhanced bus access. It is applicable to faster-speed application.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURE

- FR CPU
  - 32-bit RISC, load/store architecture with a five-stage pipeline
  - Operating frequency : 40 MHz (Use of PLL : Oscillation 10 MHz)
  - 16-bit fixed length instructions (basic instructions) , 1 instruction per cycle
  - Embedded application optimized instructions : Memory-to-memory transfer, bit processing, barrel shift, and other instructions.
  - High-level language support instructions : Function entry/exit instructions, multiple register load/store instructions.
  - Register interlock functions: Facilitating coding in assemblers
  - Built-in multiplier with instruction-level support
    32-bit multiplication with sign : 5 cycles
    16-bit multiplication with sign : 3 cycles

(Continued)

Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function implemented by a four-word queue in the CPU
- Instruction compatible with FR family

• Bus interface

This bus interface is used for internal macro IF (USB, OSDC)
- $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ areas are connected as following :
  $\overline{CS1}$ area : Reserved, $\overline{CS2}$ area : USB function, $\overline{CS3}$ area : OSDC

• Built-in memory

Memory	MB91FV319R	MB91F318R/F318S	MB91316/316A
RAM	48 Kbytes	48 Kbytes	32 Kbytes
Memory for program	Flash memory : 1 Mbyte	Flash memory : 1 Mbyte	MASK ROM : 512 Kbytes
Memory for font	Flash memory : 512 Kbytes	MASK ROM : 384 Kbytes	MASK ROM : 384 Kbytes

• DMAC (DMA Controller)
- 5 channels (ch.0 and ch.1 are connected to USB function.)
- Two transfer sources (internal peripherals/software)
- Specifying of addressing mode 32-bit full address (increased/decreased/fixed)
- Transfer modes (demand transfer, burst transfer, step transfer, block transfer)
- Selectable transfer data size : 8, 16, or 32-bits

• Bit search module (for REALOS)
- Search for the position of the bit “1”/“0”-changed first in one word from the MSB

• Reload timer (including a channel for REALOS)
- 16-bit timer: 3 channels
- The internal clock is selectable from 2/8/32 divisions.

• UART
- Full-duplex double buffer
- 5 channels
- Selectable parity ON/OFF
- Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable
- Built-in timer for dedicated baud rate
- External clock can be used as transfer clock.
- Assorted error detection functions (for parity, frame, and overrun errors)

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- I²C Interface *
  - 4 channels (built-in bridge function)
  - Master/slave sending and receiving
  - Clock synchronization function
  - Detecting transmitting direction function
  - Bus error detection function
  - Standard mode (Max 100 kbps) /High speed mode (Max 400 kbps) supported
  - Built-in FIFO function with 16-byte data each for transmit/receive
  - Arbitration function
  - Slave address and general call address detection function
  - Start condition repeated generation and detection
  - 10-bit/7-bit slave address

- Interrupt controller
  - Total of external interrupt pin is 5. (one non-maskable interrupt pin ($\overline{\text{NMI}}$) and four normal interrupt pins (INT3 to INT0))
  - Interrupt from internal peripheral
  - Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt
  - At the STOP, available use for Wake Up

- A/D converter
  - 10-bit resolution, 10 channels
  - Successive approximation type converter. Conversion time: Approx. 10 µs
  - Conversion modes (one-shot conversion mode, scanning conversion mode)
  - Activation trigger (software / external trigger)

- PPG
  - 4 channels are incorporated.
  - 16-bit down counter, 16-bit data register with buffer for setting cycles
  - The internal clock is selectable from 1/4/16/64 divisions.

- PWC
  - 1 channel (1 input) is incorporated.
  - 16-bit up counter
  - Easy digital low pass filter

- Multi function timer
  - 4 channels are incorporated.
  - Low pass filter eliminating noise below the clock setting
  - Capable of pulse width measurement according to fine settings using seven types of clock signals
  - Event count function from pin input
  - Interval timer function using seven kinds of clock and external input clock

- USB function
  - Full speed • double buffer of USB2.0 version
  - CONTROL IN/OUT, BULK IN/OUT, INTERRUPT IN

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- OSDC function
  - RGB: each 3 bits (16 colors available among 512 colors)
  - Analog RGB output: Max 50 MHz
  - Digital RGB output: Max 90 MHz
  - A font in 24 × 32 dots can be displayed up to 80 × 32.
  - Two-layered display of MAIN/CC (Font in CC layer is fixed at 18 dots in horizontal axis)
  - 4096 characters at the maximum (including 16 characters for font RAM)

- Closed caption decoder function
  - 2 channels are incorporated.
  - CC decode function
  - ID-1 (480i/480p) decode function

- PLL for video clock
  - 3 PLLs generating dot clock and VBI clock

- Other interval timer
  - 16-bit timer : 3 channels
  - Watchdog timer

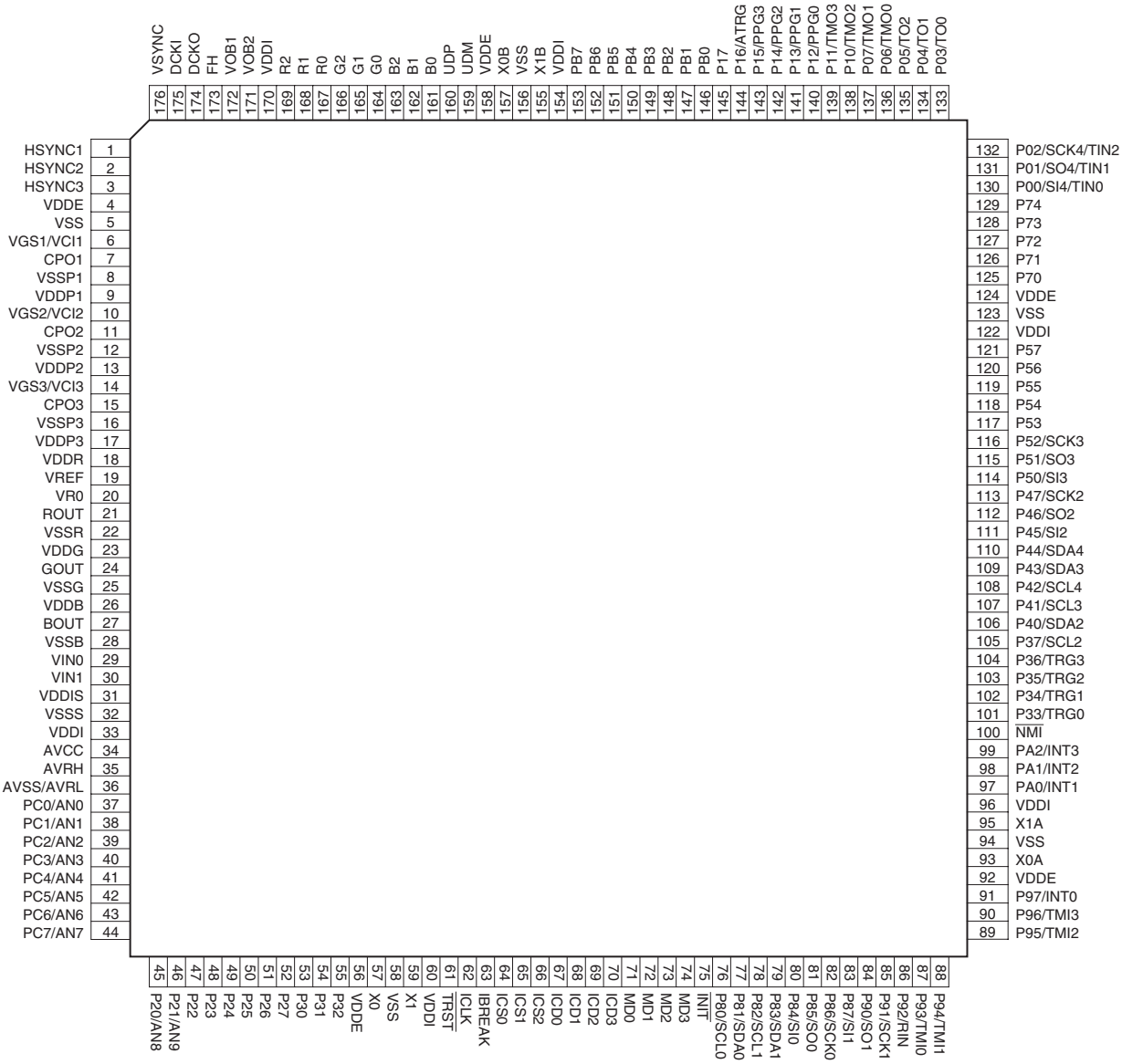
- I/O port
  - Max 88 ports

- Other features
  - Built-in oscillation circuit as clock source
  - $\overline{\text{INIT}}$ is prepared as a reset pin.
  - Watchdog timer reset and software reset are also available.
  - Stop mode and sleep mode are supported as low-power consumption mode.
  - Gear function
  - Built-in time-base timer
  - Package : LQFP-176, 0.5mm pitch, 24 mm × 24 mm
  - CMOS technology : 0.18 μm
  - Power supply voltage : 3.3 V ± 0.3 V, 1.8 V ± 0.15 V 2-power supply

* : “Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.”

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-176P-M07)

■ PIN DESCRIPTION

Pin No.	Pin Name	I/O Circuit type*	Function
1	HSYNC1	G	Vertical synchronous input 1
2	HSYNC2	G	Vertical synchronous input 2
3	HSYNC3	G	Vertical synchronous input 3
4	VDDE	—	I/O power supply
5	VSS	—	Ground
6	VGS1/VCI1	—	Guard band ground
7	CPO1	K	Charge pump output
8	VSSP1	—	Dot clock PLL ground
9	VDDP1	—	Dot clock PLL power supply
10	VGS2/VCI2	—	Guard band ground
11	CPO2	K	Charge pump output
12	VSSP2	—	Dot clock PLL ground
13	VDDP2	—	Dot clock PLL power supply
14	VGS3/VCI3	—	Guard band ground
15	CPO3	K	Charge pump output
16	VSSP3	—	Dot clock PLL ground
17	VDDP3	—	Dot clock PLL power supply
18	VDDR	—	D/A power supply for R
19	VREF	K	Power supply reference input
20	VR0	K	Resistor connection pin
21	ROUT	K	R output (analog)
22	VSSR	—	D/A ground for R
23	VDDG	—	D/A power supply for G
24	GOUT	K	G output (analog)
25	VSSG	—	D/A ground for G
26	VDDB	—	D/A power supply for B
27	BOUT	K	B output (analog)
28	VSSB	—	D/A ground for B
29	VIN0	K	Data slicer input 0
30	VIN1	K	Data slicer input 1
31	VDDIS	—	Data slicer power supply
32	VSSS	—	Data slicer ground
33	VDDI	—	Internal logic power supply
34	AVCC	—	A/D power supply
35	AVRH	—	A/D reference power supply

(Continued)

Pin No.	Pin Name	I/O Circuit type*	Function
36	AVSS/AVRL	—	A/D ground
37	PC0	E	General-purpose port
	AN0		Analog input
38	PC1	E	General-purpose port
	AN1		Analog input
39	PC2	E	General-purpose port
	AN2		Analog input
40	PC3	E	General-purpose port
	AN3		Analog input
41	PC4	E	General-purpose port
	AN4		Analog input
42	PC5	E	General-purpose port
	AN5		Analog input
43	PC6	E	General-purpose port
	AN6		Analog input
44	PC7	E	General-purpose port
	AN7		Analog input
45	P20	E	General-purpose port
	AN8		Analog input
46	P21	E	General-purpose port
	AN9		Analog input
47	P22	C	General-purpose port
48	P23	C	General-purpose port
49	P24	C	General-purpose port
50	P25	C	General-purpose port
51	P26	C	General-purpose port
52	P27	C	General-purpose port
53	P30	C	General-purpose port
54	P31	C	General-purpose port
55	P32	C	General-purpose port
56	VDDE	—	3.3 V power supply
57	X0	A	10 MHz oscillation pin
58	VSS	—	Ground
59	X1	A	10 MHz oscillation pin
60	VDDI	—	Internal logic power supply

(Continued)

Pin No.	Pin Name	I/O Circuit type*	Function
61	$\overline{\text{TRST}}$	B	DSU tool reset (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
62	ICLK	M	DSU clock (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
63	IBREAK	L	DSU break (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
64	ICS0	O	DSU status (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
65	ICS1	O	DSU status (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
66	ICS2	O	DSU status (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
67	ICD0	P	DSU data (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
68	ICD1	P	DSU data (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
69	ICD2	P	DSU data (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
70	ICD3	P	DSU data (In MB91F318R/F318S, this pin is the open pin so do not connect with other pins.)
71	MD0	F	Mode pin
72	MD1	F	Mode pin
73	MD2	F	Mode pin
74	MD3	L	Mode pin
75	$\overline{\text{INIT}}$	B	Initial (reset) pin
76	P80	J	General-purpose port
	SCL0		I^2C clock pin
77	P81	J	General-purpose port
	SDA0		I^2C data pin
78	P82	J	General-purpose port
	SCL1		I^2C clock pin
79	P83	J	General-purpose port
	SDA1		I^2C data pin
80	P84	C	General-purpose port
	SI0		UART0 serial input
81	P85	C	General-purpose port
	SO0		UART0 serial output

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Pin No.	Pin Name	I/O Circuit type*	Function
82	P86	C	General-purpose port
	SCK0		UART0 clock input/output
83	P87	C	General-purpose port
	SI1		UART1 serial input
84	P90	C	General-purpose port
	SO1		UART1 serial output
85	P91	C	General-purpose port
	SCK1		UART1 clock input/output
86	P92	C	General-purpose port
	RIN		PWC input
87	P93	C	General-purpose port
	TMI0		Multi-functional timer 0 input
88	P94	C	General-purpose port
	TMI1		Multi-functional timer 1 input
89	P95	C	General-purpose port
	TMI2		Multi-functional timer 2 input
90	P96	C	General-purpose port
	TMI3		Multi-functional timer 3 input
91	P97	O	General-purpose port
	INT0		External interrupt input 0
92	VDDE	—	3.3 V power supply
93	X0A	A	32 kHz oscillation pin
94	VSS	—	Ground
95	X1A	A	32 kHz oscillation pin
96	VDDI	—	Internal logic power supply
97	PA0	O	General-purpose port
	INT1		External interrupt input 1
98	PA1	O	General-purpose port
	INT2		External interrupt input 2
99	PA2	O	General-purpose port
	INT3		External interrupt input 3
100	$\overline{\text{NMI}}$	B	$\overline{\text{NMI}}$ input
101	P33	C	General-purpose port
	TRG0		PPG0 trigger input

(Continued)

Pin No.	Pin Name	I/O Circuit type*	Function
102	P34	C	General-purpose port
	TRG1		PPG1 trigger input
103	P35	C	General-purpose port
	TRG2		PPG2 trigger input
104	P36	C	General-purpose port
	TRG3		PPG3 trigger input
105	P37	N	General-purpose port
	SCL2		I²C clock pin
106	P40	N	General-purpose port
	SDA2		I²C data pin
107	P41	N	General-purpose port
	SCL3		I²C clock pin
108	P42	N	General-purpose port
	SCL4		I²C clock pin
109	P43	N	General-purpose port
	SDA3		I²C data pin
110	P44	N	General-purpose port
	SDA4		I²C data pin
111	P45	C	General-purpose port
	SI2		UART2 serial input
112	P46	C	General-purpose port
	SO2		UART2 serial output
113	P47	C	General-purpose port
	SCK2		UART2 clock output
114	P50	C	General-purpose port
	SI3		UART3 serial input
115	P51	C	General-purpose port
	SO3		UART3 serial output
116	P52	C	General-purpose port
	SCK3		UART3 clock output
117	P53	C	General-purpose port
118	P54	C	General-purpose port
119	P55	C	General-purpose port
120	P56	C	General-purpose port
121	P57	C	General-purpose port

(Continued)

Pin No.	Pin Name	I/O Circuit type*	Function
122	VDDI	—	Internal logic power supply
123	VSS	—	Ground
124	VDDE	—	3.3 V power supply
125	P70	C	General-purpose port
126	P71	C	General-purpose port
127	P72	C	General-purpose port
128	P73	C	General-purpose port
129	P74	C	General-purpose port
130	P00	C	General-purpose port
	SI4		UART4 serial input
	TIN0		Reload timer 0 trigger input
131	P01	C	General-purpose port
	SO4		UART4 serial output
	TIN1		Reload timer 1 trigger input
132	P02	C	General-purpose port
	SCK4		UART4 clock input
	TIN2		Reload timer 2 trigger input
133	P03	C	General-purpose port
	TO0		Reload timer 0 output
134	P04	C	General-purpose port
	TO1		Reload timer 1 output
135	P05	C	General-purpose port
	TO2		Reload timer 2 output
136	P06	C	General-purpose port
	TMO0		Multi-functional timer 0 output
137	P07	C	General-purpose port
	TMO1		Multi-functional timer 1 output
138	P10	C	General-purpose port
	TMO2		Multi-functional timer 2 output
139	P11	C	General-purpose port
	TMO3		Multi-functional timer 3 output
140	P12	C	General-purpose port
	PPG0		PPG0 output
141	P13	C	General-purpose port
	PPG1		PPG1 output

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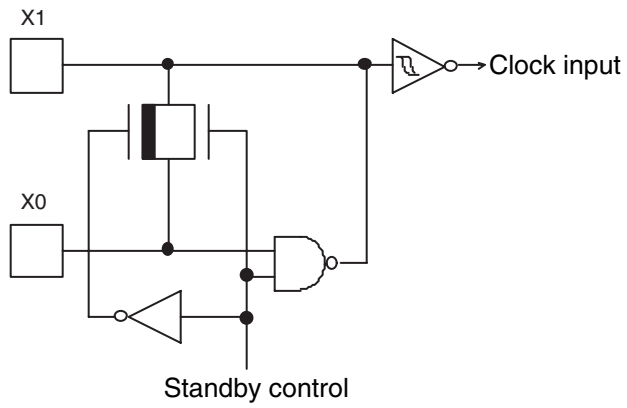
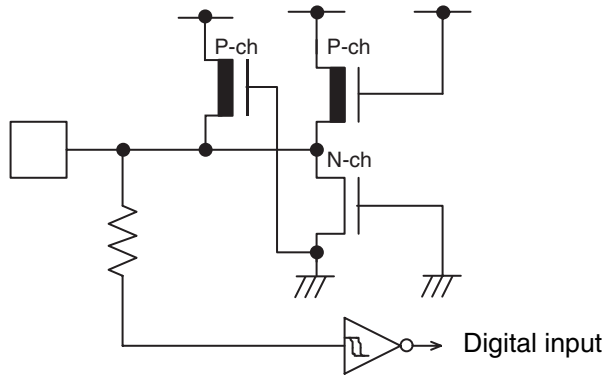
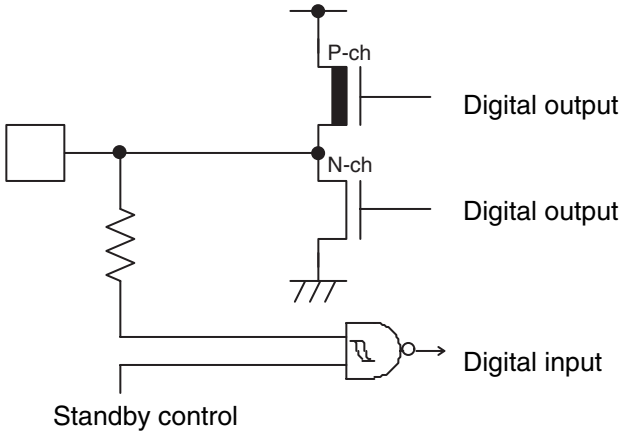
Pin No.	Pin Name	I/O Circuit type*	Function
142	P14	C	General-purpose port
	PPG2		PPG2 output
143	P15	C	General-purpose port
	PPG3		PPG3 output
144	P16	C	General-purpose port
	ATRG		A/D conversion trigger input
145	P17	C	General-purpose port
146	PB0	C	General-purpose port
147	PB1	C	General-purpose port
148	PB2	I	General-purpose port
149	PB3	C	General-purpose port
150	PB4	C	General-purpose port
151	PB5	C	General-purpose port
152	PB6	H	General-purpose port
153	PB7	C	General-purpose port
154	VDDI	—	Internal power supply
155	X1B	A	48 MHz oscillation pin
156	VSS	—	Ground
157	X0B	A	48 MHz oscillation pin
158	VDDE	—	3.3 V power supply
159	UDM	USB	USB function
160	UDP		USB function
161	B0	D	RGB digital output
162	B1	D	RGB digital output
163	B2	D	RGB digital output
164	G0	D	RGB digital output
165	G1	D	RGB digital output
166	G2	D	RGB digital output
167	R0	D	RGB digital output
168	R1	D	RGB digital output
169	R2	D	RGB digital output
170	VDDI	—	Internal logic power supply
171	VOB2	D	Translucent color period output
172	VOB1	D	OSD display period output
173	FH	D	Horizontal synchronous output
174	DCKO	D	Dot clock output
175	DCKI	G	Dot clock input
176	VSYNC	G	Vertical synchronous output

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		• Oscillation circuit • Feedback resistance X0 : 1 MΩ X0A : 10 MΩ
B		• CMOS level hysteresis input • With pull-up resistor
C		• CMOS level output • CMOS level hysteresis input • With standby control

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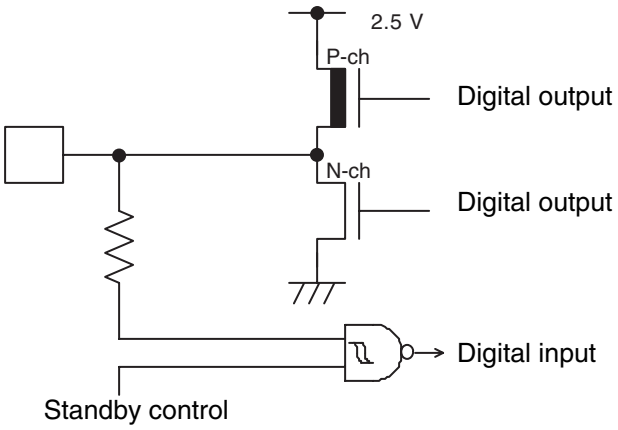
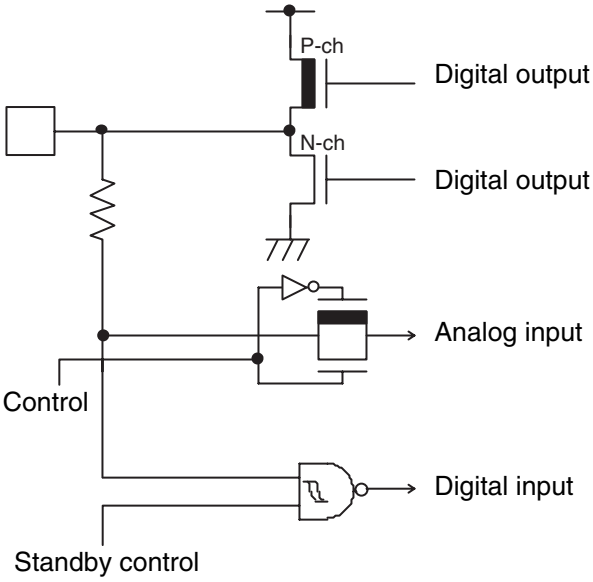
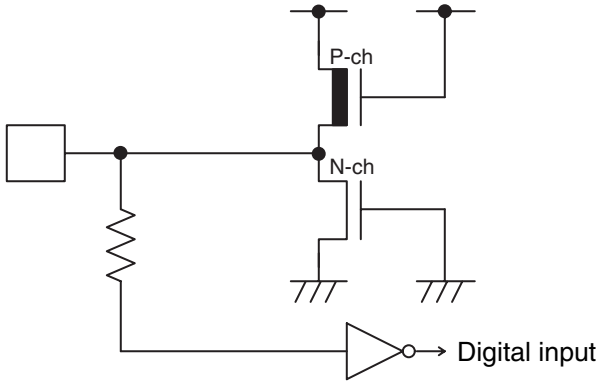
Type	Circuit type	Remarks
D		• 2.5 V CMOS level output • CMOS level hysteresis input • With standby control
E		• CMOS level output • CMOS level hysteresis input • With standby control • With analog input switch
F		• CMOS level input • Without standby control

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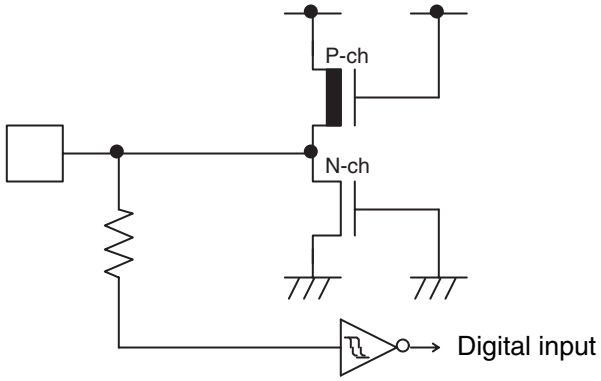
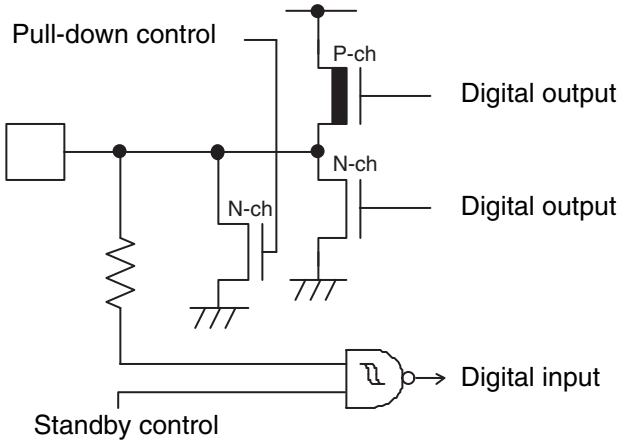
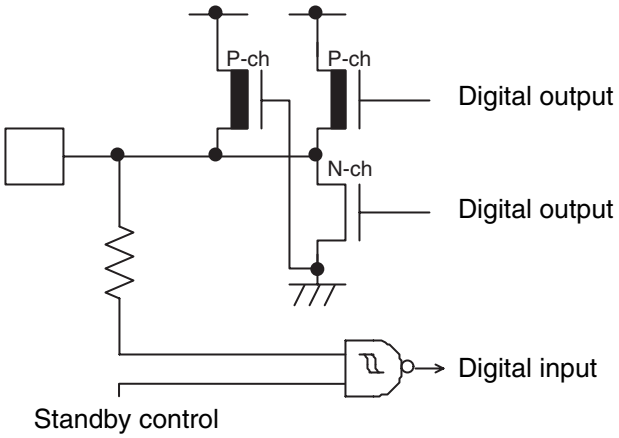
Type	Circuit type	Remarks
G		• CMOS level hysteresis input • Without standby control
H		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-down resistor
I		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up resistor

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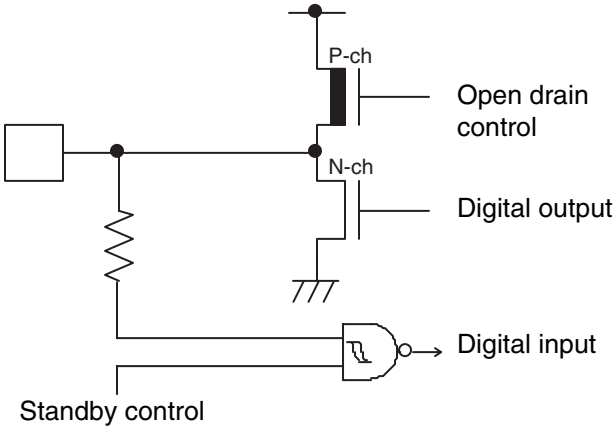
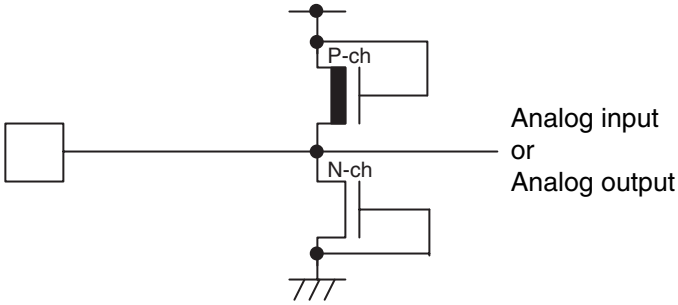
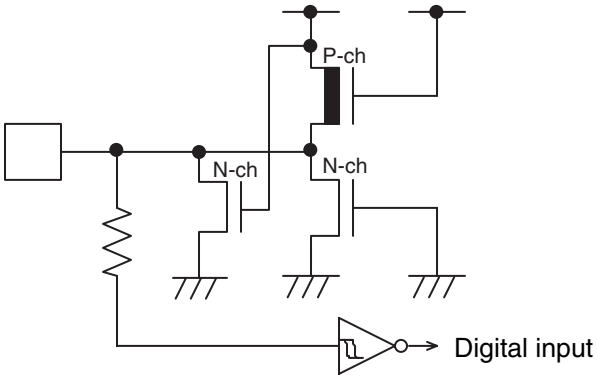
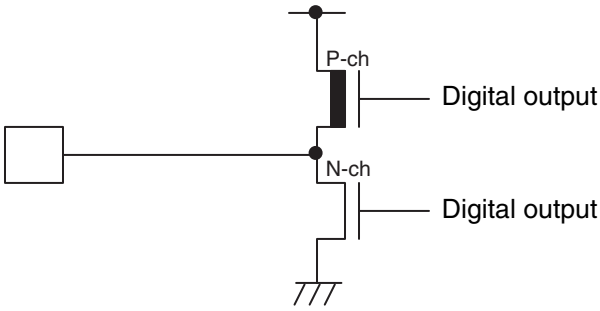
Type	Circuit type	Remarks
J		• Open drain output • CMOS level hysteresis input • With standby control
K		Analog pin
L		• CMOS level hysteresis input • With pull-down resistor
M		CMOS level output

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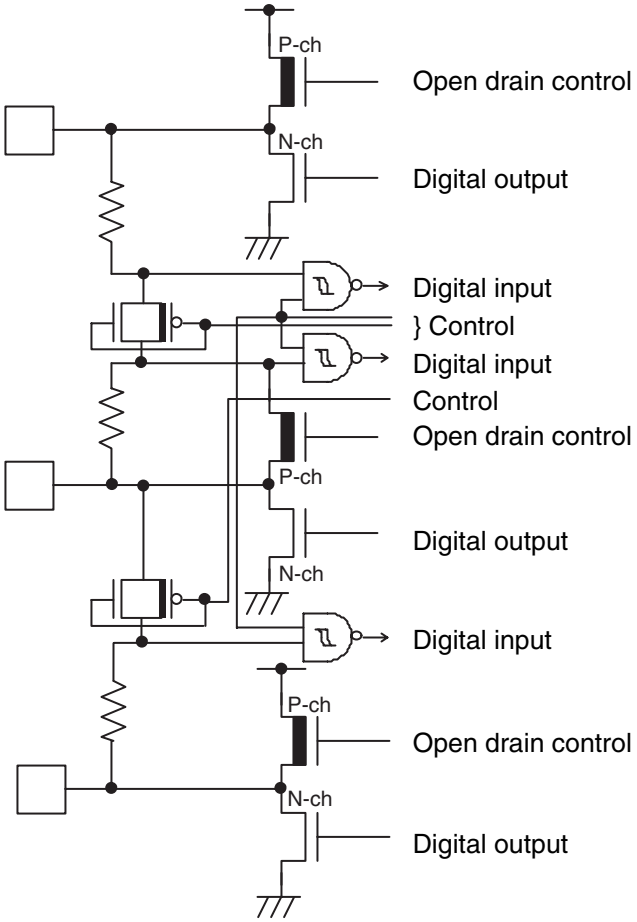
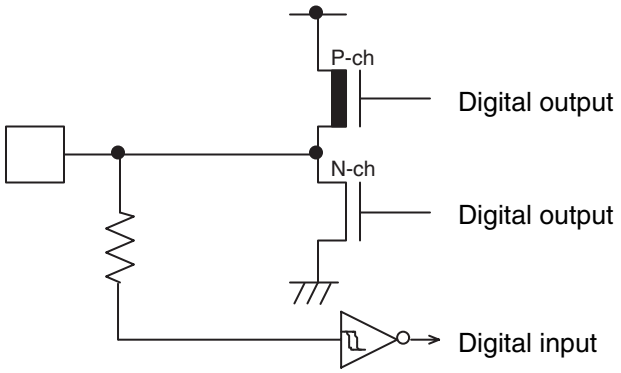
Type	Circuit type	Remarks
N		• 3 ports for I²C • CMOS level hysteresis input • CMOS level output • With stop control
O		• CMOS level output • CMOS level hysteresis input • Without standby control

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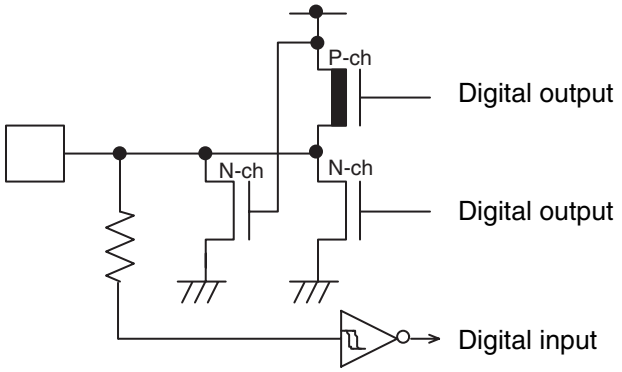
(Continued)

Type	Circuit type	Remarks
P		• CMOS level output • CMOS level hysteresis input • Without standby control • With pull-down resistor

■ HANDLING DEVICES

- **Preventing a Latch-up**

  A latch-up can occur on a CMOS IC under following conditions. A latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

  - When a voltage higher than VDDE or VDDI or a voltage lower than VSS is applied to an input or output pin.
  - When a voltage higher than the rating is applied between VDDE or VDDI and VSS.

- **Handling of Unused Input Pins**

  Do not leave an unused input pin open since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- **Power Supply Pins**

  If more than one VDDE or VDDI or VSS pin exists, those that must be kept at the same potential are designed to be connected to one other inside the device to prevent malfunctions such as latch-up. Be sure to connect the pins to a power supply and ground external to the device to minimize undesired electromagnetic radiation, prevent strobe signal malfunctions due to an increase in ground level, and conform to the total output current rating. Given consideration to connecting the current supply source to VDDE or VDDI and VSS pin of the device at the lowest impedance possible.

  It is also recommended that a ceramic capacitor of around 0.1 μF be connected between VDDE or VDDI and VSS pin at circuit points close to the device as a bypass capacitor.

- **Crystal Oscillation Circuit**

  Noise near the X0 or X1 pin may cause the device to malfunction. Design printed circuit boards so that X0, X1, the quartz oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as near to one another as possible.

  It is strongly recommended that printed circuit board artwork that surrounds the X0 and X1 pins with ground be used to increase the expectation of stable operation.

  Please ask the Oscillation maker to evaluate the oscillational characteristics of the crystal and this device.

- **Mode Pins (MD0 to MD3)**

  In order to prevent mistakes due to noise, and sending them into test mode, connect these pins as close to VDDE and VSS pins, and at as low an impedance as possible.

- **Tool Reset Pins ($\overline{\text{TRST}}$)**

  Be sure to input the same signal as the $\overline{\text{INIT}}$ when this pin is not used for the tool. The same processing is executed for the mass product.

- **Power-on**

  Immediately after power-on, be sure to apply setting initialization reset (INIT) with $\overline{\text{INIT}}$ pin.

  Also immediately after power-on, keep the $\overline{\text{INIT}}$ pin at the “L” level until the oscillator has reached the required oscillation stabilization wait time. (For initialization by INIT from the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time is set to the minimum value.)

- **Source Oscillation Input at Power-on**

  At power-on, be sure to input a source clock until the oscillation stabilization wait time is reached.

• **Precautions at Power-On/Power-Off**

• Precautions when turning on and off VDDI pin and VDDE pin

To ensure the reliability of LSI devices, do not continuously apply only VDDE pin for about a minute when VDDI is off.

When VDDE pin is changed from off to on, the power noise may make it impossible to retain the internal state of the circuit.

Power-on : Supply voltage of VDDI pin → analog → Supply voltage of VDDE pin → signal

Power-off : Signal → Supply voltage of VDDE pin → analog → Supply voltage of VDDI pin

• Indeterminate Output when the Power is Turned On

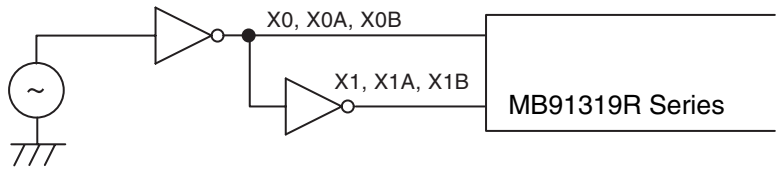
When turning on the power, the output pin may remain indeterminate until internal power supply becomes stable.

• Clock

About the attention when the external clock is used

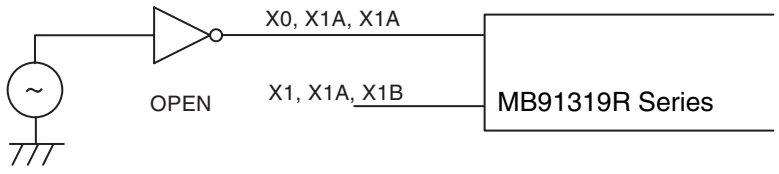
When the external clock is used, in principle, supply a clock signal to the X0 (X0A, X0B) pin and an opposite-phase clock signal to the X1 (X1A, X1B) pin at the same time. However, in this case the stop mode (oscillator stop mode) must not be used (This is because, in STOP mode, the X1 (X1A, X1B) pin stops at “H” output) . At 12.5 MHz or less, the device can be used with the clock signal supplied only to the X0 (X0A, X0B) pin.

• Using an External Clock (normal)



Note: The STOP mode (oscillation stop mode) cannot be used.

• Using an External Clock (available at 12.5 MHz or less)



Note : The X1 (X1A, X1B) pin must be designed to have a delay within 15 ns, at 10 MHz, from the signal to the X0 (X0A, X0B) pin.

• Restrictions
Common in MB91319R series

(1) Clock control block
Take the oscillation stabilization wait time during Low level input to the $\overline{INIT}$ pin.

(2) Bit Search Module
The 0-detection data register (BSD0) , 1-detection data register (BSD1) , and transition-detection data register (BSDC) are only word-accessible.

(3) I/O port
Ports are accessed only in bytes.

(4) Low-power Consumption Mode
• Be sure to use the following sequence to enter standby mode if synchronous standby mode is being used (the SYNCS bit (bit 8) of the TBCR (timebase counter control register) is set) :

```
 (LD1 #value_of_stanby, R0)
 (LD1 #_STCR, R12)
STB R0, @R12          ; Write to standby control register (STCR)
LDUB    @R12, R0      ; STCR read for synchronous standby
LDUB    @R12, R0      ; Dummy re-read of STCR
NOP                   ; NOP × 5 for adjusted timing
NOP
NOP
NOP
NOP
```

(5) Notes on the PS register
The PS register is processed prior to the execution of some instructions, which may cause the exception handling described below to trigger breakpoints in interrupt processing routines or to update the displayed contents of the PS register when the debugger is being used.
In all of these situations, because the microcontroller has been designed to correctly perform reprocessing after returning from an EIT, the operation before and after the EIT is performed according to the specifications.

• The following operations are performed if, in the instruction immediately before a DIVOU or DIVOS instruction, a user interrupt or an NMI occurs, single-step execution is performed, or break is selected from the emulator menu.
(1)The D0 and D1 flags are updated in advance.
(2)An EIT handling routine (user interrupt, NMI, or emulator) is executed.
(3)Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1) .

• If the any of the ORCCR, STILM, MOV Ri or PS instructions is executed in order to enable interrupts when a user interrupt source or NMI source is in the interrupt occurred state, the following operations are performed.
(1)The PS register is updated in advance.
(2)An EIT handling routine (user interrupt and NMI) is executed.
(3)Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1) .

(6) Watchdog timer

The watchdog timer that is built into this product monitors the program to see if it performs a reset delay operation within a fixed period of time. And, that resets the CPU if the reset delay operation is not performed due to a runaway program.
As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.
A watchdog reset may not be generated in the above situation caused by the system running out of control. In that case, reset (INIT) by external $\overline{\text{INIT}}$ pin.

(7) Notes on using A/D

The MB91319R series has built-in A/D converter. Do not supply a voltage higher than VDDE to the AVCC.

• Software reset in synchronous mode

When software reset in the synchronous mode is used, the following two conditions must be satisfied before setting the SRST bit of the STCR (standby control register) to 0.
- Set the interrupt enable flag (I-Flag) to the interrupt disabled (I-Flag = 0).
- Do not use NMI.

(8) Simultaneous generation of software break and user interrupt/NMI (only for MB91FV319R)

If a software break and a user interrupt/NMI occur simultaneously, the emulator debugger may cause the following phenomena.
- The debugger stops pointing to a location other than the programmed breakpoints.
- The halted program is not re-executed correctly.

If these phenomena occur, use a hardware break instead of the software break. If the monitor debugger has been used, avoid setting any break at the relevant location.

(9) Step execution of RETI instruction

In an environment where interrupts frequently occur during single-step execution, only the relevant interrupt processing routines are executed repeatedly during single-step execution of the RETI instruction. This will prevent the main routine and low-interrupt-level programs from being executed. To avoid it, do not single-step RETI instructions.
When the relevant interrupt routine no longer requires being debugged, disable the relevant interrupt and perform debugging.

(10) About an operand break

Do not apply a data event break to access to the area containing the address of a stack pointer.

(11) Example of batch file for configuration

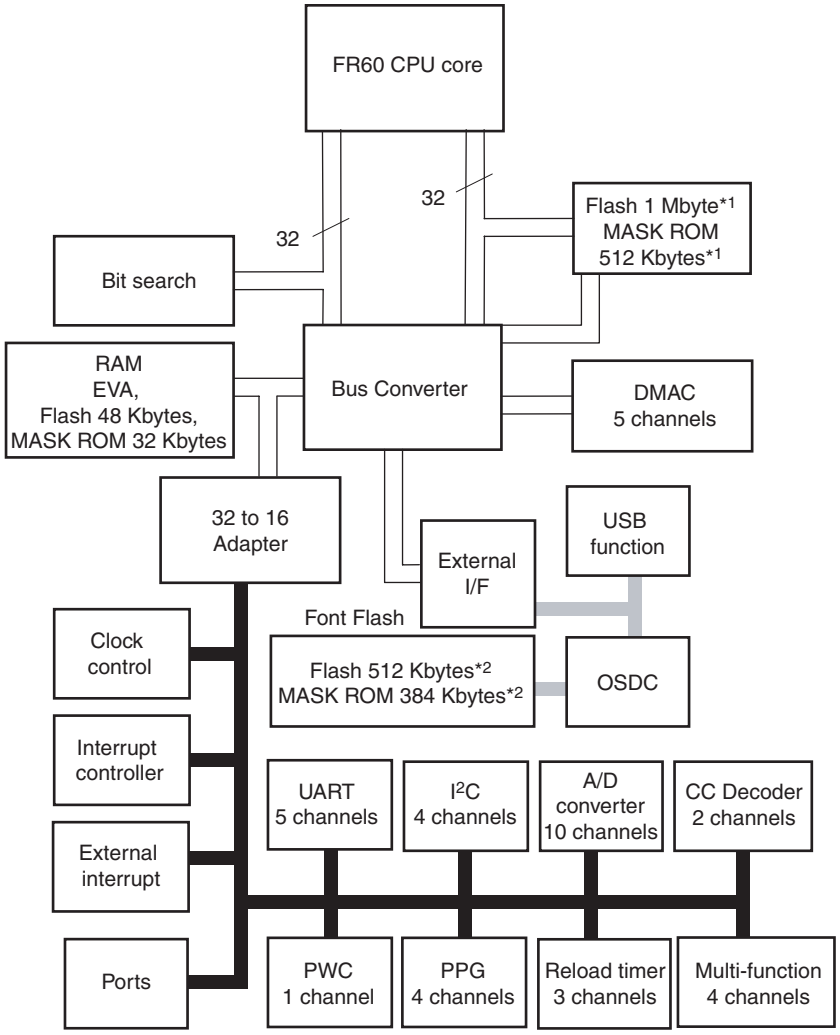
To debug a program downloaded to internal RAM, be sure to execute the following batch file after executing RESET.

```
#------------------------------------------------------------------------------
#Set MODR (0x7fd)  = Enable In memory + 16-bit External Bus
set mem/byte 0x7fd = 0x5
#------------------------------------------------------------------------------
```

(12) Address in the built-in Flash/ROM area (Flash memory for program : 1 Mbyte product)

The address 0X0017FFF8 in the built-in Flash/ROM area has been reserved. You must configure the FE.

■ BLOCK DIAGRAM



*1 : MB91FV319R and MB91F318R/F318S contain the program ROM of 1 Mbyte flash memory, and MB91316/316A contain that of 512 Kbytes MASK ROM.

*2 : MB91FV319R contains the font ROM of 512 Kbytes flash memory, and MB91F318R/F318S, MB91316/316A contain that of 384 Kbytes MASK ROM.

■ MEMORY SPACE

The FR family has 4 GB of logical address space (2^{32} addresses) available to the CPU by linear access.

• Direct Addressing Areas

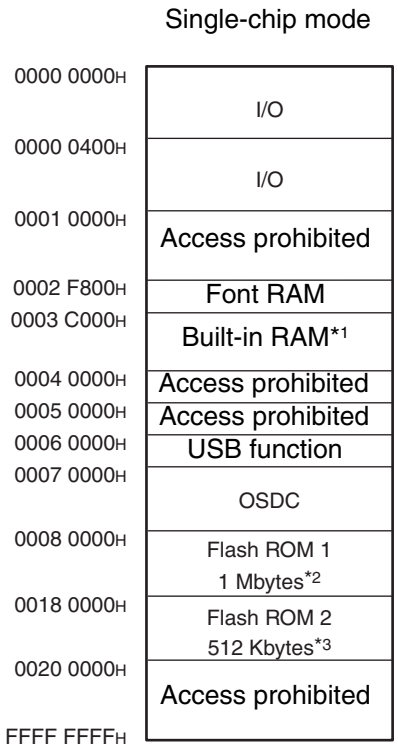
The following address space area is used for I/O.

This area is called the direct addressing area. The addresses of operands in this area may be specified directly in an instruction.

The direct addressing area varies depending on the size of the data being accessed as follows.

→ Byte data access : 000H to 0FFH
→ Half word data access : 000H to 1FFH
→ Word data access : 000H to 3FFH

• Memory Map

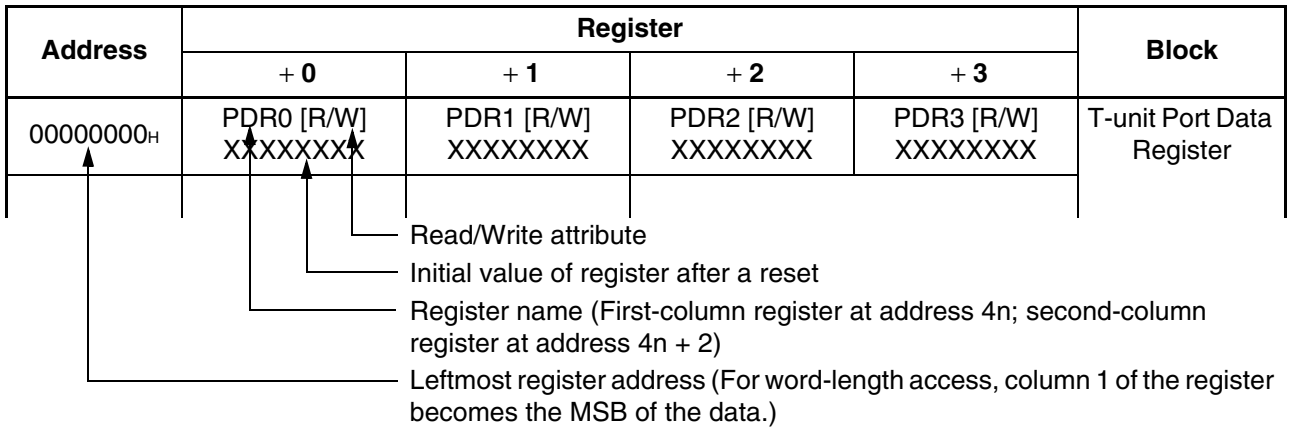


*1 : Built-in RAM area of MB91F318R/F318S, MB91FV319R is 0003 4000H to 0003 FFFFH (48 Kbytes) .
Built-in RAM area of MB91316/316A is 0003 8000H to 0003 FFFFH (32 Kbytes) .
*2 : MB91316/316A is 0008 0000H to 000F FFFFH (MASK ROM 512 Kbytes).
*3 : MB91F318R/F318S and MB91316/316A are 0018 0000H to 001F FFFFH (MASK ROM 384 Kbytes) .

■ I/O MAP

This shows the correspondence between the memory space area and various peripheral resource registers.

[How to read the table]



Note : Initial values of register bits are represented as follows :

"1" : Initial Value "1"
"0" : Initial Value "0"
"X" : Initial Value "X"
" - " : No physical register at this location

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H to 00000FH	—	—	—	—	Reserved
000010H	PDR0[R/W] XXXXXXXX	PDR1[R/W] XXXXXXXX	PDR2[R/W] XXXXXXXX	PDR3[R/W] XXXXXXXX	R-bus Port Data Register
000014H	PDR4[R/W] XXXXXXXX	PDR5[R/W] XXXXXXXX	—	PDR7[R/W] --XXXXXX	
000018H	PDR8[R/W] XXXXXXXX	PDR9[R/W] XXXXXXXX	PDRA[R/W] -----XXX	PDRB[R/W] XXXXXXXX	
00001CH	PDRC[R/W] XXXXXXXX	—	—	—	
000020H	ADCTH[R/W] XXXXXX00	ADCTL[R/W] 00000X00	ADCH[R/W] 00000000 00000000		10-bit A/D Converter
000024H	ADAT0[R] XXXXXX00 00000000		ADAT1[R] XXXXXX00 00000000		
000028H	ADAT2[R] XXXXXX00 00000000		ADAT3[R] XXXXXX00 00000000		
00002CH	ADAT4[R] XXXXXX00 00000000		ADAT5[R] XXXXXX00 00000000		
000030H	ADAT6[R] XXXXXX00 00000000		ADAT7[R] XXXXXX00 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000034H to 00003CH	—	—	—	—	Reserved
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000		Ext int
000044H	DICR [R/W] -------0	HRCL [R/W] 0--11111	—		DLYI/I-unit
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R/W] ----0000 00000000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R/W] ----0000 00000000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR2 [R/W] ----0000 00000000		
000060H	SSR0 [R/W] 00001-00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00--0-0-	UART0
000064H	UTIM0 [R] (UTIMR [W]) 00000000 00000000		DRCL0 [W] --------	UTIMC0 [R/W] 0--00001	U-TIMER 0
000068H	SSR1 [R/W] 00001-00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00--0-0-	UART1
00006CH	UTIM1 [R] (UTIMR [W]) 00000000 00000000		DRCL1 [W] --------	UTIMC1 [R/W] 0--00001	U-TIMER 1
000070H	SSR2 [R/W] 00001-00	SIDR2 [R/W] XXXXXXXX	SCR2 [R/W] 00000100	SMR2 [R/W] 00--0-0-	UART2
000074H	UTIM2 [R] (UTIMR [W]) 00000000 00000000		DRCL2 [W] --------	UTIMC2 [R/W] 0--00001	U-TIMER 2
000078H	SSR3 [R/W] 00001-00	SIDR3 [R/W] XXXXXXXX	SCR3 [R/W] 00000100	SMR3 [R/W] 00--0-0-	UART3
00007CH	UTIM3 [R] (UTIMR [W]) 00000000 00000000		DRCL3 [W] --------	UTIMC3 [R/W] 0--00001	U-TIMER 3
000080H	SSR4 [R/W] 00001-00	SIDR4 [R/W] XXXXXXXX	SCR4 [R/W] 00000100	SMR4 [R/W] 00--0-0-	UART4
000084H	UTIM4 [R] (UTIMR [W]) 00000000 00000000		DRCL4 [W] --------	UTIMC4 [R/W] 0--00001	U-TIMER 4

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000088H to 00008CH	—		—		Reserved
000090H	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	—		PWC
000094H	PWCD[R] XXXXXXXX XXXXXXXX		—		
000098H	PWCC2[R/W] 000-----	Reserved	—		PWC
00009CH	PWCUD[R] XXXXXXXX XXXXXXXX		—		
0000A0H to 0000ACH	—		—		Reserved
0000B0H	IFN0 [R] 00000000	IFRN0 [R/W] 00000000	IFCR0 [R/W] 00-00000	IFDR0 [R/W] 00000000	I²C Interface 0
0000B4H	IBCR0 [R/W] 00000000	IBSR0 [R/W] 00000000	ITBA0 [R/W] ------00 00000000		
0000B8H	ITMK0 [R/W] 00----11 11111111		ISMK0 [R/W] 01111111	ISBA0 [R/W] 00000000	
0000BCH	—	IDAR0 [R/W] 00000000	ICCR0 [R/W] 0-011111	IDBL0 [R/W] -------0	
0000C0H	IFN1 [R] 00000000	IFRN1 [R/W] 00000000	IFCR1 [R/W] 00-00000	IFDR1 [R/W] 00000000	I²C Interface 1
0000C4H	IBCR1 [R/W] 00000000	IBSR1 [R/W] 00000000	ITBA1 [R/W] ------00 00000000		
0000C8H	ITMK1 [R/W] 00----11 11111111		ISMK1 [R/W] 01111111	ISBA1 [R/W] 00000000	
0000CCH	—	IDAR1 [R/W] 00000000	ICCR1 [R/W] 0-011111	IDBL1 [R/W] -------0	
0000D0H	IFN2 [R] 00000000	IFRN2 [R/W] 00000000	IFCR2 [R/W] 00-00000	IFDR2 [R/W] 00000000	I²C Interface 2
0000D4H	IBCR2 [R/W] 00000000	IBSR2 [R/W] 00000000	ITBA2 [R/W] ------00 00000000		
0000D8H	ITMK2 [R/W] 00----11 11111111		ISMK2 [R/W] 01111111	ISBA2 [R/W] 00000000	
0000DCH	—	IDAR2 [R/W] 00000000	ICCR2 [R/W] 0-011111	IDBL2 [R/W] -------0	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000E0H	IFN3 [R] 00000000	IFRN3 [R/W] 00000000	IFCR3 [R/W] 00-00000	IFDR3 [R/W] 00000000	I²C Interface 3
0000E4H	IBCR3 [R/W] 00000000	IBSR3 [R/W] 00000000	ITBA3 [R/W] ------00 00000000		
0000E8H	ITMK3 [R/W] 00----11 11111111		ISMK3 [R/W] 01111111	ISBA3 [R/W] 00000000	
0000ECH	—	IDAR3 [R/W] 00000000	ICCR3 [R/W] 0-011111	IDBL3 [R/W] -------0	
0000F0H	T0LPCR [R/W] -----000	T0CCR [R/W] 0-010000	T0TCR [R/W] 00000000	T0R [R/W] ---00000	Multi function Timer
0000F4H	T0DRR [R/W] XXXXXXXX XXXXXXXX		T0CRR [R/W] XXXXXXXX XXXXXXXX		
0000F8H	T1LPCR [R/W] -----000	T1CCR [R/W] 0-000000	T1TCR[R/W] 00000000	T1R [R/W] ---00000	
0000FCH	T1DRR [R/W] XXXXXXXX XXXXXXXX		T1CRR [R/W] XXXXXXXX XXXXXXXX		
000100H	T2LPCR [R/W] -----000	T2CCR [R/W] 0-000000	T2TCR [R/W] 00000000	T2R [R/W] ---00000	
000104H	T2DRR [R/W] XXXXXXXX XXXXXXXX		T2CRR [R/W] XXXXXXXX XXXXXXXX		
000108H	T3LPCR [R/W] -----000	T3CCR [R/W] 0-000000	T3TCR [R/W] 00000000	T3R [R/W] ---00000	
00010CH	T3DRR [R/W] XXXXXXXX XXXXXXXX		T3CRR [R/W] XXXXXXXX XXXXXXXX		
000110H	TMODE [R/W] -------- -----0--		—	—	
000114H to 00011FH	—		—		Reserved
000120H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PPG0
000124H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 00000000	PCNL0 [R/W] 00000000	
000128H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PPG1
00012CH	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 00000000	PCNL1 [R/W] 00000000	
000130H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PPG2
000134H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 00000000	PCNL2 [R/W] 00000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000138H	PTMR3 [R] 11111111 11111111		PCSR3[W] XXXXXXXX XXXXXXXX		PPG3
00013CH	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 00000000	PCNL3 [R/W] 00000000	
000140H to 00014CH	—				Reserved
000150H to 00015CH	—				Reserved
000160H	DSLC00 0-------	DSLC10 -011----	CCDC0 00-00011	VSEP0 00--0001	CC decoder 0 channel
000164H	CSYSEP0 -101-011	HMASK0 --100000	HCLR0 ---00110	FLD0 00100000	
000168H	HCNT0 00000000	C21H0 0-111111	CRIP0 11111111	CRIC0 000-0000	
00016CH	CSTB0 11111111	CDTH0 11111111	CDAT00 00000000	CDAT10 00000000	
000170H	ID1C0 0-----00	ID20H0 0-111111	IDREF0 0-111111	IDTH0 11111111	
000174H	IDSTB0 11111111	IDDAT00 --000000	IDDAT10 00000000	IDDAT20 --000000	
000178H	DSAC10 ---000-0	DSAC20 10110011	DSAC30 00-00-00	—	
00017CH	—	—	—	—	
000180H	DSLC01 0-------	DSLC11 -011----	CCDC1 00-00011	VSEP1 00--0001	CC decoder 1 channel
000184H	CSYTSEP1 -101-011	HMASK1 --100000	HCLR1 ---00110	FLD1 00100000	
000188H	HCNT1 00000000	C21H1 0-111111	CRIP1 11111111	CRIC1 000-0000	
00018CH	CSTB1 11111111	CDTH1 11111111	CDAT01 00000000	CDAT1 00000000	
000190H	ID1C1 0-----00	ID20H1 0-111111	IDREF1 0-111111	IDTH1 11111111	
000194H	IDSTB1 11111111	IDDAT01 --000000	IDDAT11 00000000	IDDAT21 --000000	
000198H	DSAC11 ---000-0	DSAC21 10110011	DSAC31 00-00-00	—	
00019CH	—	—	—	—	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001A0H to 0001FCH	—				Reserved
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228H	—				
00022CH to 00023CH	—				Reserved
000240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244H to 0002FCH	—				Reserved
000300H to 0003ECH	—				
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000400H	DDR0 [R/W] 00000000	DDR1 [R/W] 00000000	DDR2 [R/W] 00000000	DDR3 [R/W] 00000000	R-bus Port Direction Register
000404H	DDR4 [R/W] 00000000	DDR5 [R/W] 00000000	—	DDR7 [R/W] --000000	
000408H	DDR8 [R/W] 00000000	DDR9 [R/W] 00000000	DDRA [R/W] -----000	DDRB [R/W] 00000000	
00040CH	DDRC [R/W] 00000000	—	—	—	
000410H	PFR0 [R/W] 0--00000	PFR1 [R/W] 00000000	PFR2 [R/W] 00000000	PFR3 [R/W] 00000000	R-bus Port Function Register
000414H	PFR4 [R/W] 0000--00	PFR5 [R/W] 11111111	PFR6 [R/W] 11111111	PFR7 [R/W] 11111111	
000418H	PFR8 [R/W] 11111111	PFR9 [R/W] 11111111	PFRA [R/W] 11111111	PFRB [R/W] 11111111	
00041CH	PFRC [R/W] 1111---1	PFRD [R/W] ---11111	—	—	
000420H to 00043CH	—				Reserved
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02[R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000470H to 00047CH	—				Reserved
000480H	RSRR [R/W] 10000000*2	STCR [R/W] 00110011*2	TBCR [R/W] 00XXXX00*1	CTBR [W] XXXXXXXX	Clock Control Unit
000484H	CLKR [R/W] 00000000*1	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011*1	DIVR1[R/W] 00000000*1	
000488H	—	—	OSCCR [R/W] XXXXXXX0	—	Reserved
00048CH	WPCR [R/W] B 00---000	—	—	—	Watch Timer
000490H	OSCR [R/W] B 00---000	—	—	—	Main Oscillation Stabilization Wait Timer
000494H to 0005FCH	—				Reserved
000600H to 0007FCH	—				Reserved
000800H to 000AFCH	—				Reserved
000B00H	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXX	—	DSU
000B04H	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	
000B08H	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	
000B0CH	EWP1 [R] 00000000 00000000		—		
000B10H	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		
000B14H to 000B1CH	—				
000B20H	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24H	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000B28H	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU
000B2CH	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30H	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3CH	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4CH	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5CH	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70H to 000FFCH	—				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 006FFCH	—				Reserved
007000H	FLCR [R/W] 0110X000	—			Program Flash I/F
007004H	FLWC [R/W] 00010011	—			
007008H to 0070FFH	—				Reserved
007100H	FNCR [R/W] 0110X000	—			Font Flash I/F
007104H	FNWT [R/W] 00010011	—			

*1 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset.

*2 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset by the $\overline{\text{INIT}}$ pin.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
050000H to 050024H	Reserved				Reserved
050028H to 05FFFFH	Reserved				Reserved
060000H	FIFO0o [R] XXXXXXXX XXXXXXXX		FIFO0i [W] XXXXXXXX XXXXXXXX		USB Function
060004H	FIFO1 [R] XXXXXXXX XXXXXXXX		FIFO2 [W] XXXXXXXX XXXXXXXX		
060008H	FIFO3 [R] XXXXXXXX XXXXXXXX		—		
06000CH to 06001FH	Reserved				
060020H	Reserved		CONT1 [R/W] 000XX0XX XXX00000		
060024H	CONT2 [R/W] XXXXXXXX XXX00000		CONT3 [R/W] XXXXXXXX XXX00000		
060028H	CONT4 [R/W] XXXXXXXX XXX00000		CONT5 [R/W] XXXXXXXX XXXX00XX		
06002CH	CONT6 [R/W] XXXXXXXX XXXX00XX		CONT7 [R/W] XXXXXXXX XXX00000		
060030H	CONT8 [R/W] XXXXXXXX XXX00000		CONT9 [R/W] 0XX0XXXX 0XXX0000		
060034H	CONT10 [R/W] 00000000 X00000XX		TTSIZE [R/W] 00010001 00010001		
060038H	TRSIZE [R/W] 00010001 00010001		Reserved		
06003CH	Reserved				
060040H	RSIZE0 [R] XXXXXXXX XXXX0000		Reserved		
060044H	RSIZE1 [R] XXXXXXXX X0000000		Reserved		
060048H to 06005FH	Reserved				
060060H	Reserved		ST1 [R/W] XXXXXX00 00000000		
060064H	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
060068H	ST2 [R] XXXXXXXX X0000000		ST3 [R/W] 00XXXXXX X0000000		USB Function
06006CH	ST4 [R/W] XXXXX000 00000000		ST5 [R/W] 0XX00XXX XX000000		
060070H to 06007FH	Reserved				
060080H to 06FFFFH	Reserved				Reserved
078000H	OSD_VADR [W] XXXXXXXX XXXXXXXX		OSD_CD1 [W] XXXXXXXX XXXXXXXX		OSDC (MAIN)
078004H	OSD_CD2 [W] XXXXXXXX XXXXXXXX		OSD_RCD1 [W] XXXXXXXX XXXXXXXX		
078008H	OSD_RCD2 [W] XXXXXXXX XXXXXXXX		OSD_SOC1 [W] XXXXXXXX 0000XXXX		
07800CH	OSD_SOC2 [W] XXXXXXXX XXXXXXXX		OSD_VDPC [W] XXXXXXXX XXXXXXXX		
078010H	OSD_HDPC [W] XXXXXXXX XXXXXXXX		OSD_CVSC [W] XXXXXXXX XXXXXXXX		
078014H	OSD_SBFCC [W] XXXXXXXX XXXXXXXX		OSD_THCC [W] XXXXXXXX XXXXXXXX		
078018H	OSD_GFCC [W] XXXXXXXX XXXXXXXX		OSD_SBCC1 [W] XXXXXXXX XXXXXXXX		
07801CH	OSD_SBCC2 [W] XXXXXXXX XXXXXXXX		OSD_SPCC1 [W] XXXXXXXX XXXXXXXX		
078020H	OSD_SPCC2 [W] XXXXXXXX XXXXXXXX		OSD_SPCC3 [W] XXXXXXXX XXXXXXXX		
078024H	OSD_SPCC4 [W] XXXXXXXX XXXXXXXX		OSD_SYNCC [W] XXXXXXXX XXXXXXXX		
078028H	—		—		
07802CH	—		OSD_IOC1 [W] XXXXXXXX XXXXXX00		
078030H	OSD_IOC2 [W] XXXXXXXX XXXXXXXX		OSD_DPC1 [W] XXXXXXXX XXXXXXXX		
078034H	OSD_DPC2 [W] XXXXXXXX XXXXXXXX		OSD_DPC3 [W] XXXXXXXX XXXXXXXX		
078038H	OSD_DPC4 [W] XXXXXXXX XXXXXXXX		OSD_IRC [W] XXXXXXXX XXXXXXXX		
07803CH	OSD_PLT0 [W] XXXXXXXX XXXXXXXX		OSD_PLT1 [W] XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
078040H	OSD_PLT2 [W] XXXXXXXX XXXXXXXX		OSD_PLT3 [W] XXXXXXXX XXXXXXXX		OSDC (MAIN)
078044H	OSD_PLT4 [W] XXXXXXXX XXXXXXXX		OSD_PLT5 [W] XXXXXXXX XXXXXXXX		
078048H	OSD_PLT6 [W] XXXXXXXX XXXXXXXX		OSD_PLT7 [W] XXXXXXXX XXXXXXXX		
07804CH	OSD_PLT8 [W] XXXXXXXX XXXXXXXX		OSD_PLT9 [W] XXXXXXXX XXXXXXXX		
078050H	OSD_PLT10 [W] XXXXXXXX XXXXXXXX		OSD_PLT11 [W] XXXXXXXX XXXXXXXX		
078054H	OSD_PLT12 [W] XXXXXXXX XXXXXXXX		OSD_PLT13 [W] XXXXXXXX XXXXXXXX		
078058H	OSD_PLT14 [W] XXXXXXXX XXXXXXXX		OSD_PLT15 [W] XXXXXXXX XXXXXXXX		
07805CH	OSD_ACT1 [W] XXXXXXXX XXXXXXXX		OSD_ACT2 [W] XXXXXXXX XXXXXXXX		
078060H	OSD_PLACC11 [W] XXXXXXXX XXXXXXXX		OSD_PLACC12 [W] XXXXXXXX XXXXXXXX		
078064H	OSD_PLACC2 [W] XXXXXXXX XXXXXXXX		OSD_PLACC3 [W] XXXXXXXX XXXXXXXX		
078068H	OSD_PLBCC11 [W] XXXXXXXX XXXXXXXX		OSD_PLBCC12 [W] XXXXXXXX XXXXXXXX		
07806CH	OSD_PLBCC2 [W] XXXXXXXX XXXXXXXX		OSD_PLBCC3 [W] XXXXXXXX XXXXXXXX		
078070H	OSD_PLCC11[W] XXXXXXXX XXXXXXXX		OSD_PLCC12[W] XXXXXXXX XXXXXXXX		
078074H	OSD_PLCC2[W] XXXXXXXX XXXXXXXX		OSD_PLCC3[W] XXXXXXXX XXXXXXXX		
078078H	OSD_CSC1 [W] XXXXXXXX XXXXXXXX		OSD_CSC2 [W] XXXXXXXX XXXXXXXX		
07807CH to 0780FFH	—		—		Reserved
078100H	CCOSD_VADR [W] XXXXXXXX XXXXXXXX		CCOSD_CD1 [W] XXXXXXXX XXXXXXXX		OSDC (CC)
078104H	CCOSD_CD2 [W] XXXXXXXX XXXXXXXX		CCOSD_RCD1 [W] XXXXXXXX XXXXXXXX		
078108H	CCOSD_RCD2 [W] XXXXXXXX XXXXXXXX		CCOSD_SOC1 [W] XXXXXXXX 0000XXXX		
07810CH	CCOSD_SOC2 [W] XXXXXXXX XXXXXXXX		CCOSD_VDPC [W] XXXXXXXX XXXXXXXX		

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
078110H	CCOSD_HDPC [W] XXXXXXXX XXXXXXXX		CCOSD_CVSC [W] XXXXXXXX XXXXXXXX		OSDC (CC)
078114H	—		CCOSD_THCC [W] XXXXXXXX XXXXXXXX		
078118H	—		—		
07811CH	—		—		
078120H	—		—		
078124H	—		—		
078128H	—		—		
07812CH	—		—		
078130H	—		CCOSD_DPC1 [W] XXXXXXXX XXXXXXXX		
078134H	CCOSD_DPC2 [W] XXXXXXXX XXXXXXXX		CCOSD_DPC3 [W] XXXXXXXX XXXXXXXX		
078138H	CCOSD_DPC4 [W] XXXXXXXX XXXXXXXX		CCOSD_IRC [W] XXXXXXXX XXXXXXXX		
07813CH	CCOSD_PLT0 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT1 [W] XXXXXXXX XXXXXXXX		
078140H	CCOSD_PLT2 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT3 [W] XXXXXXXX XXXXXXXX		
078144H	CCOSD_PLT4 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT5 [W] XXXXXXXX XXXXXXXX		
078148H	CCOSD_PLT6 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT7 [W] XXXXXXXX XXXXXXXX		
07814CH	CCOSD_PLT8 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT9 [W] XXXXXXXX XXXXXXXX		
078150H	CCOSD_PLT10 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT11 [W] XXXXXXXX XXXXXXXX		
078154H	CCOSD_PLT12 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT13 [W] XXXXXXXX XXXXXXXX		
078158H	CCOSD_PLT14 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT15 [W] XXXXXXXX XXXXXXXX		
07815CH	—		—		
078160H to 07FFFFH	Reserved				Reserved

■ INTERRUPT FACTORS, INTERRUPT VECTORS, AND INTERRUPT REGISTER

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
Reset	0	00	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	$3EC_H$	$000FFFEC_H$	—
System reserved	5	05	—	$3E8_H$	$000FFFE8_H$	—
System reserved	6	06	—	$3E4_H$	$000FFFE4_H$	—
Coprocessor absent trap	7	07	—	$3E0_H$	$000FFFE0_H$	—
Coprocessor error trap	8	08	—	$3DC_H$	$000FFFDC_H$	—
INTE instruction	9	09	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	$3D0_H$	$000FFFD0_H$	—
Step trace trap	12	0C	—	$3CC_H$	$000FFFCC_H$	—
NMI request (tool)	13	0D	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	15 (F_H) fixed	$3C0_H$	$000FFFC0_H$	—
External interrupt 0	16	10	ICR00	$3BC_H$	$000FFFBC_H$	—
External interrupt 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	—
External interrupt 2	18	12	ICR02	$3B4_H$	$000FFFB4_H$	—
External interrupt 3	19	13	ICR03	$3B0_H$	$000FFFB0_H$	—
External interrupt 4 (USB function)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	—
External interrupt 5 (OSDC-MAIN)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	—
External interrupt 6 (OSDC-CC)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	—
System reserved	23	17	ICR07	$3A0_H$	$000FFFA0_H$	—
Reload timer 0	24	18	ICR08	$39C_H$	$000FFF9C_H$	8
Reload timer 1	25	19	ICR09	398_H	$000FFF98_H$	9
Reload timer 2	26	1A	ICR10	394_H	$000FFF94_H$	10
UART0 (Reception completed)	27	1B	ICR11	390_H	$000FFF90_H$	0
UART1 (Reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	1
UART2 (Reception completed)	29	1D	ICR13	388_H	$000FFF88_H$	2
UART0 (Transmission completed)	30	1E	ICR14	384_H	$000FFF84_H$	3
UART1 (Transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	4

(Continued)

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
UART2 (Transmission completed)	32	20	ICR16	37C$_H$	000FFF7C$_H$	5
DMAC0 (end, error)	33	21	ICR17	378$_H$	000FFF78$_H$	—
DMAC1 (end, error)	34	22	ICR18	374$_H$	000FFF74$_H$	—
DMAC2 (end, error)	35	23	ICR19	370$_H$	000FFF70$_H$	—
DMAC3 (end, error)	36	24	ICR20	36C$_H$	000FFF6C$_H$	—
DMAC4 (end, error)	37	25	ICR21	368$_H$	000FFF68$_H$	—
A/D converter	38	26	ICR22	364$_H$	000FFF64$_H$	—
PPG0	39	27	ICR23	360$_H$	000FFF60$_H$	—
PPG1	40	28	ICR24	35C$_H$	000FFF5C$_H$	—
PPG2	41	29	ICR25	358$_H$	000FFF58$_H$	—
PPG3	42	2A	ICR26	354$_H$	000FFF54$_H$	—
PWC	43	2B	ICR27	350$_H$	000FFF50$_H$	—
CCD0	44	2C	ICR28	34C$_H$	000FFF4C$_H$	—
CCD1	45	2D	ICR29	348$_H$	000FFF48$_H$	—
Main oscillation wait	46	2E	ICR30	344$_H$	000FFF44$_H$	—
Time-base timer overflow	47	2F	ICR31	340$_H$	000FFF40$_H$	—
System reserved	48	30	ICR32	33C$_H$	000FFF3C$_H$	—
Watch timer	49	31	ICR33	338$_H$	000FFF38$_H$	—
I^2C ch.0	50	32	ICR34	334$_H$	000FFF34$_H$	—
I^2C ch.1	51	33	ICR35	330$_H$	000FFF30$_H$	—
I^2C ch.2	52	34	ICR36	32C$_H$	000FFF2C$_H$	—
I^2C ch.3	53	35	ICR37	328$_H$	000FFF28$_H$	—
UART3 (Reception completed)	54	36	ICR38	324$_H$	000FFF24$_H$	—
UART4 (Reception completed)	55	37	ICR39	320$_H$	000FFF20$_H$	—
UART3 (Transmission completed)	56	38	ICR40	31C$_H$	000FFF1C$_H$	—
UART4 (Transmission completed)	57	39	ICR41	318$_H$	000FFF18$_H$	—
Multi-functional timer 0	58	3A	ICR42	314$_H$	000FFF14$_H$	—
Multi-functional timer 1	59	3B	ICR43	310$_H$	000FFF10$_H$	—
Multi-functional timer 2	60	3C	ICR44	30C$_H$	000FFF0C$_H$	—
Multi-functional timer 3	61	3D	ICR45	308$_H$	000FFF08$_H$	—
System reserved	62	3E	ICR46	304$_H$	000FFF04$_H$	—
Delay interrupt factor bit	63	3F	ICR47	300$_H$	000FFF00$_H$	—
System reserved (Used by REALOS)	64	40	—	2FC$_H$	000FFEFC$_H$	—
System reserved (Used by REALOS)	65	41	—	2F8$_H$	000FFEF8$_H$	—

(Continued)

(Continued)

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
System reserved	66	42	—	$2F4_H$	$000FFEF4_H$	—
System reserved	67	43	—	$2F0_H$	$000FFEF0_H$	—
System reserved	68	44	—	$2EC_H$	$000FFEEC_H$	—
System reserved	69	45	—	$2E8_H$	$000FFEE8_H$	—
System reserved	70	46	—	$2E4_H$	$000FFEE4_H$	—
System reserved	71	47	—	$2E0_H$	$000FFEE0_H$	—
System reserved	72	48	—	$2DC_H$	$000FFEDC_H$	—
System reserved	73	49	—	$2D8_H$	$000FFED8_H$	—
System reserved	74	4A	—	$2D4_H$	$000FFED4_H$	—
System reserved	75	4B	—	$2D0_H$	$000FFED0_H$	—
System reserved	76	4C	—	$2CC_H$	$000FFECC_H$	—
System reserved	77	4D	—	$2C8_H$	$000FFEC8_H$	—
System reserved	78	4E	—	$2C4_H$	$000FFEC4_H$	—
System reserved	79	4F	—	$2C0_H$	$000FFEC0_H$	—
Used by INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$	—

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage *	V_{DDE} (3.3 V)	V_{SS} – 0.5	V_{SS} + 4.0	V
	V_{DDI} (1.8 V)	V_{SS} – 0.3	V_{SS} + 2.5	V
Analog power supply voltage *	AV_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V
Input voltage *	V_I	V_{SS} – 0.5	V_{DDE} + 0.5	V
Analog pin input voltage *	V_{IA}	V_{SS} – 0.5	AVcc + 0.5	V
Output voltage *	V_O	V_{SS} – 0.5	V_{CC} + 0.5	V
Storage temperature	Tstg	– 40	+ 125	°C

* : The parameter is based on V_{SS} =AV_{SS} =0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} =0 V)

Parameter	Symbol	Value		Unit
		Min	Max	
Operating temperature	Ta	– 10	+ 70	°C
Power supply voltage	V_{DDE} (3.3 V)	3.00	3.6	V
	V_{DDI} (1.8 V)	1.65	1.95	
Analog power supply voltage	AV_{CC}	3.00	V_{DDE}	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(1) CPU

• MB91FV319R, MB91F318R/F318S

($Ta = -10\ °C$ to $+70\ °C$, $V_{DDE} = 3.3\ V \pm 0.3\ V$, $V_{DDI} = 1.8\ V \pm 0.15\ V$, $V_{SS} = 0\ V$)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Current dissipation (upper : 1.8V lower : 3.3V)	I_{CCT}	Watch mode $Ta = +25\ °C$, fclk = 32 kHz	—	400	900	µA	Dot clock PLL stop USB clock stop
			—	700	1000		
	I_{CC}	Normal operation $Ta = +25\ °C$, fcp = 40 MHz, fcpp = 20 MHz	—	140	180	mA	Dot clock at 90 MHz MB91F318R/F318S only
			—	140	190		
	I_{CCS}	Main sleep mode $Ta = +25\ °C$, fcp = 40 MHz, fcpp = 20 MHz	—	80	100	mA	Dot clock PLL stop
			—	80	110		
	I_{CCL}	Sub RUN mode $Ta = +25\ °C$, fclk = 32 kHz	—	500	1200	µA	Dot clock PLL stop USB clock stop
			—	900	1300		
	I_{CCH}	Main stop mode $Ta = +25\ °C$, fclk = 0 kHz	—	240	800	µA	
			—	50	100		
		$Ta = +70\ °C$, fclk = 0 kHz	—	1900	8800	µA	
			—	300	500		
"H" level input voltage	V_{IH}	—	$V_{CC} \times 0.8$	—	V_{CC}	V	
"L" level input voltage	V_{IL}	$V_{CC} = 3.3\ V$	V_{SS}	—	$V_{CC} \times 0.2$	V	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P74, P80 to P87, P90 to P97, PA0 to PA2, PB0 to PB4, PC0 to PC7, DCKI, VSYNC, HSYNC1 to HSYNC3
"H" level output voltage	V_{OH}	$V_{CC} = 3.3\ V$, $I_{OH} = -4\ mA$	$V_{CC} - 0.5$	—	V_{CC}	V	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P74, P80 to P87, P90 to P97, PA0 to PA2, PB0 to PB4, PC0 to PC7, B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH

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Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
"L" level output voltage	V_{OL}	V_{CC} = 3.3 V, I_{OL} = 4 mA	V_{SS}	—	0.4	V	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P74, P80 to P87, P90 to P97, PA0 to PA2, PB0 to PB4, PC0 to PC7, B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
Input leak current	I_{IL}	—	− 5	—	+ 5	µA	
I^2C bus switch connection resistor	R_{BS}	—	—	—	130	Ω	Between SCL2 and SCL3 Between SDA2 and SDA3 Between SCL3 and SCL4 Between SDA3 and SDA4
Analog RGB reference voltage	V_{REF}	—	1.05	1.10	1.15	V	VREF
Analog RGB reference resistor	R_{REF}	—	2.4	2.7	—	kΩ	Between VR0 and VSSR
Analog RGB output impedance	R_L	—	—	150	160	Ω	ROUT, GOUT, BOUT

• **MB91316/A**

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Current dissipation (upper : 1.8V lower : 3.3V)	I_{CCT}	Watch mode Ta = + 25 °C, fclk = 32 kHz	—	300	600	µA	Dot clock PLL stop USB clock stop
			—	700	1000		
	I_{CC}	Normal operation Ta = + 25 °C, fcp = 40 MHz, fcpp = 20 MHz	—	110	130	mA	Dot clock at 90 MHz
			—	110	140		
	I_{CCS}	Main sleep mode Ta = + 25 °C, fcp = 40 MHz, fcpp = 20 MHz	—	70	90	mA	Dot clock PLL stop
			—	70	100		
	I_{CCL}	Sub RUN mode Ta = + 25 °C, fclk = 32 kHz	—	400	800	µA	Dot clock PLL stop USB clock stop
			—	900	1300		
	I_{CCH}	Main stop mode Ta = + 25 °C, fclk = 0 kHz	—	150	500	µA	
			—	50	100		
		Ta = + 70 °C, fclk = 0 kHz	—	1200	5500	µA	
			—	300	500		
"H" level input voltage	V_{IH}	—	V_{CC} × 0.8	—	V_{CC}	V	
"L" level input voltage	V_{IL}	V_{CC} = 3.3 V	V_{SS}	—	V_{CC} × 0.2	V	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P74, P80 to P87, P90 to P97, PA0 to PA2, PB0 to PB4, PC0 to PC7, DCKI, VSYNC, HSYNC1 to HSYNC3
"H" level output voltage	V_{OH}	V_{CC} = 3.3 V, I_{OH} = − 4 mA	V_{CC} − 0.5	—	V_{CC}	V	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P74, P80 to P87, P90 to P97, PA0 to PA2, PB0 to PB4, PC0 to PC7, B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH

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Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
"L" level output voltage	V_{OL}	V_{CC} = 3.3 V, I_{OL} = 4 mA	V_{SS}	—	0.4	V	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P74, P80 to P87, P90 to P97, PA0 to PA2, PB0 to PB4, PC0 to PC7, B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
Input leak current	I_{IL}	—	− 5	—	+ 5	µA	
I^2C bus switch connection resistor	R_{BS}	—	—	—	130	Ω	Between SCL2 and SCL3 Between SDA2 and SDA3 Between SCL3 and SCL4 Between SDA3 and SDA4
Analog RGB reference voltage	V_{REF}	—	1.05	1.10	1.15	V	VREF
Analog RGB reference resistor	R_{REF}	—	2.4	2.7	—	kΩ	Between VR0 and VSSR
Analog RGB output impedance	R_L	—	—	150	160	Ω	ROUT, GOUT, BOUT

(2) USB

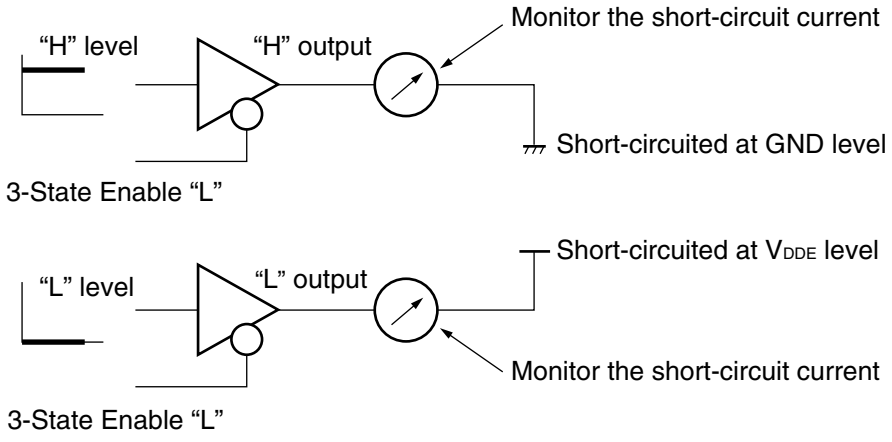
- DC Characteristics (1)

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	—	I_{OH} = − 100 µA	V_{DDE} − 0.2	—	V_{DDE}	V	
"L" level output voltage	V_{OL}	—	I_{OL} = 100 µA	0	—	0.2	V	
"H" level output current	I_{OH}	—	At Full Speed Mode V_{OH} = V_{DDE} − 0.4 V	− 20	—	—	mA	
			At Low Speed Mode V_{OH} = V_{DDE} − 0.4 V	− 6	—	—	mA	
"L" level output current	I_{OL}	—	At Full Speed Mode V_{OL} = 0.4 V	20	—	—	mA	
			At Low Speed Mode V_{OL} = 0.4 V	6	—	—	mA	
Output short-circuit current	I_{OS}	—	—	—	—	300	mA	*1
Input leak current	I_{LZ}	—	—	—	—	± 5	µA	*2

*1 : About the output short-circuit current I_{OS}

Output short-circuit current I_{OS} is the maximum current that flows when the output pin is connected to V_{DDE} or V_{SS} (within the maximum rating) .



About the output short-circuit current : The current is "the short-circuit current per differential output pin". As the USB I/O buffer is a differential output, the short-circuit current should be considered for both of the output pins.

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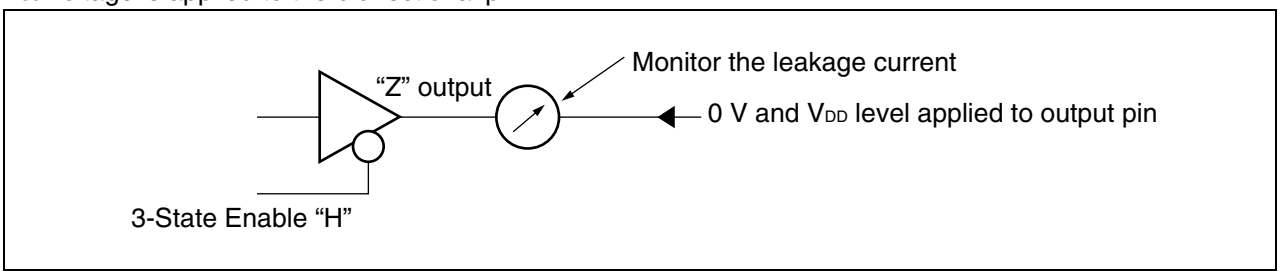
*2 : About measurement of “Z” leakage current I_{LZ}
Input leakage current I_{LZ} is measured with the USB I/O buffer in the high-impedance state when the V_{DDE} or V_{SS} voltage is applied to the bidirectional pin.



• DC Characteristics (2)

Conform to the USB Specification Revision 2.0 Full speed.

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Input Voltage :					
High (driven)	V_{IH}	2.0	—	V	*1
Low	V_{IL}	—	0.8	V	*1
Differential Input Sensitivity	V_{DI}	0.2	—	V	*2
Common Mode Input Voltage	V_{CM}	0.8	2.5	V	*2
Output Voltage :					
Low	V_{OL}	0.0	0.3	V	*3
High (driven)	V_{OH}	2.8	3.6	V	*3
Differential Output Signal Voltage	V_{CRS}	1.3	2.0	V	*4
Terminations :					
Pull-Up Resistor on Upstream Port	R_{PU}	1.425	1.575	kΩ	1.5 kΩ ± 5%
Pull-Down Resistor on Downstream Port	R_{PD}	1.425	1.575	kΩ	1.5 kΩ ± 5%
Termination voltage for upstream port pull-up	V_{TERM}	3.0	3.6	V	*5

*1 : About input voltage V_{IH}, V_{IL}

The switching threshold voltage of the USB I/O buffer's single-end receiver is set within the range from V_{IL} (Max) = 0.8 V to V_{IH} (Min) = 2.0 V (TTL input standard) .

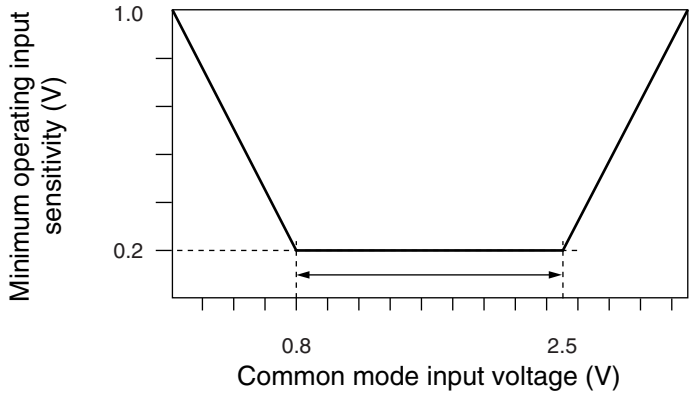
For V_{IH} and V_{IL}, the LSI has some hysteresis to reduce noise susceptibility.

*2 : About input voltage V_{DI}, V_{CM}

A differential receiver is used to receive USB differential data signals.

The differential receiver has a differential input sensitivity of 200 mV when the differential data input falls within the range from 0.8 V to 2.5 V with respect to the local ground reference level.

The above voltage range is referred to as common-mode input voltage range.



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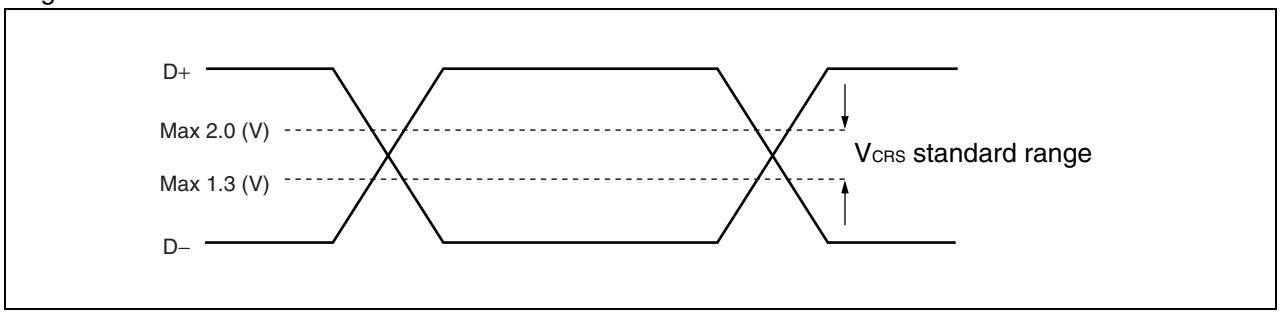
*3 : About output voltage V_{OL}, V_{OH}
The output driving performance levels of the driver are 0.3 V or less (to 3.6 V, 1.5 kΩ load) in the low state (V_{OL}) and 2.8 V or more (to ground, 1.5 kΩ load) in the high state (V_{OH}) .

*4 : About output voltage V_{CRS}
The cross voltage of the external differential output signals (D+ and D–) for the USB I/O buffer falls within the range from 1.3 V to 2.0 V.



*5 : About terminations V_{TERM}
V_{TERM} indicates the pull-up voltage at the upstream port.

4. AC Characteristics

(1) Clock Timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Clock frequency	f_C	X0, X1	—	9.0	10.2	MHz	PLL system (operation at a maximum internal speed of 40 MHz by quadrupling a self-oscillation frequency of 10 MHz via PLL)
Internal operating clock frequency	f_{CP}	—	—	2.25*	40.8	MHz	CPU system ($t_{CP} = 1/f_{CP}$)
	f_{CPP}			2.25*	20.4	MHz	Peripheral system ($t_{CPP} = 1/f_{CPP}$)
	f_{CPT}			2.25*	20.4	MHz	External bus system ($t_{CPT} = 1/f_{CPT}$)

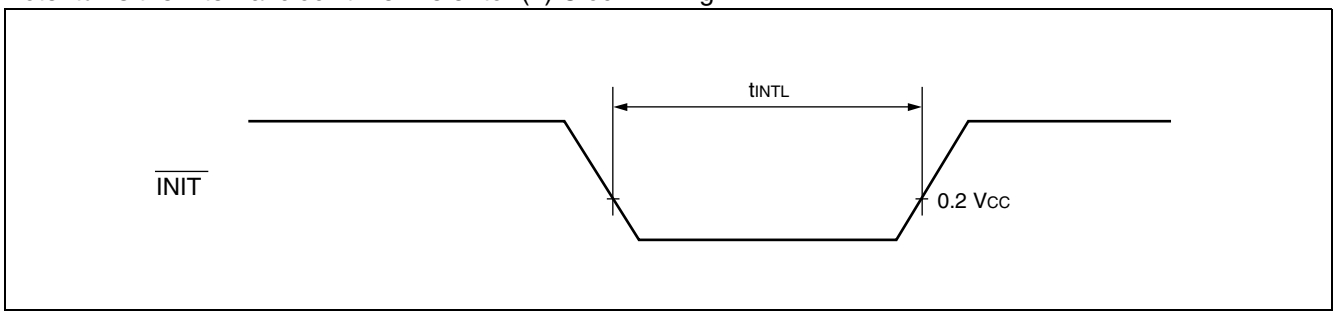
* : The numeric value when inputting the 9 MHz (the minimum clock frequency) to X0 and using the PLL system and the gear ratio 1/16 of the oscillation circuit.

(2) Reset Input

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condi-tions	Value		Unit
				Min	Max	
INIT input time (at power-on)	t_{INTL}	$\overline{INIT}$	—	20 + α	—	µs
INIT input time (other than at power-on)				$t_{CP} \times 10$	—	ns
INIT input time (at returning from stop)				20 + α	—	µs

Note: t_{CP} is the internal clock time. Refer to “(1) Clock Timing”.



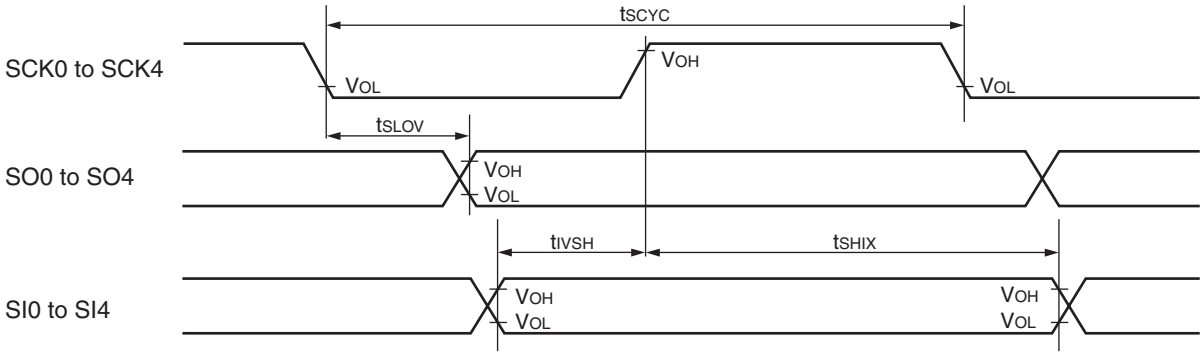
(3) UART Timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

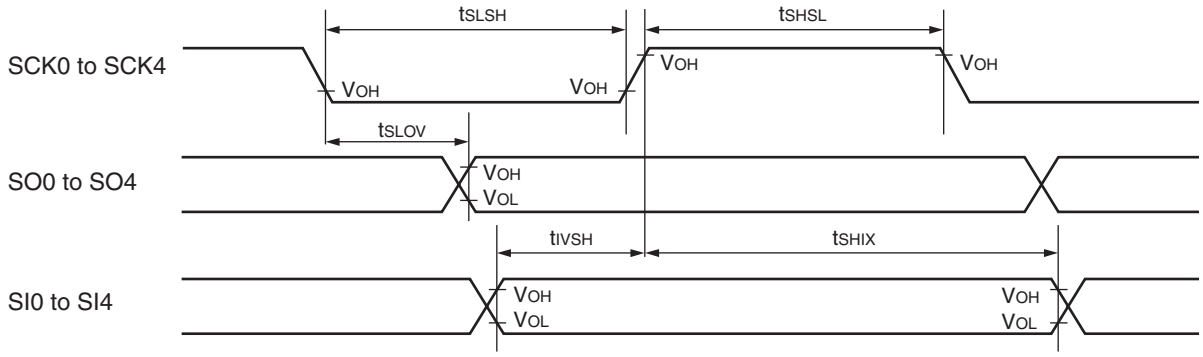
Parameter	Symbol	Pin	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal shift lock mode	8 t_{CPP}	—	ns
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK4, SO0 to SO4		− 80	+ 80	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SI0 to SI4		100	—	ns
SCK ↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK4, SI0 to SI4		60	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK4	External shift lock mode	4 t_{CPP}	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK4		4 t_{CPP}	—	ns
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK4, SO0 to SO4		—	150	ns
Valid SI → SCK ↑	t_{IVSH}	SCK0 to SCK4, SI0 to SI4		60	—	ns
Valid SCK ↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK4, SI0 to SI4		60	—	ns

Notes : • t_{CPP} indicates the peripheral clock cycle time. Refer to “(1) Clock Timing”.
• The above specifications are for the CLK synchronous mode.

• Internal shift clock mode



• External shift clock mode

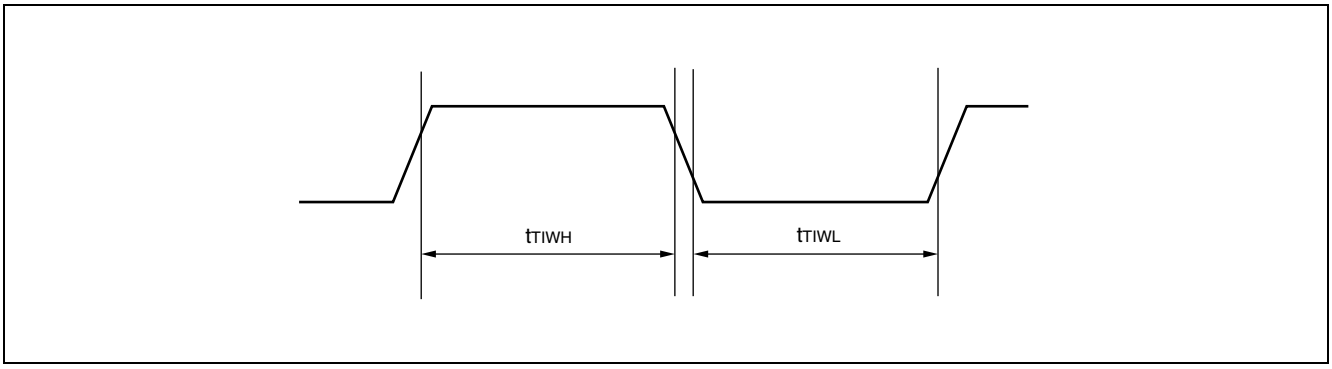


(4) Reload timer clock , PPG timer input, multi-functional timer input timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2, PPG0 to PPG3, TRG0 to TRG3, TMI0 to TMI3	—	2 t_{CPP}	—	ns

Note : t_{CPP} indicates the peripheral clock cycle time. Refer to “(1) Clock Timing”.



(5) Trigger Input Timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

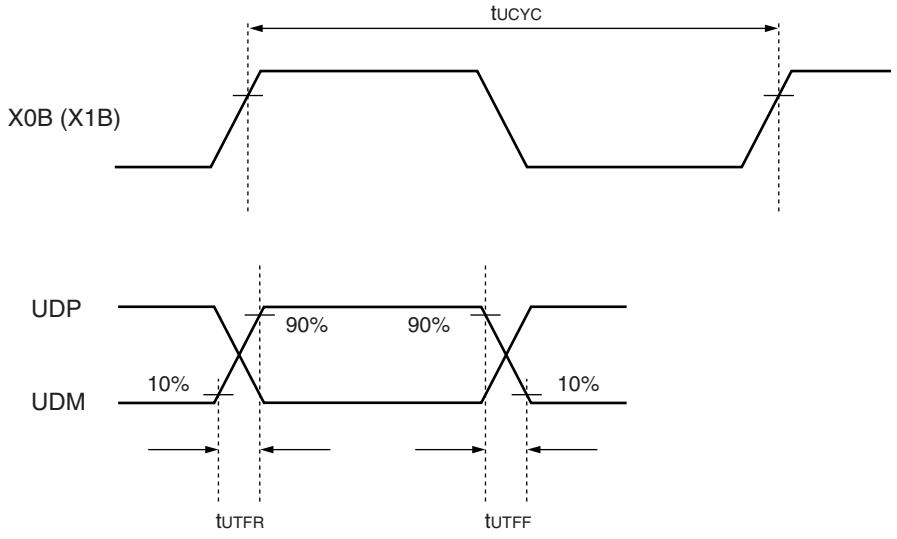
Parameter	Symbol	Pin	Conditions	Value		Unit
				Min	Max	
A/D activation trigger input time	t_{ATGX}	ATRG	—	5 t_{CPP}	—	ns

Note : t_{CPP} indicates the peripheral clock cycle time. Refer to “(1) Clock Timing”.

(6) USB interface

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input clock frequency	t_{UCYC}	X0B, X1B	—	—	48*1	—	MHz	Self-oscillation 500 ppm accuracy *1 t_{UCYC} = 1 / f_{UCYC}
		X0B	—					External input 500 ppm accuracy *1 t_{UCYC} = 1 / f_{UCYC}
Rise Time	t_{UTFR}	UDP/ UDM	At Full Speed Mode	4	—	20	ns	*2
Fall Time	t_{UTFF}	UDP/ UDM	At Full Speed Mode	4	—	20	ns	*2
Differential Rise and Fall Timing Matching	—	UDP/ UDM	At Full Speed Mode	90	—	111.11	%	*2
Driver Output Resistor	—	UDP, UDM	—	28	—	44	Ω	*3



*1 : The AC characteristics of the USB interface conform to USB Specification Revision 2.0 Full speed.

*2 : About driver characteristics t_{UTFR}, t_{UTFF}, t_{UTFRFM}
These items specify the differential data signal rise (Rise Time) and fall (Fall time) times.
These are defined as the times between 10% to 90% of the output signal voltage.
For the full-speed buffer, t_{UTFR} and t_{UTFF} are specified such that the t_{UTFR}/t_{UTFF} ratio falls within ±10% to minimize RFI radiation.

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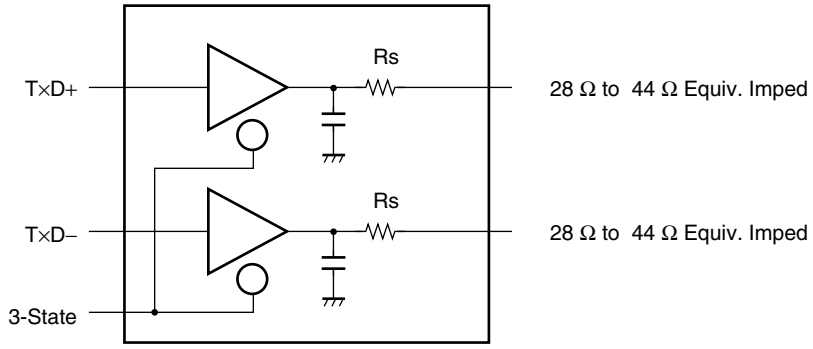
*3 : About driver characteristics ZDRV

USB full-speed connection is performed via a shielded twisted-pair cable at a characteristic impedance of 90 Ω ± 15%. The USB Standard stipulates that the USB driver's output impedance must be within the range of 28 Ω to 44 Ω. The USB Standard also stipulates that a discrete serial resistor (Rs) must be added to have balance while satisfying the above standard.

The output impedance of the USB I/O buffer on this LSI is about 3 Ω to 19 Ω. Therefore, serial resistor R_S to be added must be 25 Ω to 30 Ω (27 Ω recommended) .



Driver output impedance 3 Ω to 19 Ω
Rs serial resistor: 25 Ω to 30 Ω
Add a serial resistor of preferably 27 Ω

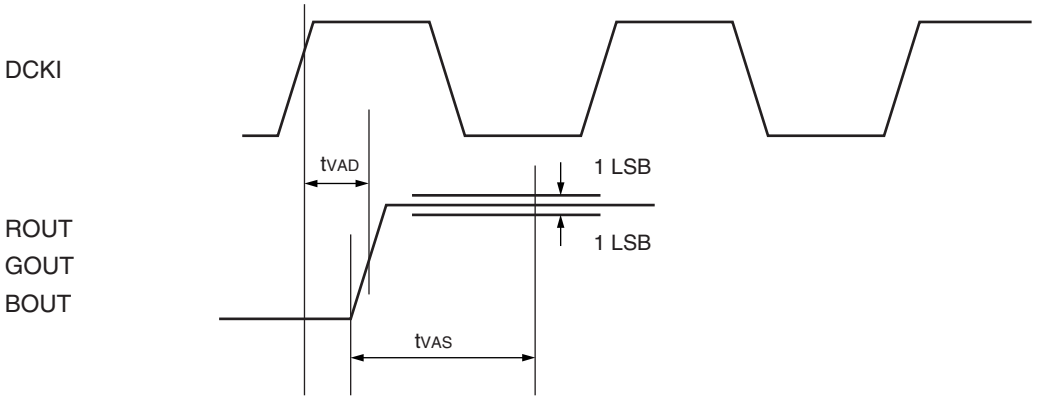
(7) Analog RGB

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB output delay	t_{VAD}	ROUT, GOUT, BOUT	V_{REF} = 1.1 V, V_{DDR} = V_{DDG} = V_{DDB} = 2.5 V, VRO* = 2.7 kΩ	—	12	—	ns	50 MHz (Max)
Analog RGB output settling time	t_{VAS}	ROUT, GOUT, BOUT		—	—	20	ns	

* : VRO is an external resistor for DAC.

- Display signal output timing



(8) Digital RGB

Vertical synchronous, horizontal synchronous, and display output control signal input timing

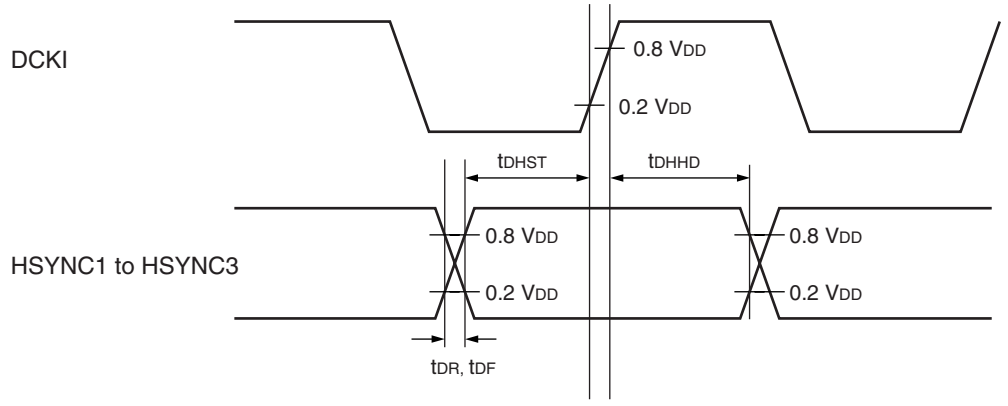
(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Horizontal sync signal cycle time	t_{HCYC}	HSYNC1 to HSYNC3	100 + t_{WH}	—	Dot clock	
Horizontal sync signal pulse width	t_{WH}	HSYNC1 to HSYNC3	20	—	Dot clock	*1
			—	6	µs	
Horizontal sync signal setup time	t_{DHST}	HSYNC1 to HSYNC3	4	—	ns	
Horizontal sync signal hold time	t_{DHHD}		0	—	ns	
Vertical sync signal setup time	t_{HVST}	VSYNC	5	1H*2 – 5	Dot clock	
Vertical sync signal hold time	t_{HVHD}		3	—	H*2	
Input sync signal rise/fall time	t_{DR} t_{DF}	HSYNC1 to HSYNC3, VSYNC	—	2	ns	

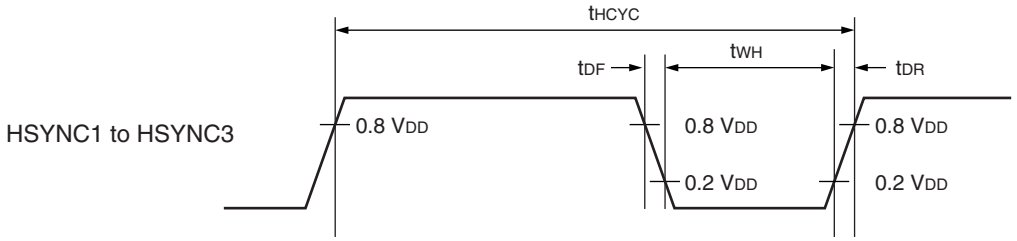
*1 : During the horizontal sync signal pulse period, the device stops its internal OSDC operation, disabling writing to the internal VRAM. Therefore, set the horizontal sync signal pulse width and VRAM write cycle to ensure that : horizontal sync signal pulse width < VRAM write cycle.
Precisely, adjust the command issuance interval not to issue command 2 or command 4 (VRAM write command) more than twice in the horizontal sync signal pulse width period.
If the above condition is not satisfied, the device may fail writing to VRAM.

*2 : 1H is assumed to be one horizontal sync signal period.

- Horizontal sync signal, display output control signal input timing

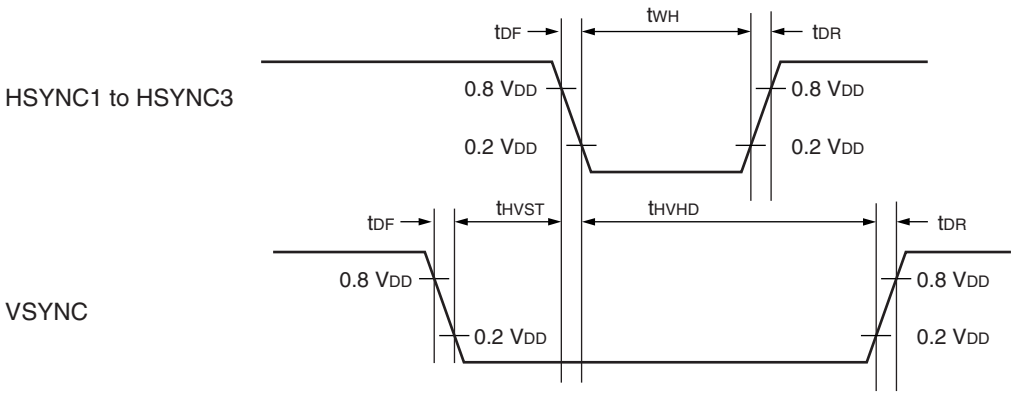


• Horizontal sync signal input

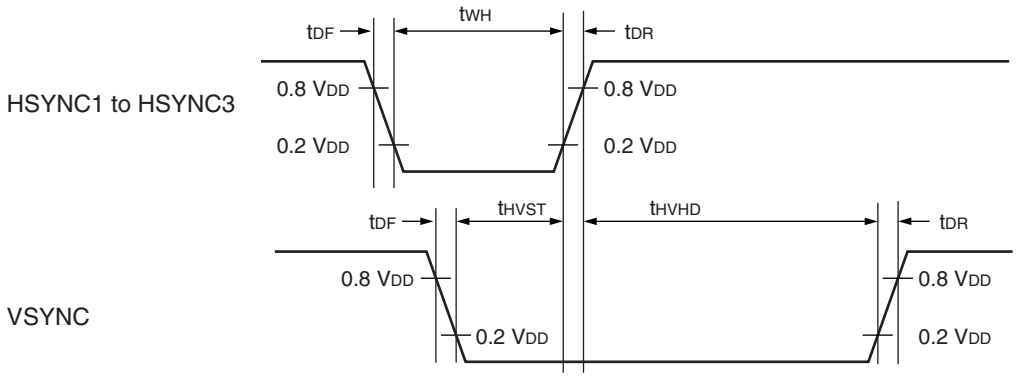


• Vertical sync signal input timing

  • VSYNC detection at the leading edge of HSYNC



  • VSYNC detection at the trailing edge of HSYNC



(9) Display signal timing

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

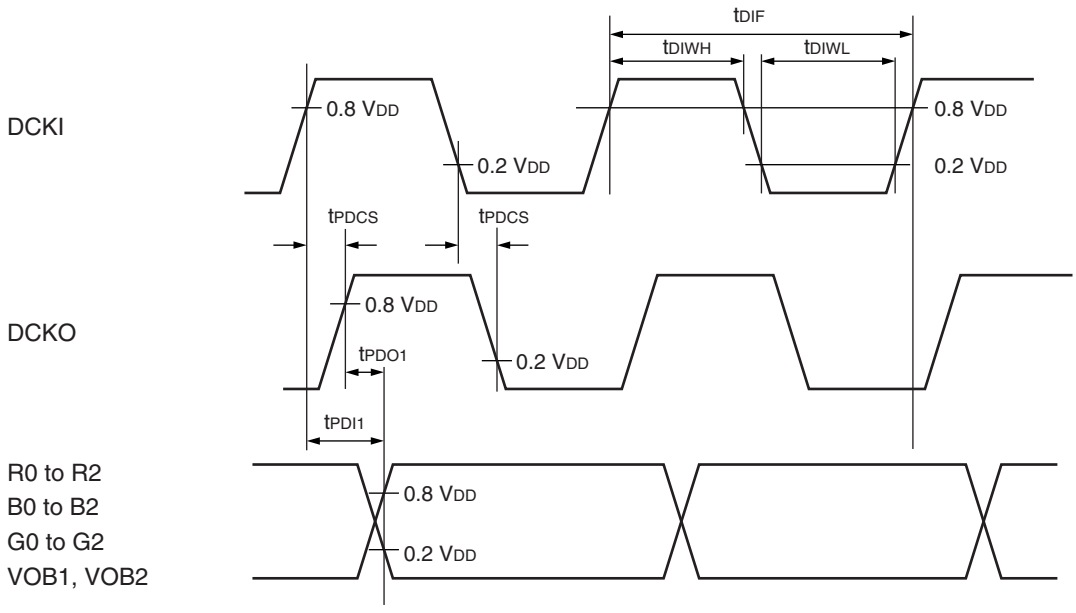
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Dot clock cycle time	t_{DIF}	DCKI	11	90	MHz	*1
Dot clock pulse time	t_{DIWH}	DCKI	5	—	ns	*1
	t_{DIWL}		5	—	ns	
Dot clock output delay time 1	t_{PDCS}	DCKO	3	8	ns	*2
Display signal output delay time I1	t_{PDI1}	R0 to R2, B0 to B2, G0 to G2, VOB1, VOB2	2	8	ns	*2
Display signal output delay time O1	t_{PDO1}	R0 to R2, B0 to B2, G0 to G2, VOB1, VOB2	− 4	+ 5	ns	*2

*1 : Input a continuous dot clock signal without a break.

*2 : Output load 16 pF

Note : The actual display output varies depending on how the display output/position is controlled for each display layer.

- Display signal output timing



(10-a) External circuit for data slicer

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit
			Min	Typ	Max	
Video signal input level	V_{VIN}	VIN0, VIN1	1.0	—	1.5	Vp-p

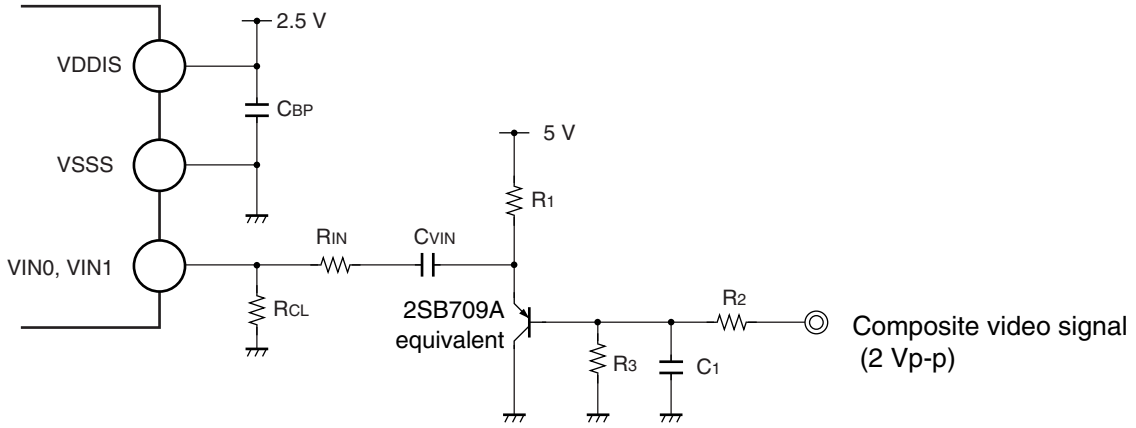
(10-b) External circuit for data slicer

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

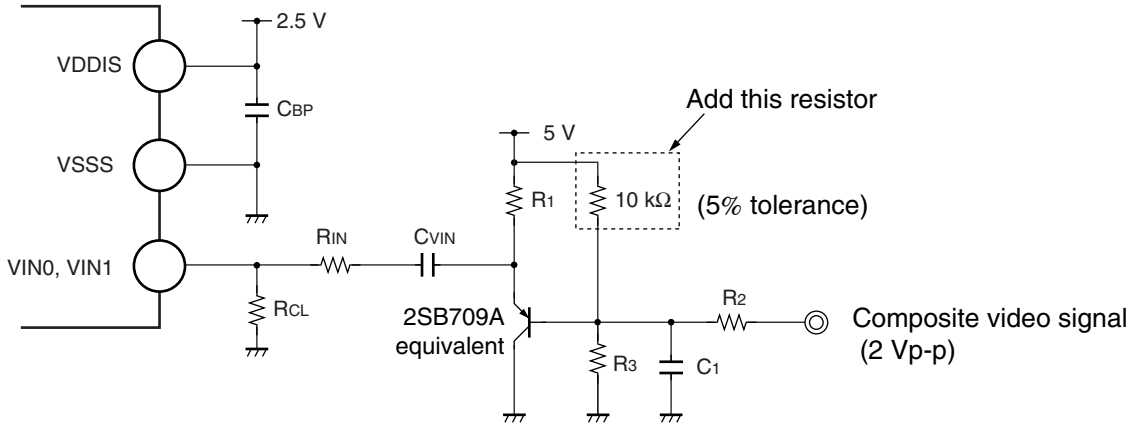
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Coupling capacitor for VIN pin	C_{VIN}	VIN0, VIN1	—	—	0.1	µF	Ceramic capacitor with B rating or higher, 10% tolerance
Clamping resistor	R_{CL}	VIN0, VIN1	—	—	1	MΩ	5% tolerance
Input resistor for VIN pin	R_{IN}	VIN0, VIN1	—	—	0	Ω	5% tolerance
Low-pass filter capacitor for VIN	C_1	—	—	—	82	pF	Ceramic capacitor with B rating or higher, 10% tolerance
Power supply bypass capacitor	C_{BP}	VDDIS, VSSS	—	—	0.1	µF	Ceramic capacitor
Resistor for video signal input buffer	R_1	—	—	—	2.2	kΩ	5% tolerance
Video signal input level correcting resistor	R_2	—	—	—	4.7	kΩ	5% tolerance
Video signal input level correcting resistor	R_3	—	—	10	12	kΩ	5% tolerance

External recommended circuit for data slicer

(1) When the input composite video signals have been DC clamped



(2) When the input composite video signals have not been DC clamped



(11) I²C timing

- At master mode operating

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 kΩ C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs	
Bus free time between [STOP condition] and [START condition]	t_{BUS}		4.7	—	1.3	—	µs	
SCL↓ → SDA output delay time	t_{DLDAT}		—	5 × M*1	—	5 × M*1	ns	
Setup time of [repeat START condition] SCL↑ → SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs	
Hold time of [repeat START condition] SDA↓ → SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL↑ → SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs	
SDA data input hold time (vs. SCL↓)	t_{HDDAT}		2 × M*1	—	2 × M*1	—	µs	
SDA data input setup time (vs. SCL↑)	t_{SUDAT}		250	—	100*2	—	ns	

*1 : M = Resource clock cycle (ns)

*2 : A Fast-mode I²C bus device can be used for a standard mode I²C bus system as long as the device satisfies a requirement of "$t_{SUDAT} \geq 250$ ns".
When the device does not extend the "L" period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

- At slave mode operating

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 kΩ C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t_{LOW}		4.7	—	1.3	—	µs	
"H" period of SCL clock	t_{HIGH}		4.0	—	0.6	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}		—	5 × M*1	—	5 × M*1	ns	
Bus free time between [STOP condition and START condition]	t_{BUS}		4.7	—	1.3	—	µs	
SDA data input hold time (vs. SCL↓)	t_{HDDAT}		2 × M*1	—	2 × M*1	—	µs	
SDA data input setup time (vs. SCL↑)	t_{SUDAT}		250	—	100*2	—	ns	
Setup time of [repeat START condition] SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs	
Hold time of [repeat START condition] SDA ↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs	

*1 : M = Resource clock cycle (ns)

*2 : A Fast-mode I²C bus device can be used for a standard mode I²C bus system as long as the device satisfies a requirement of "$t_{SUDAT} \geq 250$ ns".
When the device does not extend the "L" period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

5. Power-on Sequence

- The power supplies must be turned on in the VDDI → AVCC, AVRH, VDDE order and off in the VDDE → AVCC, AVRH, VDDI order.
- Turn on V_{DDE} before applying on the analog power supply AV_{CC} and the analog signal.

6. Electrical Characteristics for the A/D Converter

(Ta = − 10 °C to + 70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, V_{SSE} = V_{SSI} = AV_{SS} = 0 V, AVRH = 3.0 V to 3.6 V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	− 5.5	—	+ 5.5	LSB	AV_{CC} = 3.3 V, AVRH = 3.3 V (at CPU sleep)
Nonlinear error*1	− 3.5	—	+ 3.5	LSB	
Differential linear error*1	− 2.0	—	+ 2.0	LSB	
Zero transition voltage*1	− 4.0	—	+ 6.0	LSB	
Full transition voltage*1	AVRH − 5.5	—	AVRH + 3.0	LSB	
Conversion time	8.5*2	—	—	µs	
Power supply voltage (analog + digital)	—	—	3.3	mA	
Reference power supply current (between AVRH and AVRL)	—	—	100	µA	
Analog input capacitance	—	—	27	pF	
Interchannel disparity	—	—	4	LSB	

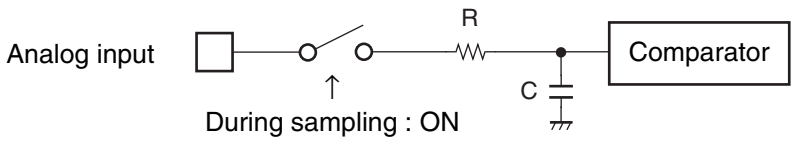
*1 : Measured in the CPU sleep state

*2 : Depends on the clock cycle of the clock signal supplied to peripheral resources.

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.
  Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance
  and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.
  If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input circuit

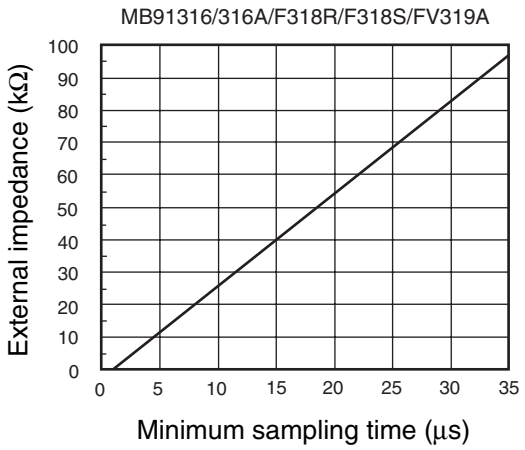


	R	C
MB91316/316A/F318R MB91F318S/FV319R	5 kΩ (Max)	27 pF (Max)

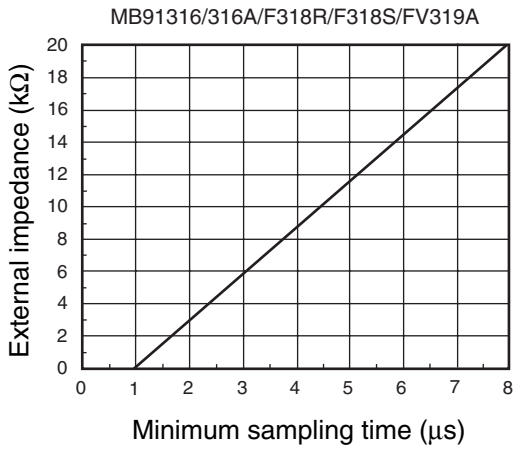
Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

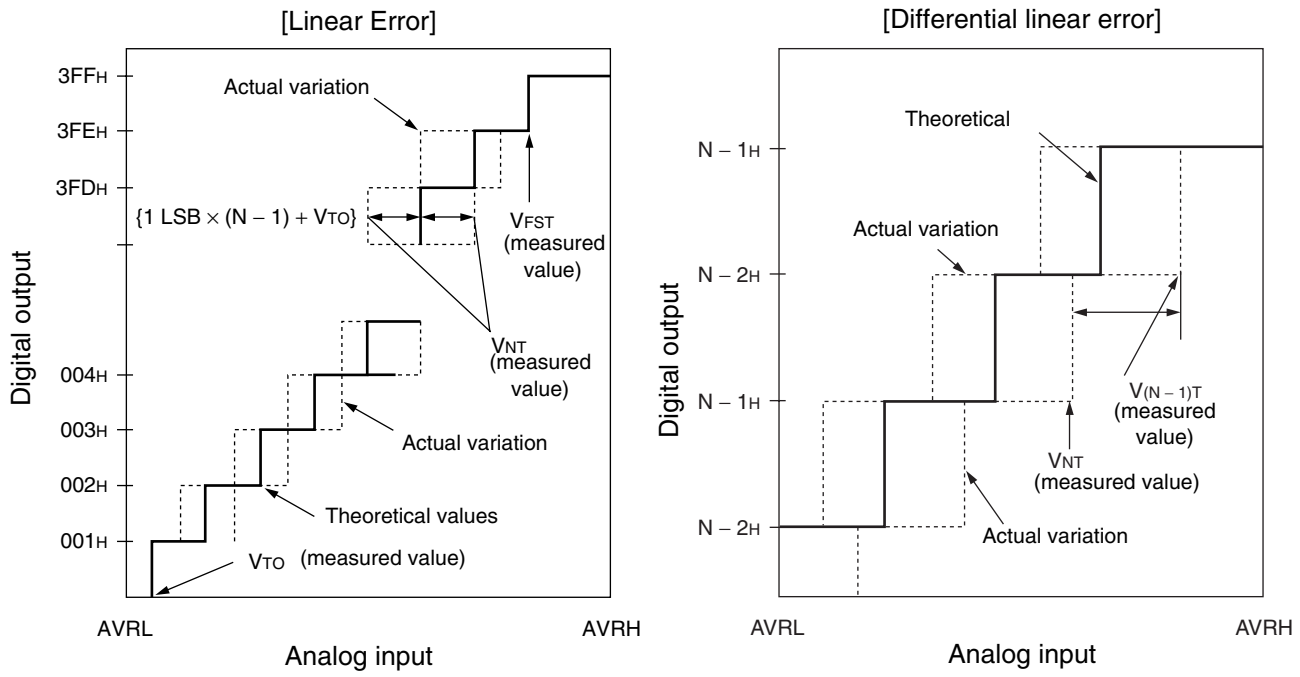


• About errors

- As |AVRH – AVSS| becomes smaller, values of relative errors grow larger.

Definition of A/D Converter Terms

- Resolution
  Indicates the ability of the A/D converter to discriminate analog variation
- Linear error
  Expresses the deviation between actual conversion characteristics and a straight line connecting the device's zero transition point (00 0000 0000←→00 0000 0001) and full scale transition point (11 1111 1110←→ 11 1111 1111)
- Differential linear error
  Expresses the deviation of the logical value of input voltage required to create a variation of 1 LSB in output code.



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$$1\ \text{LSB}'' = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}] \quad \text{(theoretical value)}$$

N : A/D converter digital output value

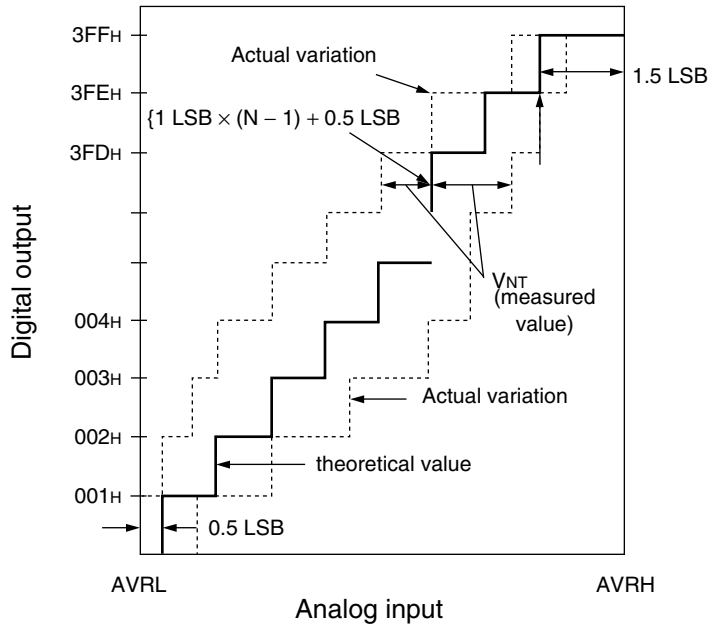
V_{OT} : Voltage at which the digital output transitions from "000"H to "001"H.

V_{FST} : Voltage at which the digital output transitions from "3FE"H to "3FF"H.

V_{NT} : Voltage at which the digital output transitions from (N-1) to N.

- Total error
  Expresses the difference between actual and theoretical values as error, including zero transition error, full-scale error, and linearity error.

[Total error]



$$\text{Total error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB}'' \times (N - 1) + 0.5\ \text{LSB}''\}}{1\ \text{LSB}''}\ [\text{LSB}]$$

N : A/D converter digital output value

V_{OT}" (theoretical value) = AVRL + 0.5 LSB" [V]

V_{FST}" (theoretical value) = AVRH – 1.5 LSB" [V]

V_{NT} : Voltage at which digital output transitions from (N-1) to N.

■ FLASH MEMORY PROGRAM/ERASE CHARACTERISTICS

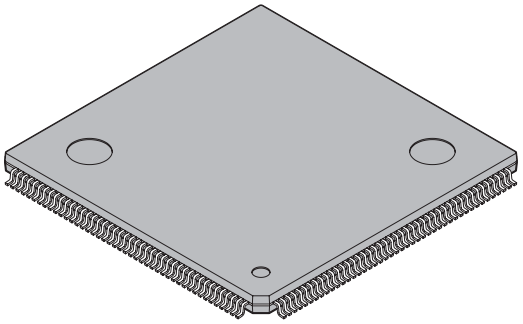
(V_{CC} = 3.3 V, Ta = + 25 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.5	2.0	s	Excludes 00_H programming prior erasure.
Byte programming time	—	6	100	µs	Excludes system-level overhead.
Chip programming time	—	3.4	56	s	Excludes system-level overhead.
Erase/program cycle	10000	—	—	cycle	

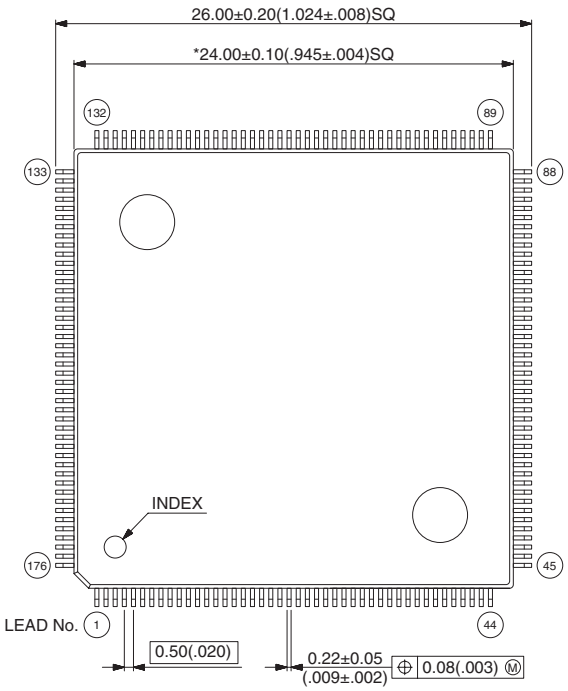
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91FV319RPMC-ESE1	176-pin plastic LQFP (FPT-176P-M07)	For development tool
MB91F318RPMC-G-XXXE1	176-pin plastic LQFP (FPT-176P-M07)	With CC decoder. Without Fujitsu Flash programming.
MB91F318RPMC-GXXX-XXXXE1	176-pin plastic LQFP (FPT-176P-M07)	With CC decoder. With Fujitsu Flash programming.
MB91F318SPMC-G-XXXE1	176-pin plastic LQFP (FPT-176P-M07)	Without CC decoder. Without Fujitsu Flash programming.
MB91F318SPMC-GXXX-XXXXE1	176-pin plastic LQFP (FPT-176P-M07)	Without CC decoder. With Fujitsu Flash programming.
MB91316PMC-G-XXXE1	176-pin plastic LQFP (FPT-176P-M07)	Without CC decoder.
MB91316APMC-G-XXXE1	176-pin plastic LQFP (FPT-176P-M07)	With CC decoder.

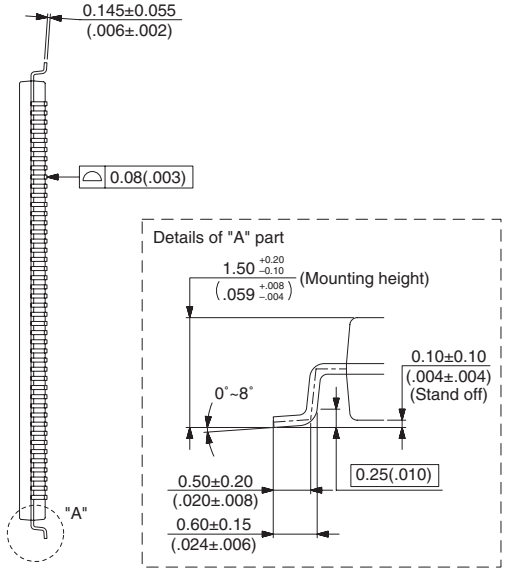
■ PACKAGE DIMENSION

176-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP-0176-2424-0.50
(FPT-176P-M07)		

176-pin plastic LQFP
(FPT-176P-M07)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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