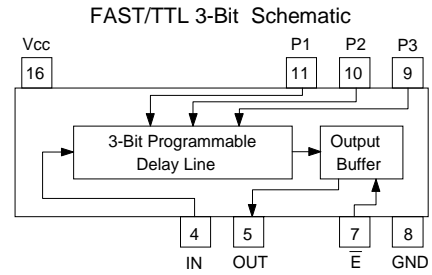


3-Bit Programmable Delay Modules

PLDM4 Series FAST/TTL Logic

7 Delay Steps -- 4 ns Inherent Delay

Available in Surface Mount



Electrical Specifications at 25°C

3-Bit FAST Part Number	Delay per Step (ns)	Error ref. to 000 (ns)	Initial Delay (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)							
				000	001	010	011	100	101	110	111
PLDM4-0.5	0.5 ± .25	± .30	4 ± 1.0	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
PLDM4-0.7	0.7 ± .30	± .40	4 ± 1.0	0.0	0.7	1.4	2.1	2.8	3.5	4.2	4.9
PLDM4-0.8	0.8 ± .30	± .50	4 ± 1.0	0.0	0.8	1.6	2.4	3.2	4.0	4.8	5.6
PLDM4-1	1.0 ± .4	± .50	4 ± 1.0	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
PLDM4-1.2	1.2 ± .4	± .60	4 ± 1.0	0.0	1.2	2.4	3.6	4.8	6.0	7.2	8.4
PLDM4-1.25	1.25 ± .5	± .70	4 ± 1.0	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75
PLDM4-1.3	1.3 ± .5	± .70	4 ± 1.0	0.0	1.3	2.6	3.9	5.2	6.5	7.8	9.1
PLDM4-1.5	1.5 ± .5	± .70	4 ± 1.0	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5
PLDM4-1.8	1.8 ± .6	± .80	4 ± 1.0	0.0	1.8	3.6	5.4	7.2	9.0	10.8	12.6
PLDM4-2	2.0 ± .7	± .80	4 ± 1.0	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0
PLDM4-2.5	2.5 ± .7	± .90	4 ± 1.0	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5
PLDM4-2.6	2.6 ± .7	± .90	4 ± 1.0	0.0	2.6	5.2	7.8	10.4	13.0	15.6	18.2
PLDM4-3	3.0 ± .7	± 1.0	4 ± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0

CUMULATIVE TOLERANCES: "Error" Tolerance is for Programmed Delays referenced to Initial Delay, Setting "000." For example, the setting "111" delay of PLDM4-10 is 70.0 ± 3.0ns ref. to "000," and 74.0 ± 4.0ns referenced to the input.

ENABLE input (Pin 7) is active low. Output will be disabled (low) when " \bar{E} " is high.

INPUT FAN-IN: Input, pin 4, is loaded by the internal passive network and 8 gate inputs (74F type). The source driving Pin 4 should be FAST/TTL (74S/74F) type or equivalent, and should not be used to drive any load other than the delay line input.

TEST CONDITIONS -- FAST / TTL

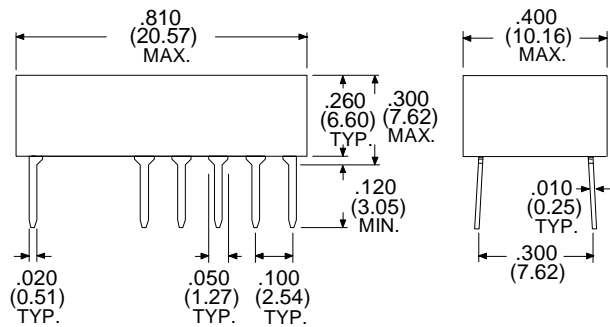
- V_{CC} Supply Voltage 5.00VDC
- Input Pulse Voltage 3.20V
- Input Pulse Rise Time 3.0 ns max.
- Input Pulse Width / Period 1000 / 2000 ns
- 1. Measurements made at 25°C
- 2. Delay Times measured at 1.50V level of leading edge.
- 3. Rise Times measured from 0.75V to 2.40V.
- 4. 10pf probe and fixture load on output.

OPERATING SPECIFICATIONS

- V_{CC} Supply Voltage 5.00 ± 0.25 VDC
- I_{CC} Supply Current 60 mA typ., 80 mA max
- Logic "1" Input *: V_{IH} 2.00 V min., 5.50 V max.
- I_{IH} 50 μA max. @ 2.70V
- Logic "0" Input *: V_{IL} 0.80 V max.
- I_{IL} -0.6 mA mA
- V_{OH} Logic "1" Voltage Out 2.40 V min.
- V_{OL} Logic "0" Voltage Out 0.50 V max.
- P_{WI} Input Pulse Width 40% of Delay min.
- Operating Temperature Range -0° to +70°C
- Storage Temperature Range -65° to +150°C

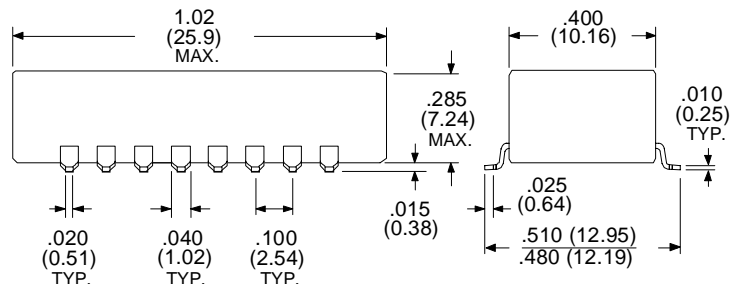
* Refer to "INPUT FAN-IN" note above.
IIL/IIH specified for Programming pins 9, 10 & 11.

Dimensions in Inches (mm)



16-Pin SMD Pkg. Unused leads are NOT removed.

To Specify SMD Package, Add "G" Suffix to P/N
Examples: PLDM4-1.25G, PLDM4-2G



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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