

RoHS Compliant Product

Description

The SPNE555 is a highly stable timer IC that can be operated in astable mode and monostable mode.
For monostable mode: time delay is controlled by one external resistor and one capacitor.
For stable mode: frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

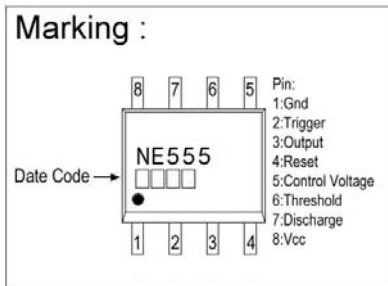
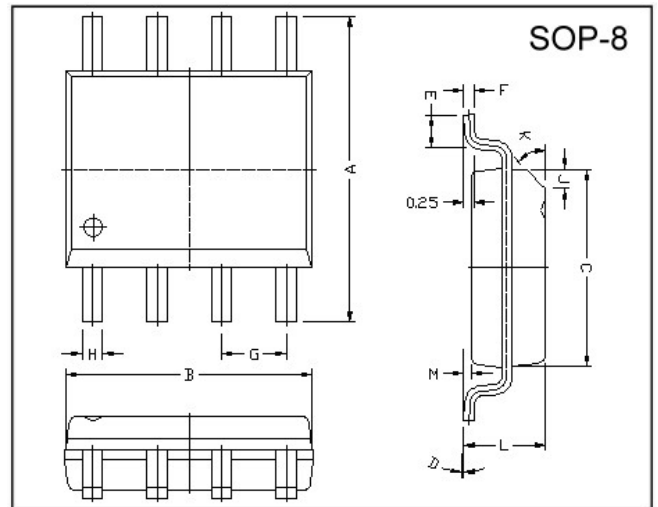
Features

- High current driver capability (=200mA)
- Adjustable duty cycle
- timing from μsec to hours
- turn off time less than $2\mu\text{sec}$

Applications

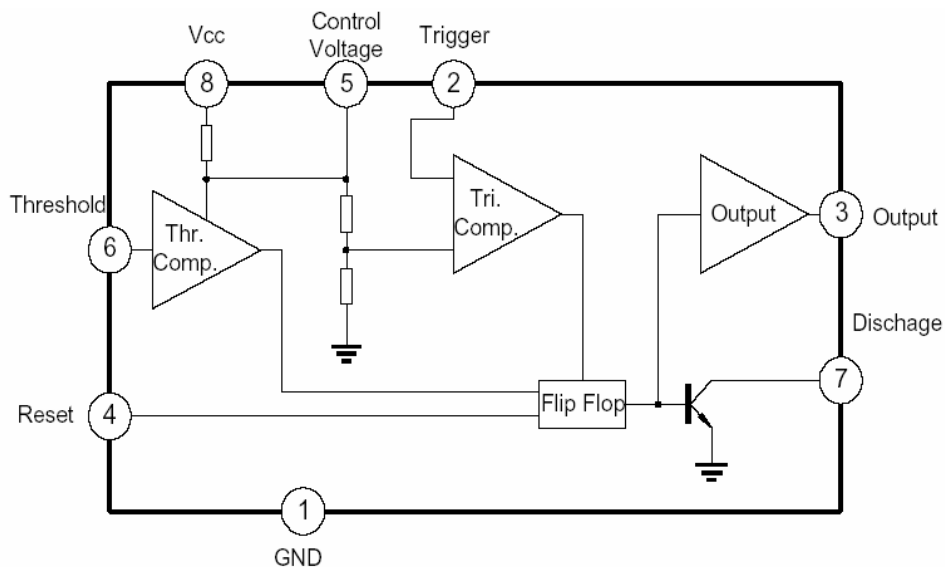
- Precision timing
- Pulse generation
- Time delay generation

Package Dimensions



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Block Diagram and Simplified Application & Pin Configuration



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Value	Units
Supply Voltage	V _{CC}	16	V
Differential Input Voltage	I _O	200	mA
Input Voltage	T _{lead}	300	°C
Power Dissipation	P _D	440	mW
Operating, Storage Temperature	T _{OPR} , T _{STG}	0~70, -65~150	°C

Electrical Characteristics (Ta = 25 °C, V_{CC} = 5 ~ 15V)

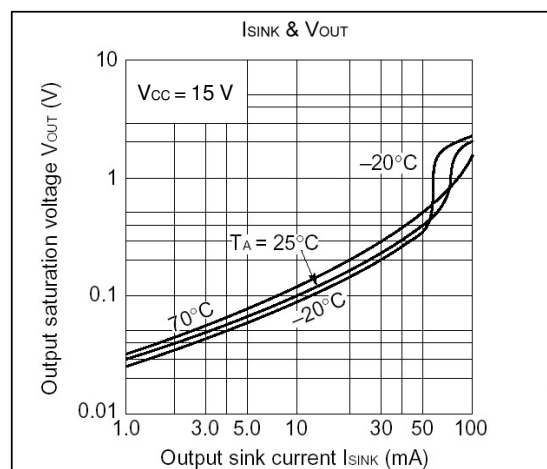
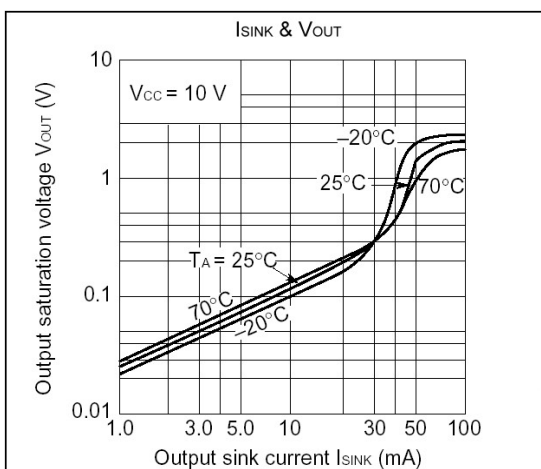
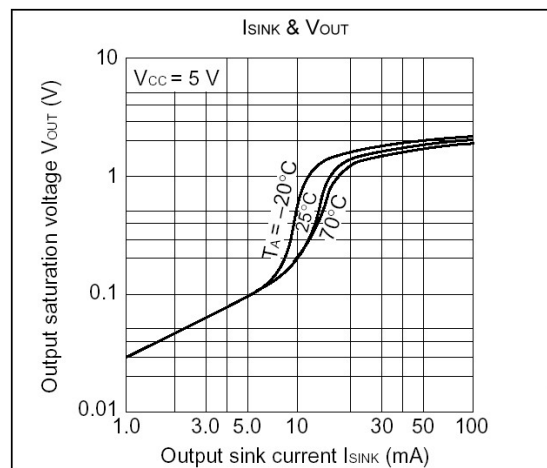
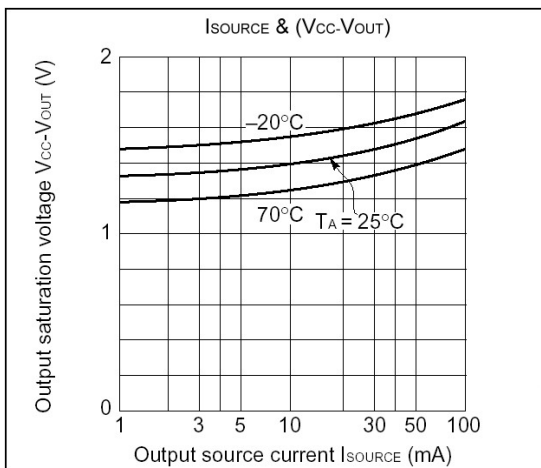
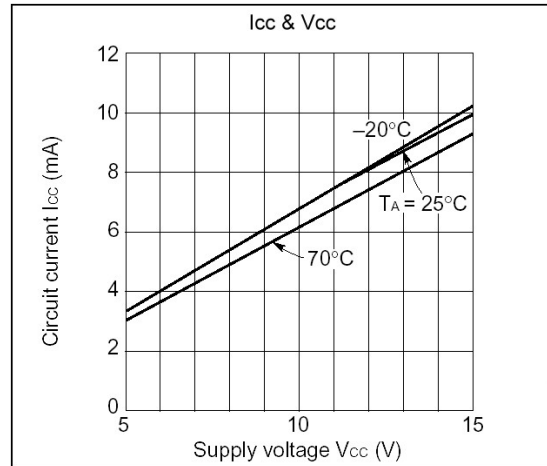
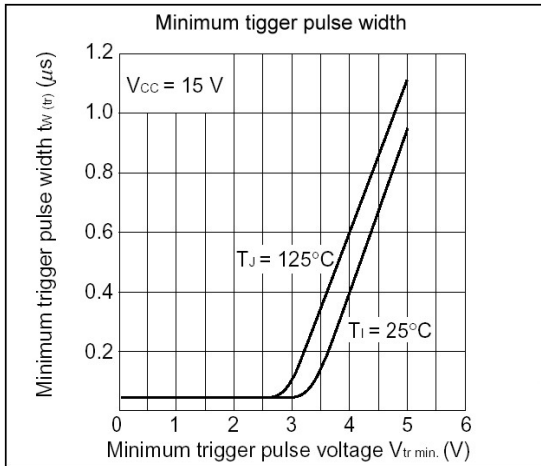
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage	V _{CC}		4.5	-	16	V
Supply Current (Note 1)	I _{CC}	V _{CC} = 5V, R _L = ∞	-	3	6	mA
		V _{CC} = 15V, R _L = ∞	-	10	15	mA
Timing Error (monostable)						
Initial Accuracy (Note 1)	A _{CCUR}	R _A = 1k ~ 100kΩ	-	1.0	-	%
Drift with Temperature	Δt/ΔT	C = 0.1 μF	-	50	-	ppm/°C
Drift with Supply Voltage	Δt/ΔV _{CC}		-	0.1	-	%/V
Timing Error (astable)						
Initial Accuracy (Note 1)	A _{CCUR}	R _A = 1k ~ 100kΩ	-	2.25	-	%
Drift with Temperature	Δt/ΔT	C = 0.1 μF	-	150	-	ppm/°C
Drift with Supply Voltage	Δt/ΔV _{CC}		-	0.3	-	%/V
Control Voltage	V _C	V _{CC} = 15V	9.0	10.0	11.0	V
		V _{CC} = 5V	2.6	3.33	4.0	
Threshold Voltage	V _{TH}	V _{CC} = 15V	9.2	10.0	10.8	V
		V _{CC} = 5V	3.1	3.33	3.55	
Threshold Current (Note 3)	I _{TH}		-	0.1	0.25	μA
Trigger Voltage	V _{tr}	V _{CC} = 5V	1.1	1.67	2.2	V
		V _{CC} = 15V	4.5	5	5.6	
Trigger Current	I _{tr}	V _{tr} = 0	-	-	2.0	μA
Reset Voltage	V _{rst}		0.4	0.7	1.0	V
Reset Current	I _{rst}		-	0.1	0.4	mA
Low Output Voltage	V _{OL}	V _{CC} = 15V, I _{sink} = 10mA	-	0.06	0.25	V
		V _{CC} = 15V, I _{sink} = 50mA	-	0.3	0.75	
		V _{CC} = 5V, I _{sink} = 5mA	-	0.05	0.35	
High Output Voltage	V _{OH}	V _{CC} = 15V, I _{sink} = 200mA	-	12.5	-	V
		V _{CC} = 15V, I _{sink} = 100mA	12.75	13.3	15	
		V _{CC} = 5V, I _{sink} = 100mA	2.75	3.3	5	
Reset Time of Output	t _R		-	100	-	nSec
Fall Time of Output	t _F		-	100	-	nSec
Discharge leakage Current	I _{LKG}		-	20	100	nA

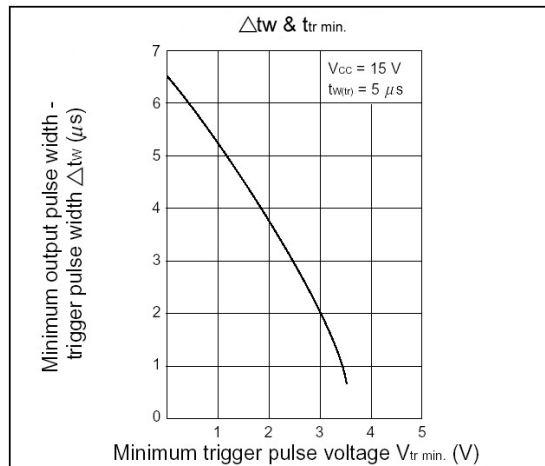
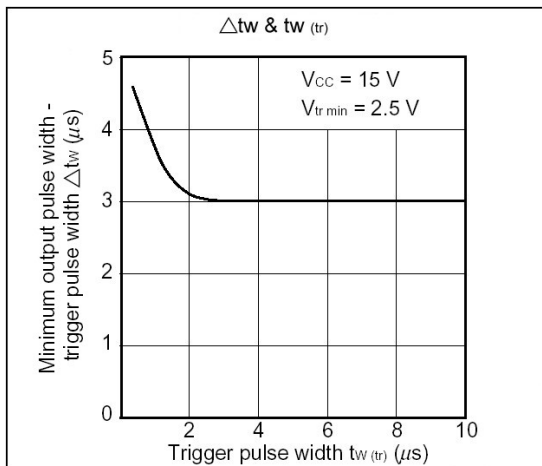
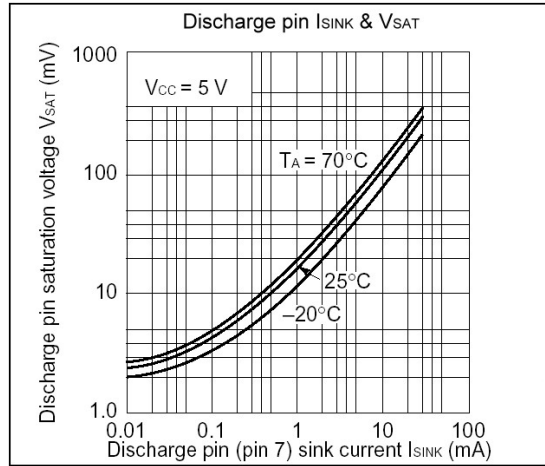
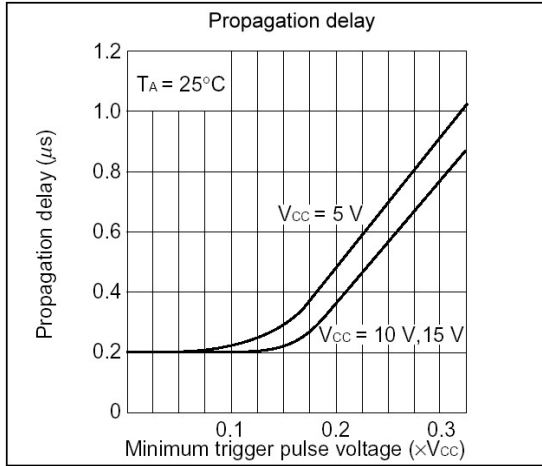
Note 1: Supply current when output is high typically 1 mA less at V_{CC} = 5V

Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.

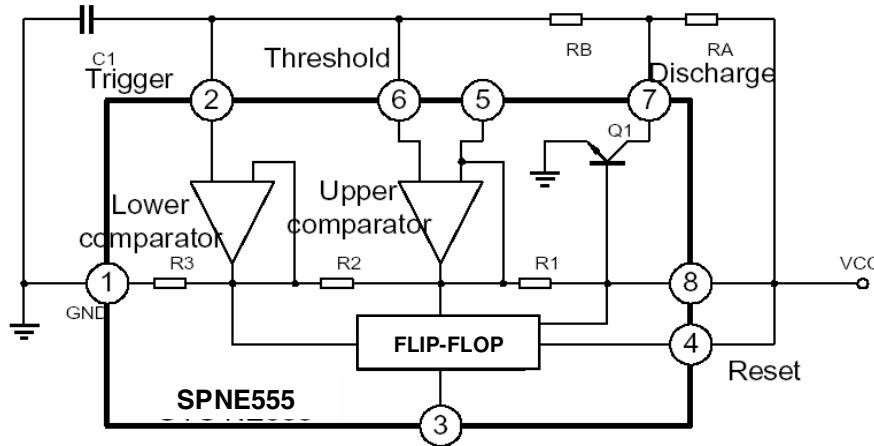
Note 3: This will determine the maximum value of RA+RB for 15V operation, the maximum total is R=20MΩ, and for 5V operation the maximum total is R=6.7MΩ.

Characteristics Curve





Application Circuit



Application Notes

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (Reset) is tied to Vcc (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA, RB and discharge through RB only. In the internal circuit of SSCNE555, one input of the upper comparator is at voltage of $2/3V_{cc}$ ($R1=R2=R3$), another input is connected to Pin 6. As soon as C1 is charging to higher than $2/3V_{cc}$, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of $1/3V_{cc}$, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, flip-flop circuit is set output high.

That is, when C1 charges through RA and RB, output is high and when C1 discharge through RB, output is low. The charge time (output is high) t_1 is $0.693 (RA+RB) C_1$ and the discharge time (output is low) T_2 is $0.693RB \cdot C_1$.

$$\ln \left(\frac{V_{cc} - \frac{1}{3} V_{cc}}{V_{cc} - \frac{2}{3} V_{cc}} \right) = 0.693$$

$$T_1 = 0.693 \cdot (RA + RB) \cdot C_1$$

Thus the total period time T is given by

$$T_2 = 0.693 \cdot RB \cdot C_1$$

$$T = T_1 + T_2 = 0.693(RA + 2RB) \cdot C_1$$

Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(RA + 2RB) \cdot C_1}$$

The duty cycle is given by

$$D.C. = \frac{T_2}{T} = \frac{RB}{RA + 2RB}$$