



## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
30	0.028 at $V_{GS} = 10 \text{ V}$	6	3.8 nC		
	0.034 at V <sub>GS</sub> = 4.5 V	6	3.0 110		

### **FEATURES**

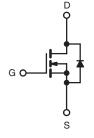
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>a</sub> Tested

# Pb-free RoHS COMPLIANT HALOGEN

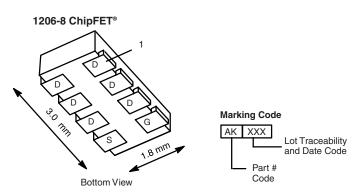
FREE

#### **APPLICATIONS**

- System Power
  - Notebook
  - Netbook
- Load Switch
- Low Current DC/DC



N-Channel MOSFET



Ordering Information: Si5468DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

<b>ABSOLUTE MAXIMUM RATINGS</b>	<b>S</b> T <sub>A</sub> = 25 °C, unles	ss otherwise no	ted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage		$V_{GS}$		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I <sub>D</sub>	6 <sup>a</sup> 6 <sup>a</sup> 6 <sup>a,b, c</sup> 5,5 <sup>a,b, c</sup>	A
Pulsed Drain Current		I <sub>DM</sub>	30	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C T <sub>A</sub> = 25 °C	I <sub>S</sub>	4.8 1.9 <sup>b, c</sup>	
Maximum Power Dissipation	$T_C = 25 °C$ $T_C = 70 °C$ $T_A = 25 °C$ $T_A = 70 °C$	P <sub>D</sub>	5.7 3.6 2.3 <sup>b, c</sup> 1.5 <sup>b, c</sup>	w
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature		260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	45	55	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	18	22	]	

#### Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. See Solder Profile (<a href="https://www.vishay.com/ppg273257">www.vishay.com/ppg273257</a>). The 1206-8 ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 95 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					1		
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	L 050 ·· A		35		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 4.5			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	1.0		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ	
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
		$V_{GS} = 10 \text{ V}, I_D = 6.8 \text{ A}$		0.023	0.028		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 6.2 \text{ A}$		0.028	0.034	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6.8 A		17		S	
Dynamic <sup>b</sup>				l	l		
Input Capacitance	C <sub>iss</sub>			435		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		95			
Reverse Transfer Capacitance	C <sub>rss</sub>			42			
Total Gate Charge	Q <sub>g</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 7.8 \text{ A}$		8	12	nC	
				3.8	6		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 7.8 \text{ A}$		1.4			
Gate-Drain Charge	$Q_{gd}$			1.1			
Gate Resistance	$R_{g}$	f = 1 MHz	1.5	3.2	4.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			15	25	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 2.4 $\Omega$		12	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 6.3$ A, $V_{GEN}=4.5$ V, $R_g=1$ $\Omega$		13	20		
Fall Time	t <sub>f</sub>			10	15		
Turn-On Delay Time	t <sub>d(on)</sub>			5	10		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 2.4 $\Omega$		10	15		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 6.3$ A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		15	25		
Fall Time	t <sub>f</sub>			10	15		
<b>Drain-Source Body Diode Characteristi</b>	cs				•		
Continuous Source-Drain Diode Current	I <sub>S</sub>	$T_C = 25  ^{\circ}C$			4.2	^	
Pulse Diode Forward Current	I <sub>SM</sub>				30	^	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 6.3 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			15	25	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 6.3 A, dI/dt = 100 A/μs, T <sub>.I</sub> = 25 °C		7	12	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 6.3 \text{ A}, \text{ al/at} = 100 \text{ A/}\mu\text{s}, I_J = 25 \text{ °C}$		9			
Reverse Recovery Rise Time	t <sub>b</sub>			6		ns	

### Notes:

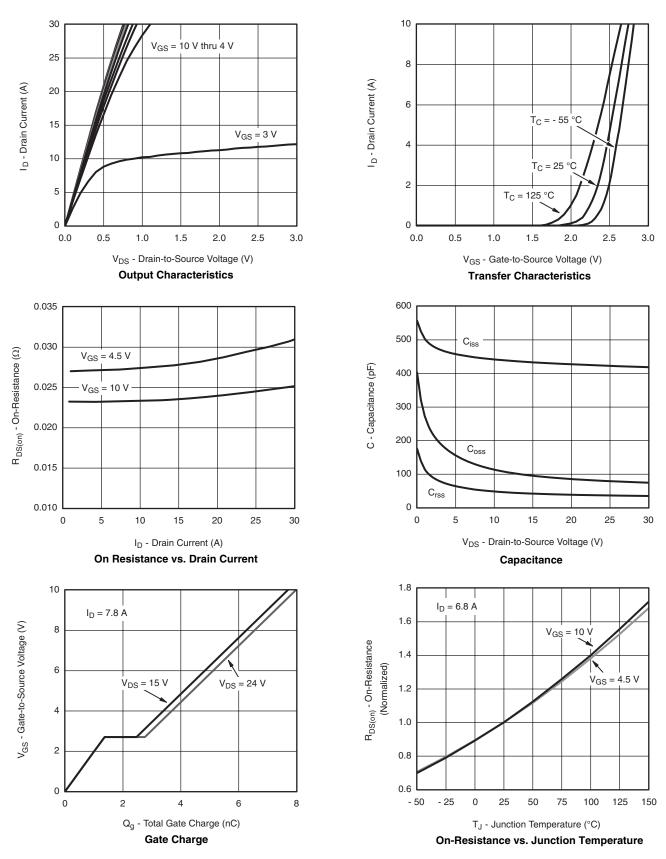
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing.



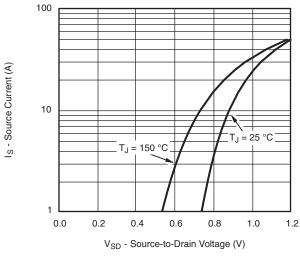
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

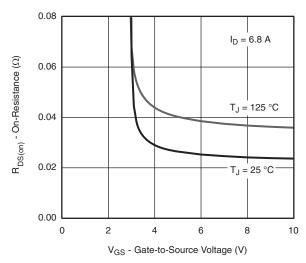


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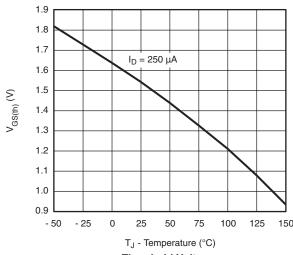
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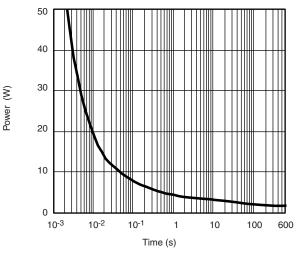




### Forward Diode Voltage vs. Temperature

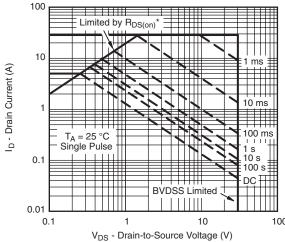






### Threshold Voltage

**Single Pulse Power** 



\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

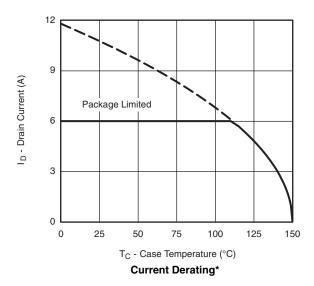
Safe Operating Area, Junction-to-Ambient

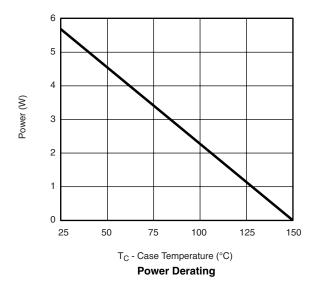






### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





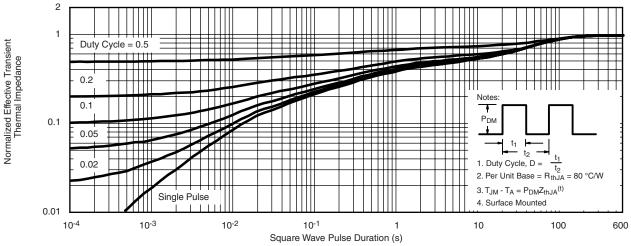
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<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

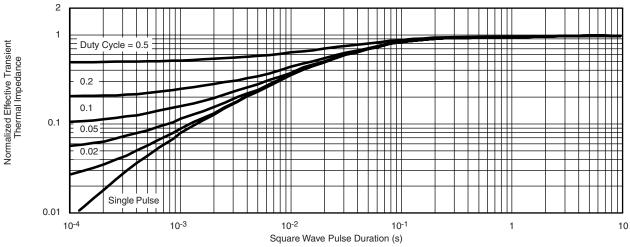
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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppq?69072">www.vishay.com/ppq?69072</a>.



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