

RoHS Compliant Product

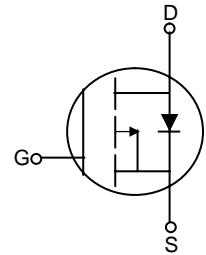
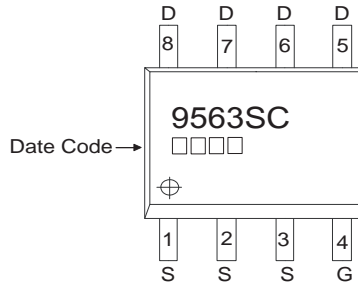
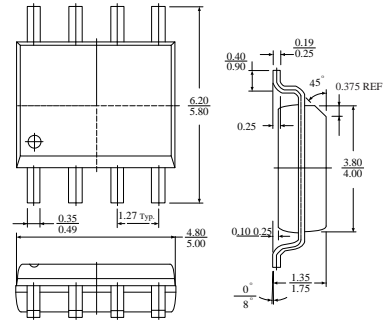
## Description

The SSG9563 provide the designer with the best Combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The SOP-8 is universally preferred for all commercial industrial surface mount application and suited for low voltage applications such as DC/DC converters.

## Features

- \* Lower On-Resistance
- \* Simple Drive Requirement
- \* Fast Switching Characteristics

SOP-8



## Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	-40	V
Gate-Source Voltage	V <sub>GS</sub>	±25	V
Continuous Drain Current <sup>3</sup>	I <sub>D</sub> @T <sub>A</sub> =25°C	-6	A
Continuous Drain Current <sup>3</sup>	I <sub>D</sub> @T <sub>A</sub> =70°C	-4.8	A
Pulsed Drain Current <sup>1</sup>	I <sub>DM</sub>	-30	A
Total Power Dissipation	P <sub>D</sub> @T <sub>A</sub> =25°C	2.5	W
Linear Derating Factor		0.02	W/°C
Operating Junction and Storage Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	-55~+150	°C

## Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient <sup>3</sup> Max.	R <sub>thj-a</sub>	50	°C/W

### Electrical Characteristics (T<sub>j</sub>=25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	- 40	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA
Breakdown Voltage Temp. Coefficient	ΔBV <sub>Ds</sub> /ΔT <sub>j</sub>	-	- 0.03	-	V/°C	Reference to 25°C, I <sub>D</sub> =-1mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.0	-	-3.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±25V
Drain-Source Leakage Current (T <sub>j</sub> =25°C)	I <sub>DSS</sub>	-	-	-1	uA	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0
Drain-Source Leakage Current(T <sub>j</sub> = 70°C)		-	-	-25	uA	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	40	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6 A
		-	-	60		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	19	30	nC	I <sub>D</sub> =-6A V <sub>DS</sub> =-32V V <sub>GS</sub> =4.5V
Gate-Source Charge	Q <sub>gs</sub>	-	5	-		
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>	-	8	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(ON)</sub>	-	12	-	nS	V <sub>DD</sub> =-20V I <sub>D</sub> =-1A V <sub>GS</sub> =-10V R <sub>G</sub> =3.3Ω R <sub>D</sub> =20Ω
Rise Time	T <sub>r</sub>	-	7	-		
Turn-off Delay Time	T <sub>d(OFF)</sub>	-	68	-		
Fall Time	T <sub>f</sub>	-	38	-		
Input Capacitance	C <sub>iss</sub>	-	1600	2560	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =-25V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	240	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	190	-		
Forward Transconductance	G <sub>fs</sub>	-	10	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-6A

### Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	-1.2	V	I <sub>S</sub> =-2.0 A, V <sub>GS</sub> =0V.
Reverse Recovery Time <sup>2</sup>	T <sub>rr</sub>	-	37	-	nS	I <sub>S</sub> =-6 A, V <sub>GS</sub> =0V. dI/dt=100A/us
Reverse Recovery Charge	Q <sub>rr</sub>	-	54	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤300us, duty cycle ≤2%.

3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; 125°C/W when mounted on min. copper pad.

### Characteristics Curve

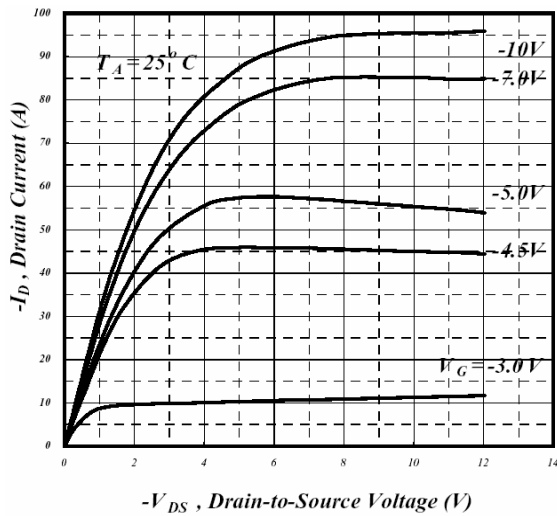


Fig 1. Typical Output Characteristics

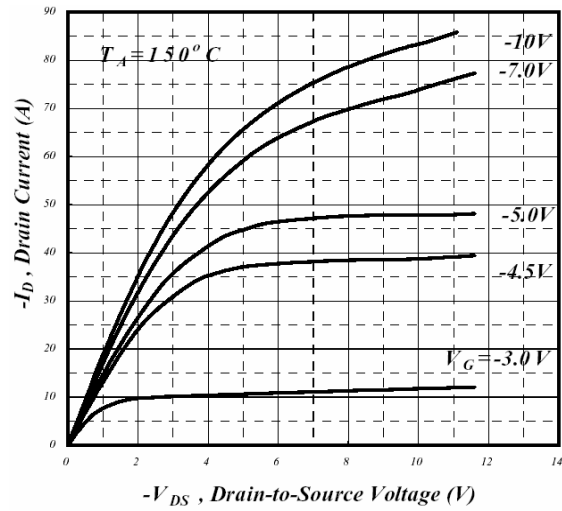


Fig 2. Typical Output Characteristics

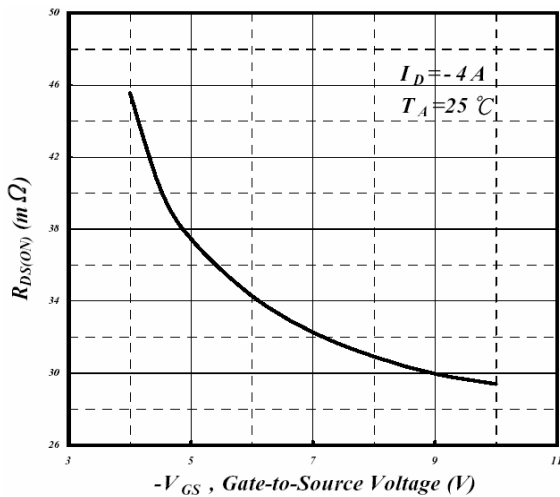


Fig 3. On-Resistance v.s. Gate Voltage

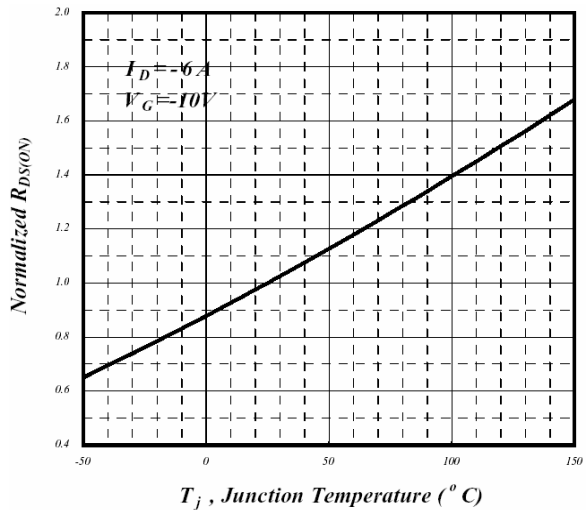


Fig 4. Normalized On-Resistance v.s. Junction Temperature

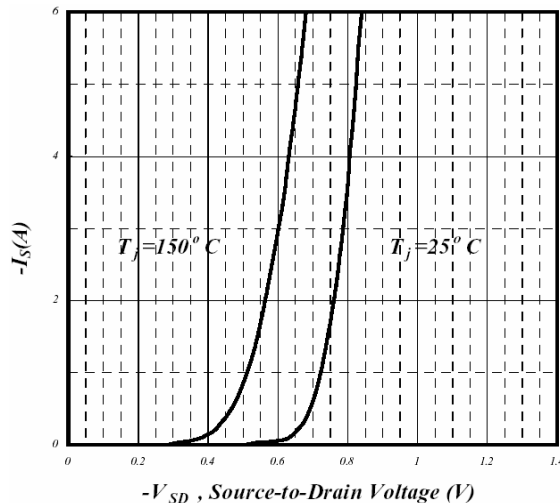


Fig 5. Forward Characteristics of Reverse Diode

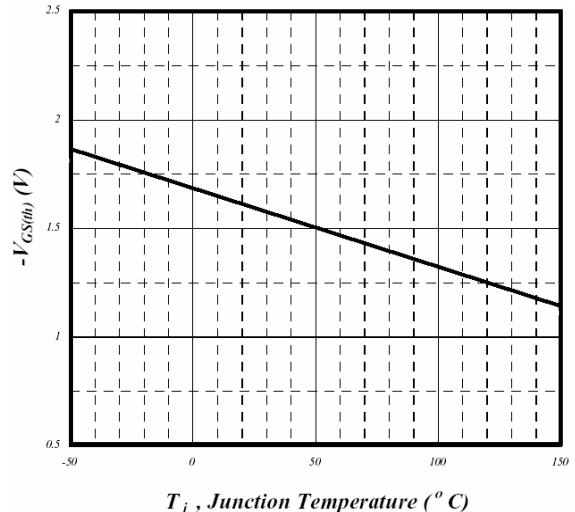


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

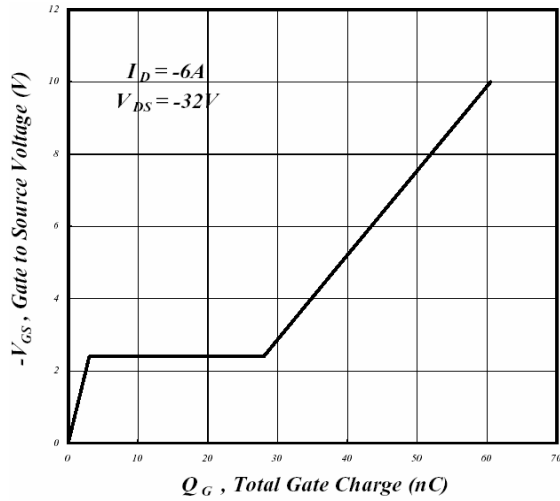


Fig 7. Gate Charge Characteristics

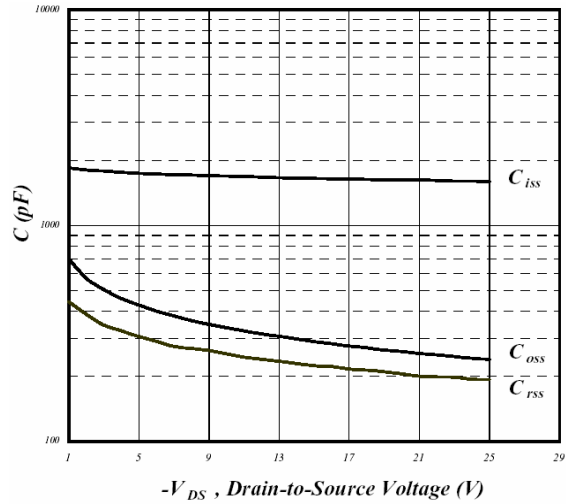


Fig 8. Typical Capacitance Characteristics

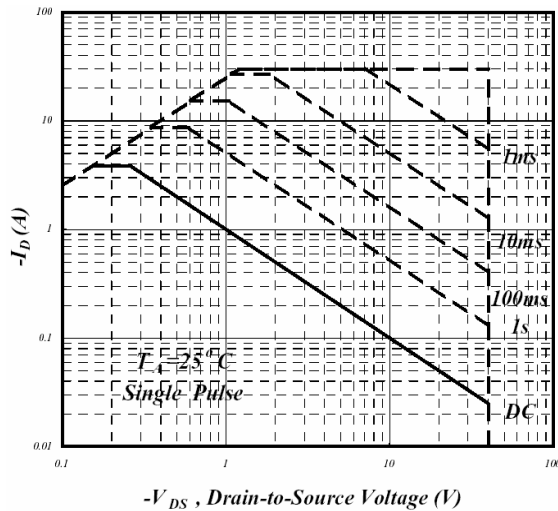


Fig 9. Maximum Safe Operating Area

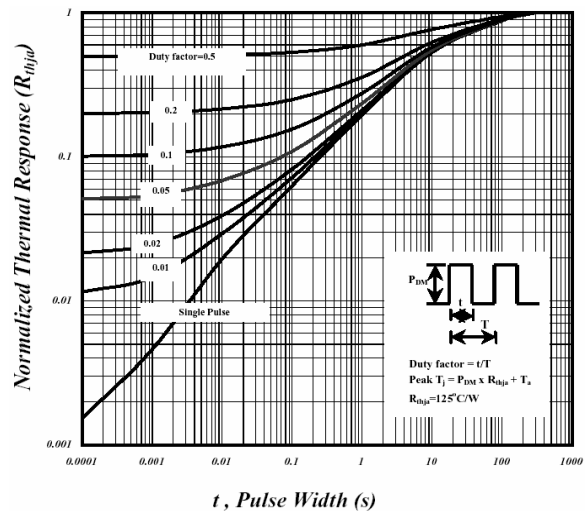


Fig 10. Effective Transient Thermal Impedance

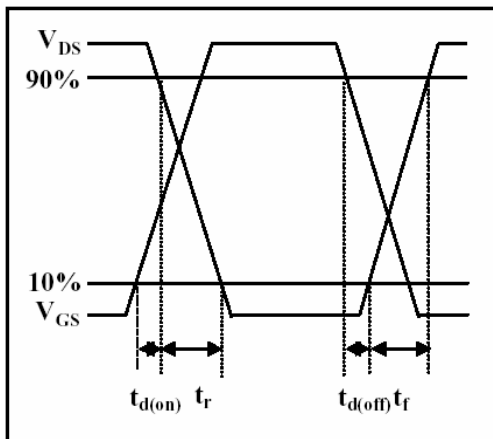


Fig 11. Switching Time Waveform

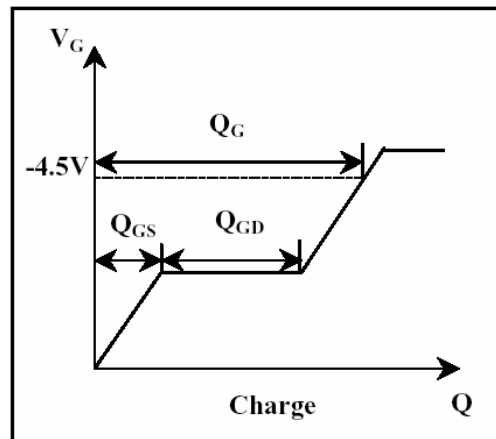


Fig 12. Gate Charge Waveform