# SOLID STATE DISK

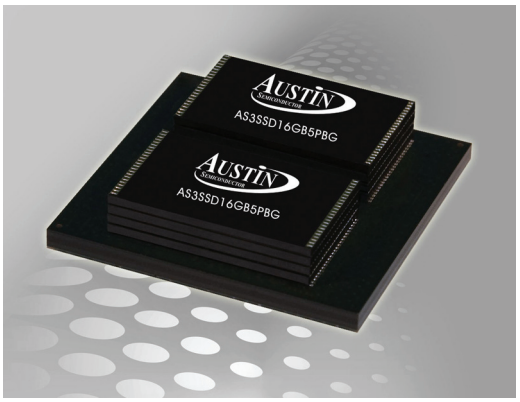
**PRELIMINARY**

**AS3SSD4GB8PBG**
**AS3SSD8GB8PBG**
**AS3SSD16GB5PBG**

## Solid State Disk On Chip (SSDoC)

## FEATURES

- Capacities
  - 4 GB
  - 8 GB
  - 16 GB
- PATA Compatibility
  - ATA-5 compatible
  - UDMA4 supported
  - PIO Mode 4 supported
  - MWDMA Mode 2 supported
- Performance
  - Sustained Sequential Read Bandwidth:16 MB/s
  - Sustained Sequential Write Bandwidth: 5 MB/s
- Form Factor
  - BGA Package
    - 31 mm (W) x 31 mm (L) x 4.2-7.8 mm (H)
    - Weighs approximately 11 grams (TYP)
- Each NAND component, either a 4, 8 or 16Gb device, based on the use of single and stacked silicon solutions
- ECC correction = 6 Bytes within a 512 Byte sector
- Automatic sleep mode
- Controller contained in base interposer
- SLC (Single-Level Cell) NAND Flash
- Reliability
  - Mean Time Between Failure (MTBF) >2,000,000 Hours (est.)
  - Program/Erase >1,000,000 Times (est.)
  - Temp Cycle 500/1000 cycles, JEDEC A104 Condition B -55ºC to +125ºC
- Power Supply Voltage: 5.0V or 3.3 V ± 10% (TYP)
- Power Consumption (Vcc = 5.0 V)
  - Idle: 10 mW (TYP)
  - Active: 255 mW (TYP)
- Operating Temperature
  - Commercial: 0C to 70C
  - Industrial: -45C to 85C
- Shock and Vibration
  - Shock: 1500G MIL-STD0810F
  - Vibration: 15 G RMS MIL-STD0810F
- Compliances
  - Lead free
  - RoHS
  - Sn/Pb Ball Option




## OVERVIEW

The solid state disk is based on a proprietary package stacking technology to create an extremely space conscious, robust Solid State Disk. The SSD is capable of operating in harsh, vibration prone product platforms such embedded computing applications, heavy transportation, ultra portables, handhelds, mobile computing, digital radio, high-speed networking & enterprise applications, as well as, military, aerospace and industrial applications.

For more products and information please visit our web site at
***www.austinsemiconductor.com***

## KEY FEATURES

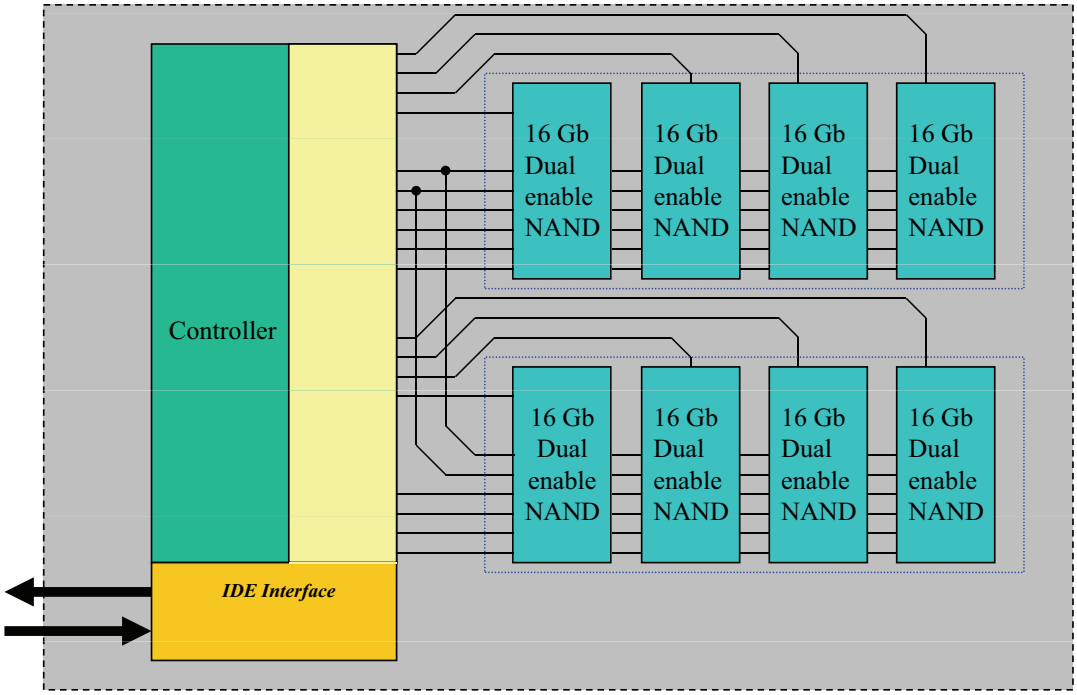
- NAND FLASH Controller
- (2) stacks, each containing (2 or 4) NAND components
- Each NAND component, either a 4,8 or 16Gb device, based on the use of single
- silicon and stacked silicon solutions
- Providing a total bit density of either 4,8 or 16GB
- Controller contained in base interposer
- Fast ATA host to buffer transfer rates supporting True IDE, PIO/4 mode support
- 512Byte Sector Buffers
- Flash Memory power-down logic
- ECC correction = 6 Bytes within a 512 Byte sector
- Automatic Sleep Mode
- Burst Transfer rate, 16.67MB per second
- Sustained Transfer rate: 6.7MB per second
- Sophisticated Wear Leveling

## ARCHITECTURE

The PATA controller in the PATA Solid State Drive utilizes a 32-bit RISC architecture which provides for direct connection of one, two or four NAND flash memory devices (2 per channel). An on-chip error correction code (ECC) and cyclic redundancy check (CRC) unit generates the required code bytes facilitating error detection and correction of up to six bytes per 512 byte data sector. On the fly code byte generation for read and write operations minimizes ECC performance impacts.

The controller's flash memory interface allows the direct connection of up to 10 chips and support Samsung (NAND) type flash memory. ASI PATA Solid State Drives use single level cell (SLC) Samsung NAND Flash Memory devices.

## BLOCK DIAGRAM




## REGULATORY COMPLIANCE

Since the PATA SSD is a component (or a set of components depending on the configuration) on the motherboard, system certifications are the responsibility of the OEM or ODM.

### DEVICE COMPLIANCE

| Compliance | Description |
|---|---|
| PB Free | Components and materials are lead free. |
| RoHS | Restriction of Hazardous Substance Directive |

# PRODUCT SPECIFICATIONS

### Capacity and User Addressable Sectors

| Unformatted | User Addressable Sector in LBA mode |
|---|---|
| 4GB* | 7,880,544 |
| 8GB* | 15,761,088 |
| 16GB* | 31,522,176 |

**Note:** Formatting and other functions will use some of the space, thus the listed capacity will not be available entirely for data storage.

### Read and Write Perfomance

| Operation | Access Type | MB/second |
|---|---|---|
| READ | Sustained Sequential Read Bandwidth | 16 MB/second |
| WRITE | Sustained Sequential Write Bandwidth | 5 MB/second |

# OPERATING CONDITIONS

## Maximum Ratings

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Absolute Maximum Ratings by Device

| Parameter | Symbol | Max. | Min. | Unit |
|---|---|---|---|---|
| Vcc supply voltage | Vcc_P | -0.5 | +5.5 | V |
| Non-Operation Temperature | Ti | -40 | +85 | °C |

## OPERATING CONDITIONS (continued)

## Recommended Operating Conditions

### Operating Temperature and Voltages

| Parameter | Symbol | Max. | Typ | Min. | Unit |
|---|---|---|---|---|---|
| Industrial: 0°C to +70°C | $T_0$ | 0 | - | 70 | °C |
| Commercial: -40°C to +85°C | $T_0$ | 0 | - | 70 | °C |
| Vcc supply voltage | Tcc_P | 4.5 | 5 | 5.5 | V |
| | Tcc_P | 3.0 | 3.3 | 3.6 | V |
| Ground supply voltage | GndPLN | 0 | 0 | 0 | V |

### DC Characteristics (PATA controller configuration)

| Symbol | Paramenter | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | -0.3 | +0.8 | V | |
| $V_{IH}$ | Input HIGH Voltage | 2.2 | Vcc+0.3 | V | |
| $V_{OL}$ | Output LOW Voltage | | 0.45 | V | $I_{OL}$=4mA |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | V | $I_{OH}$=-1mA |
| $I_{CC}$ | Operating Current, $V_{CC\_R}$=5.0V | | | | |
| | Sleep Mode | | 0.2 | mA | |
| | Operating, 20 MHz | | 30 | mA | |
| | Operating, 40 MHz | | 50 | mA | |
| $I_{CC}$ | Operating Current, $V_{CC\_R}$=3.3V | | | | |
| | Sleep Mode | | .02 | m | |
| | Operating, 20 MHz | | 30 | m | |
| | Operating, 40 MHz | | 50 | m | |
| $I_{LI}$ | Input Leakage Current | | ±10 | µA | |
| $I_{LO}$ | Output Leakage Current | | ±10 | µA | |
| $C_{I/O}$ | Input / Output Capacitance | | 10 | pF | |

## ELECTRICAL CHARACTERISTICS

### Power Consumption

| Setting | Value |
|---|---|
| Active Idle Current | 1.85mA |
| Active Current | 51mA |
| Active Power | 255mW |
| Idle Power | 9.25mW |

## ENVIRONMENTAL CONDITIONS

### Temperature Specifications

| | Mode | Max. | Min. | Unit |
|---|---|---|---|---|
| Ambient Temperature | Operate - Commercial | 0 | +70 | °C |
| | Operate - Industrial | -40 | +85 | °C |

## Altitude

Since there are no moving parts, this device is not susceptible to a lack of air molecules and will operate correctly to 85,000 feet above sea level.

### Shock and Vibration Characteristics

| Condition | Value |
|---|---|
| Operating Shock | 1500G MIL-STD-810F |
| Operating Vibration | 15G RMS MIL-STD-810F |

## ENVIRONMENTAL CONDITIONS (continued)

### Acoustics

This drive has no moving or noise-emitting parts; therefore, it produces negligible sound (0dB) in all modes of operation.

### Electrostatic Discharge (ESD)

The PATA SSD can withstand an electrostatic discharge of +/- of 2 KV. ESD testing is done to demonstrate that the units can withstand discharge encountered in normal handling or operations of the equipment.

**Humidity Specifications**

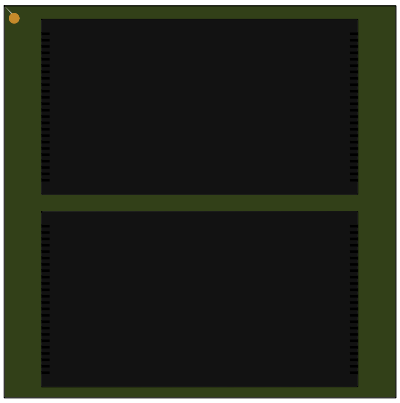
| Condition | Value | Unit |
|---|---|---|
| Operate non-condensing | 5-95 | % |

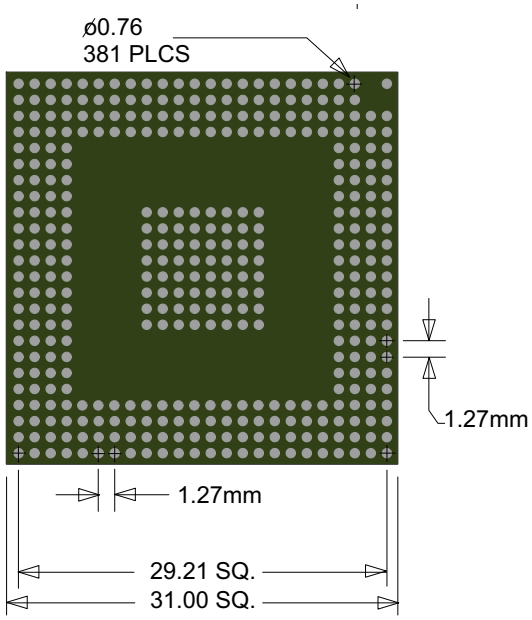
**Reliability Specifications**

| Parameter | Value |
|---|---|
| Mean Time Between Failure (MTBF) | >2,000,000 Hours (est.) |
| Program / Erase | >1,000,000 Time (est.) |
| Warranty | 2 Years |

## MECHANICAL INFORMATION

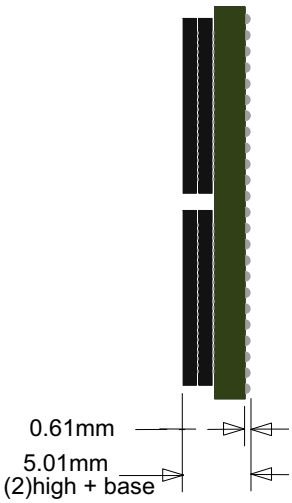
### PATA SSD (Top, Side and Bottom Views)



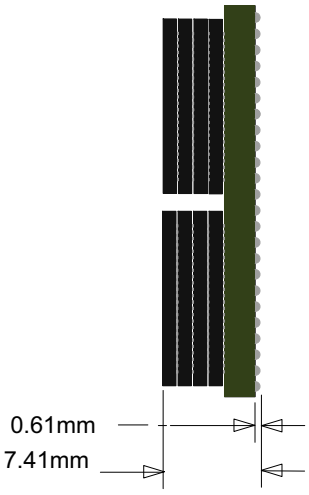



### Stacks, each containing (2 or 4) NAND Components

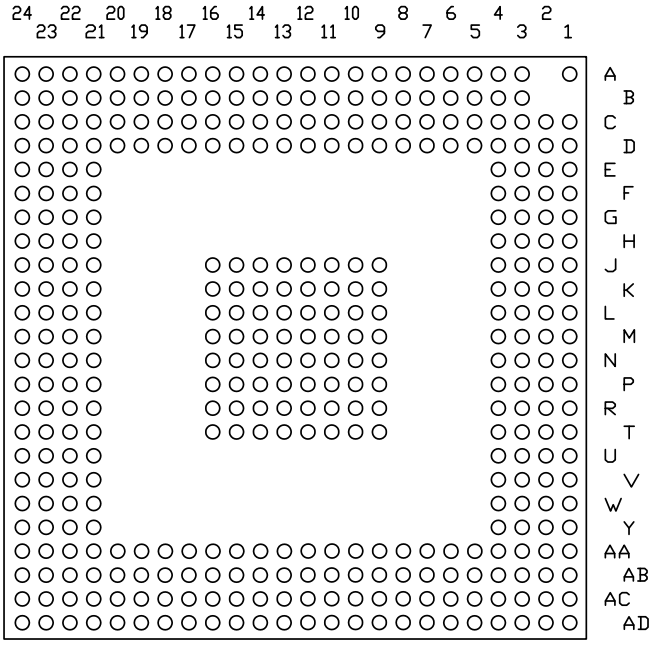
**4GB**




**8GB & 16GB**



## PIN ASSIGNMENTS




| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A1 | GndPLN | B1 | BLANK | C1 | GndPLN | D1 | IDE_A1 |
| A2 | BLANK | B2 | BLANK | C2 | GndPLN | D2 | IDE_A1 |
| A3 | IDE_DMARQ | B3 | IDE_DMARQ | C3 | IDE_DMARQ | D3 | IDE_A1 |
| A4 | IDE_A2 | B4 | IDE_A2 | C4 | IDE_A2 | D4 | IDE_DMARQ |
| A5 | FC_WAIT | B5 | FC_WAIT | C5 | FC_WAIT | D5 | IDE_A2 |
| A6 | FC_PRESET | B6 | FC_PRESET | C6 | FC_PRESET | D6 | FC_WAIT |
| A7 | FC_IDEEN | B7 | FC_IDEEN | C7 | FC_IDEEN | D7 | FC_PRESET |
| A8 | Vcc_P | B8 | Vcc_P | C8 | Vcc_P | D8 | IDE_IDEEN |
| A9 | GndPLN | B9 | GndPLN | C9 | GndPLN | D9 | Vcc_P |
| A10 | Vcc_P | B10 | Vcc_P | C10 | Vcc_P | D10 | NC |
| A11 | IDE_INTRQ | B11 | IDE_INTRQ | C11 | IDE_INTRQ | D11 | NC |
| A12 | FC_MODE | B12 | FC_MODE | C12 | FC_MODE | D12 | IDE_INTRQ |
| A13 | Vcc_C | B13 | Vcc_C | C13 | Vcc_C | D13 | FC_MODE |
| A14 | Gnd_PLN | B14 | Gnd_PLN | C14 | Gnd_PLN | D14 | Vcc_C |
| A15 | Vcc_C | B15 | Vcc_C | C15 | Vcc_C | D15 | IDE_IOWR\ |
| A16 | IDE_IOWR\ | B16 | IDE_IOWR\ | C16 | IDE_IOWR\ | D16 | IDE_IORD\ |
| A17 | IDE_IORD\ | B17 | IDE_IORD\ | C17 | IDE_IORD\ | D17 | IDE_CS1\ |
| A18 | IDE_CS1\ | B18 | IDE_CS1\ | C18 | IDE_CS1\ | D18 | IDE_CS0\ |
| A19 | IDE_CS0\ | B19 | IDE_CS0\ | C19 | IDE_CS0\ | D19 | IDE_D15 |
| A20 | IDE_D15 | B20 | IDE_D15 | C20 | IDE_D15 | D20 | IDE_D7 |
| A21 | IDE_D7 | B21 | IDE_D7 | C21 | IDE_D7 | D21 | IDE_D14 |
| A22 | IDE_D14 | B22 | IDE_D14 | C22 | IDE_D14 | D22 | IDE_D6 |
| A23 | GndPLN | B23 | GndPLN | C23 | GndPLN | D23 | IDE_D6 |
| A24 | GndPLN | B24 | GndPLN | C24 | GndPLN | D24 | IDE_D6 |

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E1 | IDE_DMARQ\ | F1 | IDE_A0 | G1 | FC_LED\ | H1 | IDE_D0 | J1 | IDE_PDIG | K1 | IDE_D1 | L1 | Vcc_P | M1 | GndPLN |
| E2 | IDE_DMARQ\ | F2 | IDE_A0 | G2 | FC_LED\ | H2 | IDE_D0 | J2 | IDE_PDIG | K2 | IDE_D1 | L2 | Vcc_P | M2 | GndPLN |
| E3 | IDE_DMARQ\ | F3 | IDE_A0 | G3 | FC_LED\ | H3 | IDE_D0 | J3 | IDE_PDIG | K3 | IDE_D1 | L3 | Vcc_P | M3 | GndPLN |
| E4 | IDE_A1 | F4 | IDE_DMARQ\ | G4 | IDE_A0 | H4 | FC_LED\ | J4 | IDE_D0 | K4 | IDE_PDIG | L4 | IDE_D1 | M4 | Vcc_P |
| E5 | BLANK | F5 | BLANK | G5 | BLANK | H5 | BLANK | J5 | BLANK | K5 | BLANK | L5 | BLANK | M5 | BLANK |
| E6 | BLANK | F6 | BLANK | G6 | BLANK | H6 | BLANK | J6 | BLANK | K6 | BLANK | L6 | BLANK | M6 | BLANK |
| E7 | BLANK | F7 | BLANK | G7 | BLANK | H7 | BLANK | J7 | BLANK | K7 | BLANK | L7 | BLANK | M7 | BLANK |
| E8 | BLANK | F8 | BLANK | G8 | BLANK | H8 | BLANK | J8 | BLANK | K8 | BLANK | L8 | BLANK | M8 | BLANK |
| E9 | BLANK | F9 | BLANK | G9 | BLANK | H9 | BLANK | J9 | VccPLN_IN | K9 | VccNAND_IN | L9 | VccNAND_IN | M9 | VccNAND_IN |
| E10 | BLANK | F10 | BLANK | G10 | BLANK | H10 | BLANK | J10 | VccPLN_IN | K10 | VccPLN_IN | L10 | VccNAND_IN | M10 | VccNAND_IN |
| E11 | BLANK | F11 | BLANK | G11 | BLANK | H11 | BLANK | J11 | VccPLN_IN | K11 | VccPLN_IN | L11 | VccPLN_IN | M11 | VccNAND_IN |
| E12 | BLANK | F12 | BLANK | G12 | BLANK | H12 | BLANK | J12 | VccPLN_IN | K12 | VccPLN_IN | L12 | VccPLN_IN | M12 | FC_WP_EN1 |
| E13 | BLANK | F13 | BLANK | G13 | BLANK | H13 | BLANK | J13 | VccPLN_IN | K13 | VccPLN_IN | L13 | VccPLN_IN | M13 | FC_WP_EN1 |
| E14 | BLANK | F14 | BLANK | G14 | BLANK | H14 | BLANK | J14 | VccPLN_IN | K14 | VccPLN_IN | L14 | VccPLN_IN | M14 | VccNAND_IN |
| E15 | BLANK | F15 | BLANK | G15 | BLANK | H15 | BLANK | J15 | VccPLN_IN | K15 | VccPLN_IN | L15 | VccNAND_IN | M15 | VccNAND_IN |
| E16 | BLANK | F16 | BLANK | G16 | BLANK | H16 | BLANK | J16 | VccPLN_IN | K16 | VccNAND_IN | L16 | VccNAND_IN | M16 | VccNAND_IN |
| E17 | BLANK | F17 | BLANK | G17 | BLANK | H17 | BLANK | J17 | BLANK | K17 | BLANK | L17 | BLANK | M17 | BLANK |
| E18 | BLANK | F18 | BLANK | G18 | BLANK | H18 | BLANK | J18 | BLANK | K18 | BLANK | L18 | BLANK | M18 | BLANK |
| E19 | BLANK | F19 | BLANK | G19 | BLANK | H19 | BLANK | J19 | BLANK | K19 | BLANK | L19 | BLANK | M19 | BLANK |
| E20 | BLANK | F20 | BLANK | G20 | BLANK | H20 | BLANK | J20 | BLANK | K20 | BLANK | L20 | BLANK | M20 | BLANK |
| E21 | IDE_D6 | F21 | IDE_D13 | G21 | IDE_D5 | H21 | Vcc_P | J21 | IDE_D12 | K21 | IDE_D4 | L21 | IDE_D11 | M21 | NC |
| E22 | IDE_D13 | F22 | IDE_D5 | G22 | Vcc_P | H22 | IDE_D12 | J22 | IDE_D4 | K22 | IDE_D11 | L22 | NC | M22 | IDE_D3 |
| E23 | IDE_D13 | F23 | IDE_D5 | G23 | Vcc_P | H23 | IDE_D12 | J23 | IDE_D4 | K23 | IDE_D11 | L23 | NC | M23 | IDE_D3 |
| E24 | IDE_D13 | F24 | IDE_D5 | G24 | Vcc_P | H24 | IDE_D12 | J24 | IDE_D4 | K24 | IDE_D11 | L24 | NC | M24 | IDE_D3 |

## PIN ASSIGNMENTS (continued)

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **N1** | Vcc_P | **P1** | IDE_D8 | **R1** | IDE_D2 | **T1** | IDE_D9 | **U1** | IDE_PIOIS16\ | **V1** | IDE_D10 | **W1** | FC_WP_EN | **Y1** | Vcc_F |
| **N2** | Vcc_P | **P2** | IDE_D8 | **R2** | IDE_D2 | **T2** | IDE_D9 | **U2** | IDE_PIOIS16\ | **V2** | IDE_D10 | **W2** | FC_WP_EN | **Y2** | Vcc_F |
| **N3** | Vcc_P | **P3** | IDE_D8 | **R3** | IDE_D2 | **T3** | IDE_D9 | **U3** | IDE_PIOIS16\ | **V3** | IDE_D10 | **W3** | FC_WP_EN | **Y3** | Vcc_F |
| **N4** | IDE_D8 | **P4** | IDE_D2 | **R4** | IDE_D9 | **T4** | IDE_PIOIS16\ | **U4** | IDE_D10 | **V4** | FC_WP_EN | **W4** | NC | **Y4** | Vcc_F |
| **N5** | BLANK | **P5** | BLANK | **R5** | BLANK | **T5** | BLANK | **U5** | BLANK | **V5** | BLANK | **W5** | BLANK | **Y5** | BLANK |
| **N6** | BLANK | **P6** | BLANK | **R6** | BLANK | **T6** | BLANK | **U6** | BLANK | **V6** | BLANK | **W6** | BLANK | **Y6** | BLANK |
| **N7** | BLANK | **P7** | BLANK | **R7** | BLANK | **T7** | BLANK | **U7** | BLANK | **V7** | BLANK | **W7** | BLANK | **Y7** | BLANK |
| **N8** | BLANK | **P8** | BLANK | **R8** | BLANK | **T8** | BLANK | **U8** | BLANK | **V8** | BLANK | **W8** | BLANK | **Y8** | BLANK |
| **N9** | VccNAND_IN | **P9** | VccNAND_IN | **R9** | VccNAND_IN | **T9** | GndPLN | **U9** | BLANK | **V9** | BLANK | **W9** | BLANK | **Y9** | BLANK |
| **N10** | VccNAND_IN | **P10** | VccNAND_IN | **R10** | GndPLN | **T10** | GndPLN | **U10** | BLANK | **V10** | BLANK | **W10** | BLANK | **Y10** | BLANK |
| **N11** | VccNAND_IN | **P11** | GndPLN | **R11** | GndPLN | **T11** | GndPLN | **U11** | BLANK | **V11** | BLANK | **W11** | BLANK | **Y11** | BLANK |
| **N12** | FC_WP_EN1 | **P12** | GndPLN | **R12** | GndPLN | **T12** | GndPLN | **U12** | BLANK | **V12** | BLANK | **W12** | BLANK | **Y12** | BLANK |
| **N13** | FC_WP_EN1 | **P13** | GndPLN | **R13** | GndPLN | **T13** | GndPLN | **U13** | BLANK | **V13** | BLANK | **W13** | BLANK | **Y13** | BLANK |
| **N14** | VccNAND_IN | **P14** | GndPLN | **R14** | GndPLN | **T14** | GndPLN | **U14** | BLANK | **V14** | BLANK | **W14** | BLANK | **Y14** | BLANK |
| **N15** | VccNAND_IN | **P15** | VccNAND_IN | **R15** | GndPLN | **T15** | GndPLN | **U15** | BLANK | **V15** | BLANK | **W15** | BLANK | **Y15** | BLANK |
| **N16** | VccNAND_IN | **P16** | VccNAND_IN | **R16** | VccNAND_IN | **T16** | GndPLN | **U16** | BLANK | **V16** | BLANK | **W16** | BLANK | **Y16** | BLANK |
| **N17** | BLANK | **P17** | BLANK | **R17** | BLANK | **T17** | BLANK | **U17** | BLANK | **V17** | BLANK | **W17** | BLANK | **Y17** | BLANK |
| **N18** | BLANK | **P18** | BLANK | **R18** | BLANK | **T18** | BLANK | **U18** | BLANK | **V18** | BLANK | **W18** | BLANK | **Y18** | BLANK |
| **N19** | BLANK | **P19** | BLANK | **R19** | BLANK | **T19** | BLANK | **U19** | BLANK | **V19** | BLANK | **W19** | BLANK | **Y19** | BLANK |
| **N20** | BLANK | **P20** | BLANK | **R20** | BLANK | **T20** | BLANK | **U20** | BLANK | **V20** | BLANK | **W20** | BLANK | **Y20** | BLANK |
| **N21** | IDE_D3 | **P21** | FADJ | **R21** | NC | **T21** | NC | **U21** | Vcc_R | **V21** | CADJ | **W21** | COUT | **Y21** | Vcc_F |
| **N22** | FOUT | **P22** | FOUT | **R22** | FADJ | **T22** | Vcc_R | **U22** | GndPLN | **V22** | Vcc_R | **W22** | CADJ | **Y22** | COUT |
| **N23** | FOUT | **P23** | FOUT | **R23** | FADJ | **T23** | Vcc_R | **U23** | GndPLN | **V23** | Vcc_R | **W23** | CADJ | **Y23** | COUT |
| **N24** | FOUT | **P24** | FOUT | **R24** | FADJ | **T24** | Vcc_R | **U24** | GndPLN | **V24** | Vcc_R | **W24** | CADJ | **Y24** | COUT |

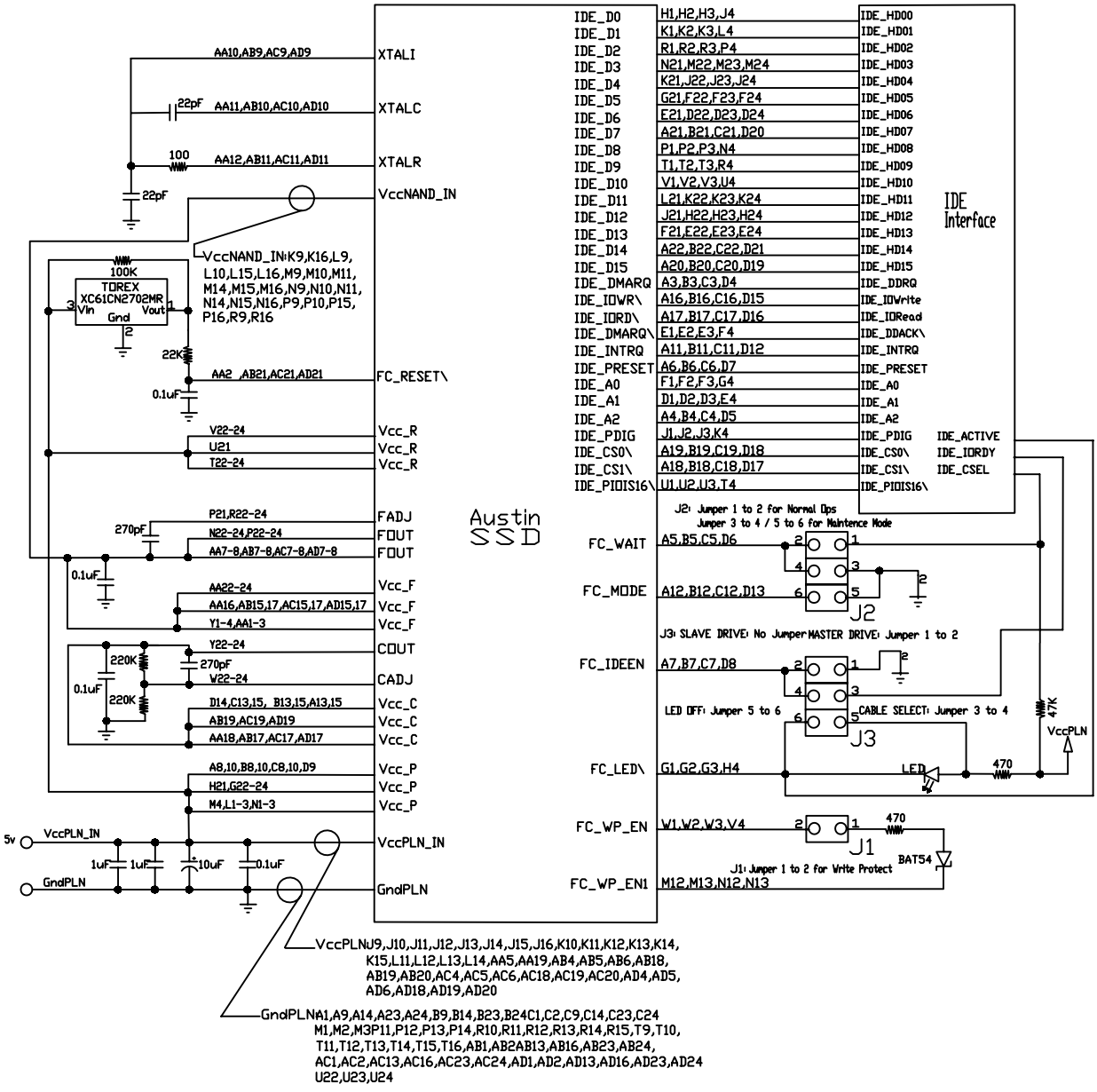
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **AA1** | Vcc_F | **AB1** | GndPLN | **AC1** | GndPLN | **AD1** | GndPLN |
| **AA2** | Vcc_F | **AB2** | GndPLN | **AC2** | GndPLN | **AD2** | GndPLN |
| **AA3** | Vcc_F | **AB3** | NC | **AC3** | NC | **AD3** | NC |
| **AA4** | NC | **AB4** | VccPLN_IN | **AC4** | VccPLN_IN | **AD4** | VccPLN_IN |
| **AA5** | VccPLN_IN | **AB5** | VccPLN_IN | **AC5** | VccPLN_IN | **AD5** | VccPLN_IN |
| **AA6** | NC | **AB6** | VccPLN_IN | **AC6** | VccPLN_IN | **AD6** | VccPLN_IN |
| **AA7** | FOUT | **AB7** | FOUT | **AC7** | FOUT | **AD7** | FOUT |
| **AA8** | FOUT | **AB8** | FOUT | **AC8** | FOUT | **AD8** | FOUT |
| **AA9** | NC | **AB9** | XTALI | **AC9** | XTALI | **AD9** | XTALI |
| **AA10** | XTALI | **AB10** | XTALC | **AC10** | XTALC | **AD10** | XTALC |
| **AA11** | XTALC | **AB11** | XTALR | **AC11** | XTALR | **AD11** | XTALR |
| **AA12** | XTALR | **AB12** | Vcc_C | **AC12** | Vcc_C | **AD12** | Vcc_C |
| **AA13** | Vcc_C | **AB13** | GndPLN | **AC13** | GndPLN | **AD13** | GndPLN |
| **AA14** | NC | **AB14** | Vcc_C | **AC14** | Vcc_C | **AD14** | Vcc_C |
| **AA15** | NC | **AB15** | Vcc_F | **AC15** | Vcc_F | **AD15** | Vcc_F |
| **AA16** | Vcc_F | **AB16** | GndPLN | **AC16** | GndPLN | **AD16** | GndPLN |
| **AA17** | NC | **AB17** | Vcc_F | **AC17** | Vcc_F | **AD17** | Vcc_F |
| **AA18** | NC | **AB18** | VccPLN_IN | **AC18** | VccPLN_IN | **AD18** | VccPLN_IN |
| **AA19** | VccPLN_IN | **AB19** | VccPLN_IN | **AC19** | VccPLN_IN | **AD19** | VccPLN_IN |
| **AA20** | FC_RESET | **AB20** | VccPLN_IN | **AC20** | VccPLN_IN | **AD20** | VccPLN_IN |
| **AA21** | NC | **AB21** | FC_RESET | **AC21** | FC_RESET | **AD21** | FC_RESET |
| **AA22** | Vcc_F | **AB22** | NC | **AC22** | NC | **AD22** | NC |
| **AA23** | Vcc_F | **AB23** | GndPLN | **AC23** | GndPLN | **AD23** | GndPLN |
| **AA24** | Vcc_F | **AB24** | GndPLN | **AC24** | GndPLN | **AD24** | GndPLN |

## SIGNAL DESCRIPTIONS

| Symbol | Type | Description |
|---|---|---|
| IDE_A0 | Output | Address bus |
| IDE_A1 | Output | |
| IDE_A2 | Output | |
| IDE_D0 | Input/Output | Data bus. The signals D15..D0 represent the bidirectional data bus; active high signals a "one". |
| IDE_D1 | Input/Output | |
| IDE_D2 | Input/Output | |
| IDE_D3 | Input/Output | |
| IDE_D4 | Input/Output | |
| IDE_D5 | Input/Output | |
| IDE_D6 | Input/Output | |
| IDE_D7 | Input/Output | |
| IDE_D8 | Input/Output | |
| IDE_D9 | Input/Output | |
| IDE_D10 | Input/Output | |
| IDE_D11 | Input/Output | |
| IDE_D12 | Input/Output | |
| IDE_D13 | Input/Output | |
| IDE_D14 | Input/Output | |
| IDE_D15 | Input/Output | |
| IDE_INTRQ | Output | Drive interrupt request. |
| IDE_IOWR\ | Input | I/O Data Write Enable is the strobe signal asserted by the host to write device registers or the data port.<br>DIOW shall be negated by the host prior to the initiation of an Ultra DMA burst. STOP shall be negated by the host before the data is transferred in an Ultra DMA burst. The assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst. |
| IDE_IORD\ | Input | I/O Data Read Enable is the strobe signal asserted by the host to read device registers or the data port. |
| IDE_CS0\ | Input | Drive chip select 0 is used by host to select Command Block registers. |
| IDE_CS1\ | Input | Drive chip select 1 is used by host to select Command Block registers. |
| IDE_PIOIS16\ | Output | 16-bit I/O transfer. |
| IDE_PDIG | Input/Output | Passed diagnostics. |
| IDE_DMARQ<br>IDE_DMARQ\ | Output | DMA request. This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. For multi word DMA transfers, the direction of data transfer is Controller by IDE_IORD\ and IDE_IOWR\. When a DMS operation is enabled, CS0\ and CS1\ shall not be asserted and transfers shall be 16 bits wide. This signal shall be release when the device is not selected. |
| FC_WAIT | Output | Ready signal to IDE_IORDY |

| | | |
|---|---|---|
| IDE_PRESET | Input | Reset |
| FC_WP_EN<br>FC_WP_EN1 | Input | Write protect signal |
| FC_RESET | Input | Reset processor. RESET# low resets the processor to the initial state and halts all activity. RESET# must be low for at least one cycle. On a transition from low to high, a Reset exception occurs and the processor starts execution at the Reset entry determined by the INT4 state. The transition may occur asynchronously to the clock. We recommend connecting this pin to a voltage monitoring circuit with open-drain output (e.g. Torex XC61A) supplying a reset signal for supply voltages less than 2.6 or 2.7V, connected to a R/C combination of 100 kΩ and 100 nF giving an additional reset delay in the order of 10 ms. |
| FC_LED\ | Output | Operation LED signal |
| FC_MODE | | |
| FC_IDEEN | Output | Master/Slave select and connect to IDE_CSEL for Cable select option |
| XTALR | Output | R/C Clock Oscillator Resistor Output. The resistor connected between this pin and XTALI determines the operating clock frequency. Use a 470Ω resistor to obtain a frequency of about 20 MHz |
| XTALC | Output | R/C Clock Oscillator Capacitor Output. Connect a 22pF capacitor between this pin and XTALI. |
| XTALI | Input | R/C Clock Oscillator Input. This input connects to the other side of the resisors and the capacitor connected to XTALR1, XTALR2 and XTALC. Connect a 22pF capacitor from this pin to ground. |
| NC | | Not connected |
| Vcc_C | Supply | Power Supply Voltage, Core |
| Vcc_R | Supply | Power Supply Voltage, Regulator |
| Vcc_F | Supply | Power Supply Voltage, Flash Memory |
| Vcc_P | Supply | Power Supply Voltage, controller |
| FADJ | Input | 3.3V Flash Memory Power Supply Adjustment. Connect a 270pF capacitor from this pin to FOUT. |
| FOUT | Output | 3.3V Flash Memory Power Supply. This output provides a regulated 3.3V supply if the power supply voltage is above 3.3V. This supply voltage must also be connected to the VCC_F pins. |
| CADJ | Input | 2.5V Core Power Supply Adjustment. Connect a 220kΩ resistor from this pin to GND, a 220kΩ resistor from this pin to COUT, and a 270pF capacitor from this pin to COUT. |
| COUT | Output | 2.5V Core Power Supply. This output provides a regulated 2.5V supply if the power supply voltage is above 3.3V. This supply voltage must be connected to the VCC_C pins. |
| VccNAND_IN | Supply | 3.3V Flash Memory Power Supply |
| VccPLN_IN | Supply | Supply to the controller |
| GndPLN | Supply | Supply ground |

## TYPICAL APPLICATION DESIGN



# COMMAND SETS

The PATA SSD device supports all the mandatory ATA commands as defined in the ATA/ATAPI-5 specification.

## ATA General Feature Command Set

The PATA SSD device supports the ATA General Feature command set.

| Common Name | Code |
|---|---|
| EXECUTE DEVICE DIAGNOSTIC | 90h |
| IDENTIFY DEVICE | ECh |
| IDENTIFY DEVICE DMA | EEh |
| INITIALI□E DRIVE PARAMETERS | 91h |
| NOP | 00h |
| READ BUFFER | E4h |
| READ DMA | C8h, C9h |
| READ LONG | 22h, 23h |
| READ MULTIPLE | C4h |
| READ NATIVE MAX ADDRESS | F8h |
| READ SECTOR(S) | 20h, 21h |
| READ VERIFY SECTOR(S) | 40h, 41h |
| RECALIBRATE | 1Xh |
| SEEK | 7Xh |
| SET FEATURES | EFh |
| SET MULTIPLE MODE | C6h |
| SMART | B0h |
| TRANSLATE SECTOR | 87h |
| WRITE BUFFER | E8h |
| WRITE DMA | CAh, CBh |
| WRITE LONG | 32h, 31h |
| WRITE MULTIPLE | C5h |
| WRITE MULTIPLE without ERASE | CDh |
| WRITE SECTOR(S) | 30h, 31h |
| WRITE SECTOR(S)without ERASE | 38h |
| WRITE VERIFY | 3Ch |

## REFERENCE

This document also references standards and specifications defined by a variety of organizations. Please use the following information to identify the location of an organization's standards information.

| Date or Revision Number | Title | Location |
|---|---|---|
| February 2000 | ATA-5 | http://www.t13.org/Documents/UploadedDocuments/project/d1321r3-ATAATAPI-5.pdf |
| December 2004 | JEDEC Standard JESD22-C101C: Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components | http://www.jedec.org/download/search/default2.cfm |
| March 2006 | Hyperston F2-16x, 32-Bit Flash Memory Controller Specification | http://www.hyperstone.com/fmc_f2_en,15593.html |
| January 2007 | JEDEC Standard: Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) | http://www.jedec.org/download/search/default2.cfm |

## GLOSSARY

This document incorporates many industry and device specific words. Use the following list to define a variety of terms and acronyms.

| Term | Definition |
|---|---|
| ATA | Advanced Technology Attachment |
| CFA | CompactFlash Association |
| CPRM | Content Protection for Recordable Media |
| CRC | Cyclic Redundancy Check |
| DMA | Direct Memory Access |
| ECC | Error Correction Code |
| ESD | Electrostatic Discharge |
| HDD | Hard Disk Drive |
| HPA | Host Protected Area |
| IDE | Integrated Device Electronics |
| LBA | Logical Block Addressing |
| MTBF | Mean Time Between Failure |
| MWDMA | Multi-word DMA |
| ODM | Original Design Manufacturer |
| OEM | Original Equipment Manufacturer |
| PATA | Parallel ATA |
| PCMCIA | Personal Computer Memory Card International Assocoation |
| PIO | Programmable Input / Output |
| SATA | Serial ATA |
| SSD | Solid state drive |
| UMDA | Ultra DMA, also know Ultra ATA |

## ORDER CHART

| Part Number | Storage Density | Sustained Transfer Rate |
|---|---|---|
| AS3SSD4GB8PBGR/IT | 4GB | 7.7MB/sec |
| AS3SSD8GB8PBGR/IT | 8GB | 7.7MB/sec |
| AS3SSD16GB5PBGR/IT | 16GB | 5.0MB/sec |
| AS3SSD4GB8PBGR/CT | 4GB | 7.7MB/sec |
| AS3SSD8GB8PBGR/CT | 8GB | 7.7MB/sec |
| AS3SSD16GB5PBGR/CT | 16GB | 5.0MB/sec |

Available Processes

CT = Commercial Temperature Range 0°C to +70°C
IT = Industrial Temperature Range -40°C to +85°C

R = RoHS Compliant / Lead Free
Blank = Sn / Pb Finish Option

**DOCUMENT TITLE**

4GB, 8GB, 16GB Solid State Disk on Chip

**REVISION HISTORY**

| Rev # | History | Release Date | Status |
|---|---|---|---|
| 1.0 | Initial Release | December 2008 | Preliminary |
| 1.1 | Updated Mechanical Information | January 2009 | Preliminary |
| 1.2 | Updated Order Chart | March 2009 | Preliminary |
| 1.3 | Updated 4GB & 8GB Drawing | July 2009 | Preliminary |