PRELIMINARY

# CY14B101LA, CY14B101NA

# 1 Mbit (128K x 8/64K x 16) nvSRAM

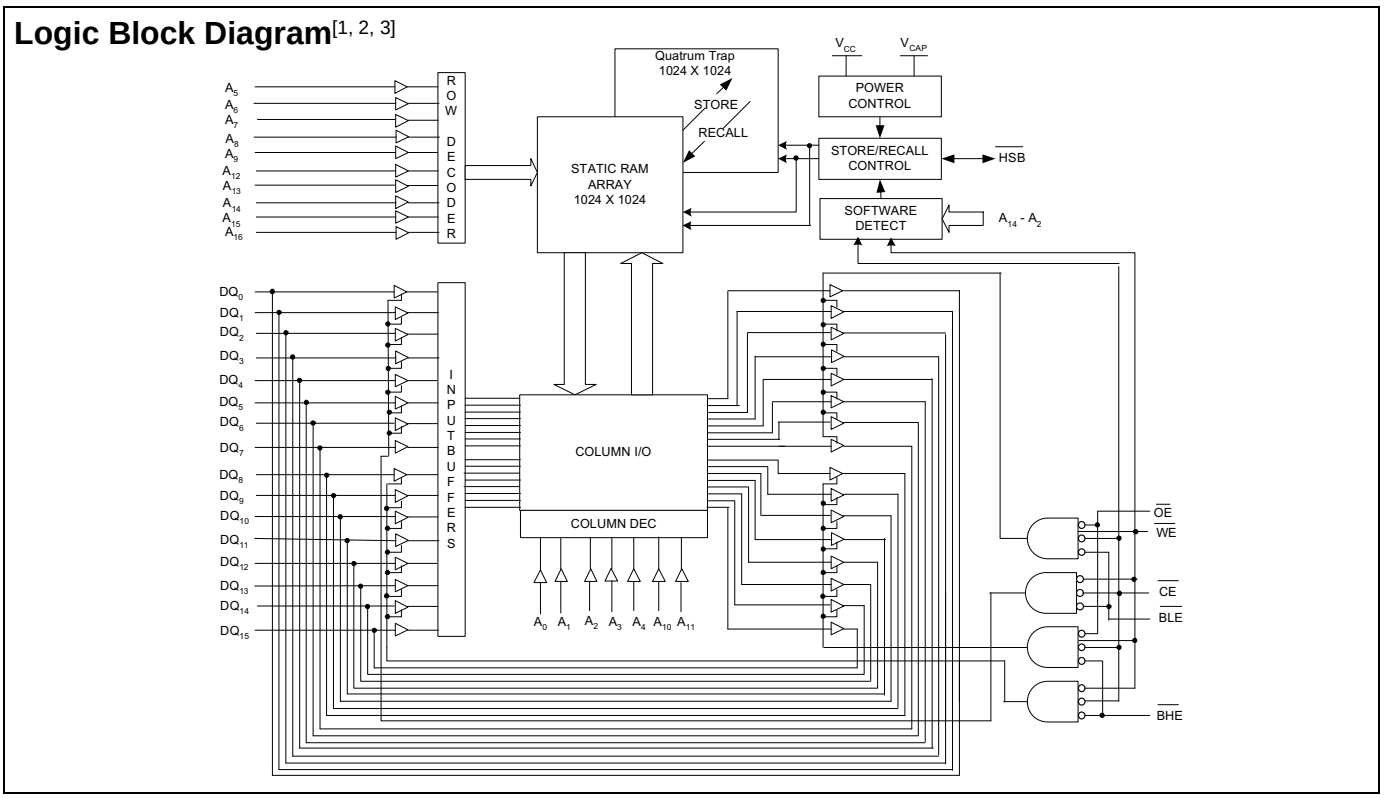
## Features

- 20 ns, 25 ns, and 45 ns Access Times
- Internally Organized as 128K x 8 (CY14B101LA) or 64K x 16 (CY14B101NA)
- Hands off Automatic STORE on Power Down with only a Small Capacitor
- STORE to QuantumTrap Nonvolatile Elements Initiated by Software, Device Pin, or AutoStore on Power Down
- RECALL to SRAM Initiated by Software or Power Up
- Infinite Read, Write, and Recall Cycles
- 200,000 STORE Cycles to QuantumTrap
- 20 year Data Retention
- Single 3V +20% to -10% Operation
- Commercial and Industrial Temperatures
- 54/44-Pin TSOP-II, 48-Pin SSOP, and 32-Pin SOIC Packages
- Pb-free and RoHS Compliance

## Functional Description

The Cypress CY14B101LA/CY14B101NA is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 128K bytes of 8 bits each or 64K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

## Logic Block Diagram[1, 2, 3]




**Notes**
1. Address $A_0$ - $A_{16}$ for x8 configuration and Address $A_0$ - $A_{15}$ for x16 configuration.
2. Data $DQ_0$ - $DQ_7$ for x8 configuration and Data $DQ_0$ - $DQ_{15}$ for x16 configuration.
3. $\overline{BHE}$ and $\overline{BLE}$ are applicable for x16 configuration only.

## Pinouts

**Figure 1. Pin Diagram - 44 Pin TSOP II**

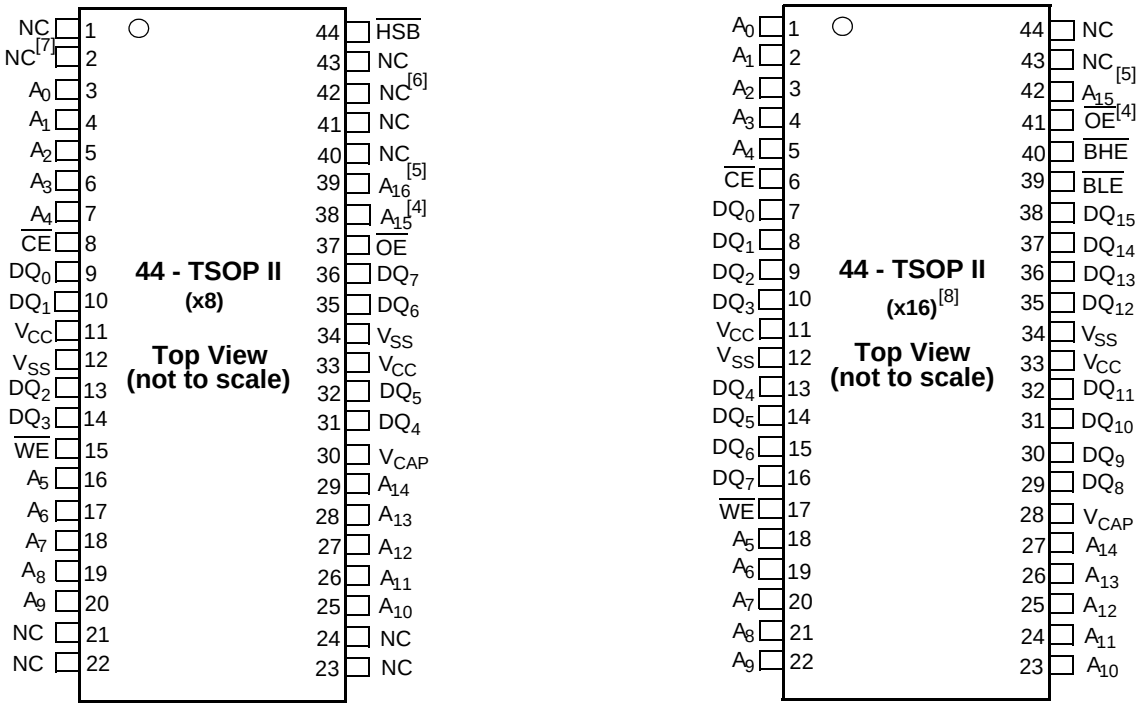
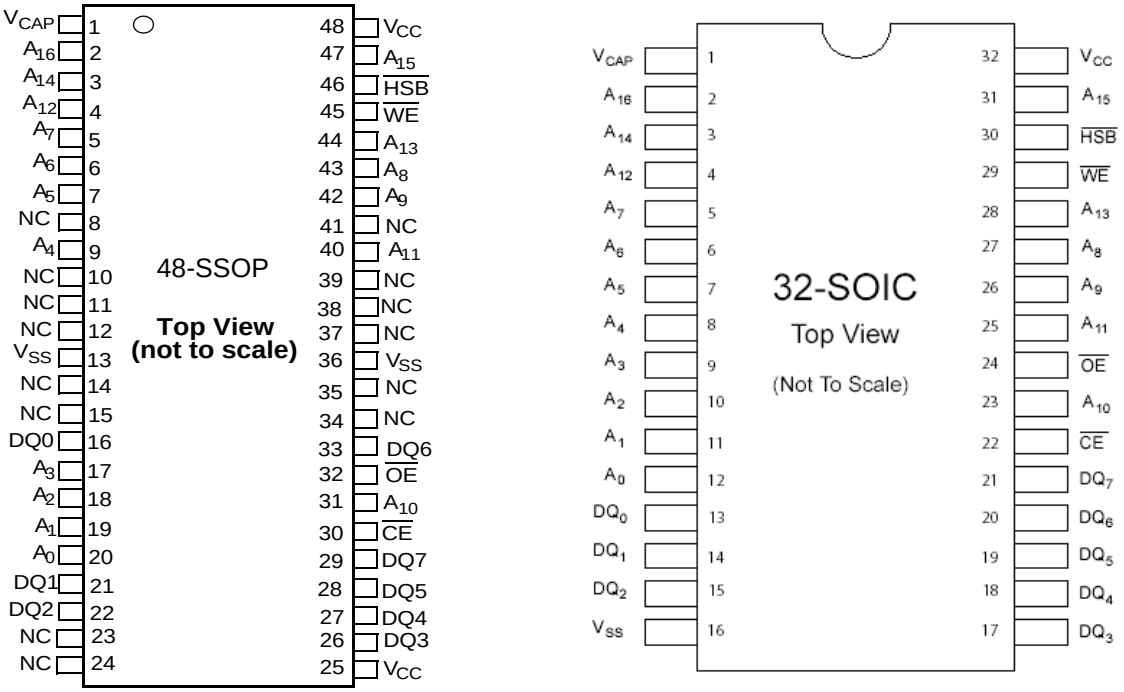



**Figure 2. Pin Diagram - 48-Pin SSOP and 32-Pin SOIC**




**Notes**

4. Address expansion for 2 Mbit. NC pin not connected to die.
5. Address expansion for 4 Mbit. NC pin not connected to die.
6. Address expansion for 8 Mbit. NC pin not connected to die.
7. Address expansion for 16 Mbit. NC pin not connected to die.
8. HSB pin is not available in 44-TSOP II (x16) package.

## Pinouts (continued)

**Figure 3. Pin Diagram - 54-Pin TSOP II**

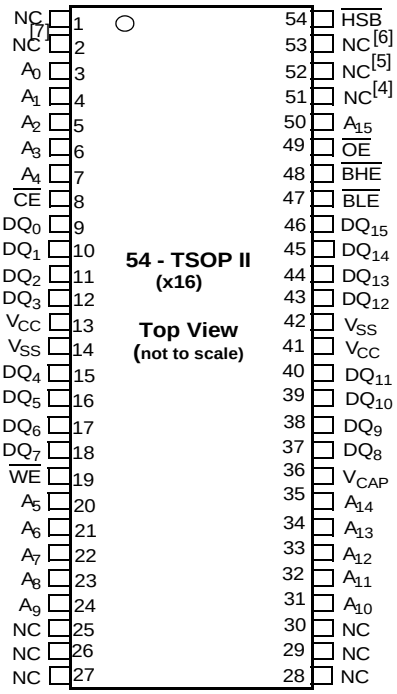



**Table 1. Pin Definitions**

| Pin Name | I/O Type | Description |
|---|---|---|
| $A_0 – A_{16}$ | Input | **Address Inputs Used to Select one of the 131,072 Bytes of the nvSRAM for x8 Configuration.** |
| $A_0 – A_{15}$ | | **Address Inputs Used to Select one of the 65,536 Words of the nvSRAM for x16 Configuration.** |
| $DQ_0 – DQ_7$ | Input/Output | **Bidirectional Data I/O Lines for x8 Configuration**. Used as input or output lines depending on operation. |
| $DQ_0 – DQ_{15}$ | | **Bidirectional Data I/O Lines for x16 Configuration**. Used as input or output lines depending on operation. |
| $\overline{WE}$ | Input | **Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location. |
| $\overline{CE}$ | Input | **Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{OE}$ | Input | **Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tristated on deasserting $\overline{OE}$ HIGH. |
| $\overline{BHE}$ | Input | **Byte High Enable, Active LOW**. Controls $DQ_{15}$ - $DQ_8$. |
| $\overline{BLE}$ | Input | **Byte Low Enable, Active LOW**. Controls $DQ_7$ - $DQ_0$. |
| $V_{SS}$ | Ground | **Ground for the Device**. Must be connected to the ground of the system. |
| $V_{CC}$ | Power Supply | **Power Supply Inputs to the Device**. 3.0V +20%, –10% |
| $\overline{HSB}$[8] | Input/Output | **Hardware STORE Busy (HSB)**. When LOW this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional). After each STORE operation HSB is driven HIGH for short time with standard output high current. |
| $V_{CAP}$ | Power Supply | **AutoStore Capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements. |
| NC | No Connect | **No Connect**. This pin is not connected to the die. |

## Device Operation

The CY14B101LA/CY14B101NA nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14B101LA/CY14B101NA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200K STORE operations. Refer to the Truth Table For SRAM Operations on page 16 for a complete description of read and write modes.

## SRAM Read

The CY14B101LA/CY14B101NA performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0-16}$ or $A_{0-15}$ determines which of the 131,072 data bytes or 65,536 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of $t_{AA}$ (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at $t_{ACE}$ or at $t_{DOE}$, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the $t_{AA}$ access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

## SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins $DQ_{0–15}$ are written into the memory if the data is valid $t_{SD}$ before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16-bit words. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers $t_{HZWE}$ after $\overline{WE}$ goes LOW.

## AutoStore Operation

The CY14B101LA/CY14B101NA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by $\overline{HSB}$; Software STORE activated by an address sequence; AutoStore on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101LA/CY14B101NA.

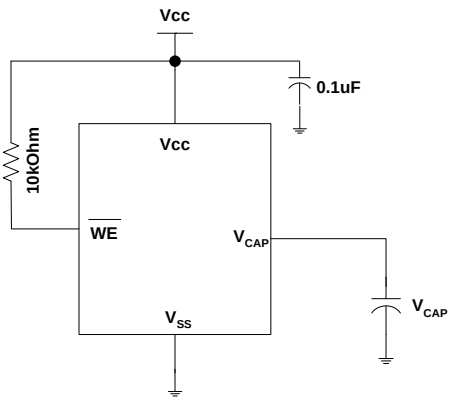
During a normal operation, the device draws current from $V_{CC}$ to charge a capacitor connected to the $V_{CAP}$ pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the $V_{CC}$ pin drops below $V_{SWITCH}$, the part automatically disconnects the $V_{CAP}$ pin from $V_{CC}$. A STORE operation is initiated with power provided by the $V_{CAP}$ capacitor.

**Note** If the capacitor is not connected to $V_{CAP}$ pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 6. In case AutoStore is enabled without a capacitor on $V_{CAP}$ pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This may corrupt the data stored in nvSRAM.

Figure 4 shows the proper connection of the storage capacitor ($V_{CAP}$) for automatic STORE operation. Refer to DC Electrical Characteristics on page 8 for the size of $V_{CAP}$. The voltage on the $V_{CAP}$ pin is driven to $V_{CC}$ by a regulator on the chip. Place a pull up on $\overline{WE}$ to hold it inactive during power up. This pull up is only effective if the $\overline{WE}$ signal is tristate during power up. Many MPUs tristate their controls on power up. This must be verified when using the pull up. When the nvSRAM comes out of power-on-recall, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

**Figure 4. AutoStore Mode**




## Hardware STORE Operation

The CY14B101LA/CY14B101NA provides the $\overline{HSB}$[8] pin to control and acknowledge the STORE operations. Use the $\overline{HSB}$ pin to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14B101LA/CY14B101NA conditionally initiates a STORE operation after $t_{DELAY}$. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time ($t_{DELAY}$) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. In case the write latch is not set, $\overline{HSB}$ is not driven LOW by the CY14B101LA/CY14B101NA. But any SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14B101LA/CY14B101NA continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the CY14B101LA/CY14B101NA remains disabled until the HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

## Hardware RECALL (Power Up)

During power up or after any low power condition ($V_{CC}$< $V_{SWITCH}$), an internal RECALL request is latched. When $V_{CC}$ again exceeds the sense voltage of $V_{SWITCH}$, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, HSB is driven low by the HSB driver.

## Software STORE

Data is transferred from SRAM to the nonvolatile memory by a software address sequence. The CY14B101LA/CY14B101NA Software STORE cycle is initiated by executing sequential $\overline{CE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

**Table 2. Mode Selection**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$[3] | $A_{15}$ - $A_0$[9] | Mode | I/O | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | Not Selected | Output High Z | Standby |
| L | H | L | X | Read SRAM | Output Data | Active |
| L | L | X | X | Write SRAM | Input Data | Active |
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x8B45 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Disable | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data | Active[10] |

The software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads, with $\overline{WE}$ kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. After the $t_{STORE}$ cycle time is fulfilled, the SRAM is activated again for the read and write operation.

## Software RECALL

Data is transferred from nonvolatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. After the $t_{RECALL}$ cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

**Notes**
9. While there are 17 address lines on the CY14B101LA (16 address lines on the CY14B101NA), only the 13 address lines ($A_{14}$ - $A_2$) are used to control software modes. Rest of the address lines are don't care.
10. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.

**Table 2. Mode Selection** (continued)

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$[3] | $A_{15}$ - $A_0$[9] | Mode | I/O | Power |
|---|---|---|---|---|---|---|
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x4B46 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Enable | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data | Active[10] |
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x8FC0 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile STORE | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active $I_{CC2}$[10] |
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x4C63 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile Recall | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active[10] |

## Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is reenabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the Software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or reenabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

## Data Protection

The CY14B101LA/CY14B101NA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when $V_{CC}$ is less than $V_{SWITCH}$. If the CY14B101LA/CY14B101NA is in a write mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after $t_{LZHSB}$ ($\overline{HSB}$ to output active). This protects against inadvertent writes during power up or brown out conditions.

## Noise Considerations

Refer to CY application note AN1064.

## Best Practices

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in this nvSRAM product are delivered from Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (for example, autostore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The $V_{CAP}$ value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum $V_{CAP}$ value because the nvSRAM internal algorithm calculates $V_{CAP}$ charge and discharge time based on this max $V_{CAP}$ value. Customers that want to use a larger $V_{CAP}$ value to make sure there is extra store charge and store time should discuss their $V_{CAP}$ size selection with Cypress to understand any impact on the $V_{CAP}$ voltage level at the end of a $t_{RECALL}$ period.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Maximum Accumulated Storage Time:

At 150°C Ambient Temperature..... 1000h

At 85°C Ambient Temperature..... 20 Years

Ambient Temperature with Power Applied .. –55°C to +150°C

Supply Voltage on $V_{CC}$ Relative to GND..... –0.5V to 4.1V

Voltage Applied to Outputs in High-Z State –0.5V to $V_{CC}$ + 0.5V

Input Voltage ..... –0.5V to Vcc+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential..... –2.0V to $V_{CC}$ + 2.0V

Package Power Dissipation Capability ($T_A$ = 25°C) ..... 1.0W

Surface Mount Pb Soldering Temperature (3 Seconds)..... +260°C

DC Output Current (1 output at a time, 1s duration)..... 15 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch Up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 2.7V to 3.6V |
| Industrial | –40°C to +85°C | |

## DC Electrical Characteristics

Over the Operating Range ($V_{CC}$ = 2.7V to 3.6V)

| Parameter | Description | Test Conditions | | Min | Typ[11] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | | 2.7 | 3.0 | 3.6 | V |
| $I_{CC1}$ | Average $V_{CC}$ Current | $t_{RC}$ = 20 ns<br>$t_{RC}$ = 25 ns<br>$t_{RC}$ = 45 ns<br>Values obtained without output loads ($I_{OUT}$ = 0 mA) | Commercial | | | 65<br>65<br>50 | mA<br>mA<br>mA |
| | | | Industrial | | | 70<br>70<br>52 | mA<br>mA<br>mA |
| $I_{CC2}$ | Average $V_{CC}$ Current during STORE | All Inputs Don't Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | | | | 10 | mA |
| $I_{CC3}$ | Average $V_{CC}$ Current at $t_{RC}$= 200 ns, $V_{CC}$ (Typ), 25°C | All I/P cycling at CMOS levels.<br>Values obtained without output loads ($I_{OUT}$ = 0 mA) | | | 35 | | mA |
| $I_{CC4}$ | Average $V_{CAP}$ Current during AutoStore Cycle | All Inputs Don't Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | | | | 5 | mA |
| $I_{SB}$ | $V_{CC}$ Standby Current | $\overline{CE} \geq (V_{CC} - 0.2V)$. $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$.<br>Standby current level after nonvolatile cycle is complete.<br>Inputs are static. f = 0 MHz | | | | 5 | mA |
| $I_{IX}$[12] | Input Leakage Current (except HSB) | $V_{CC}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$ | | –1 | | +1 | µA |
| | Input Leakage Current (for HSB) | $V_{CC}$ = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$ | | –100 | | +1 | µA |
| $I_{OZ}$ | Off-State Output Leakage Current | $V_{CC}$ = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{BHE}/\overline{BLE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$ | | –1 | | +1 | µA |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$+0.5 | V |
| $V_{IL}$ | Input LOW Voltage | | | $V_{SS}$–0.5 | | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OUT}$ = –2 mA | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OUT}$ = 4 mA | | | | 0.4 | V |
| $V_{CAP}$ | Storage Capacitor | Between $V_{CAP}$ pin and $V_{SS}$, 5V Rated | | 61 | 68 | 180 | µF |

**Notes**

11. Typical values are at 25°C, $V_{CC}$= $V_{CC}$ (Typ). Not 100% tested.
12. The HSB pin has $I_{OUT}$ = -2 uA for $V_{OH}$ of 2.4V when both active high and low drivers are disabled. When they are enabled standard $V_{OH}$ and $V_{OL}$ are valid. This parameter is characterized but not tested.

## Data Retention and Endurance

| Parameter | Description | Min | Unit |
|---|---|---|---|
| $DATA_R$ | Data Retention | 20 | Years |
| $NV_C$ | Nonvolatile STORE Operations | 200 | K |

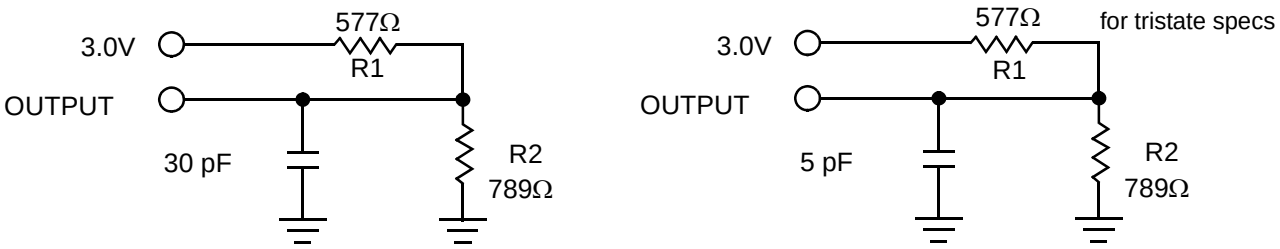
## Capacitance

| Parameter[13] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = $V_{CC}$ (Typ) | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | 7 | pF |

## Thermal Resistance

| Parameter[13] | Description | Test Conditions | 54-TSOP II | 48-SSOP | 44-TSOP II | 32-SOIC | Unit |
|---|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 30.73 | TBD | 31.11 | TBD | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 6.08 | TBD | 5.56 | TBD | °C/W |

**Figure 5. AC Test Loads**




## AC Test Conditions

Input Pulse Levels ..... 0V to 3V
Input Rise and Fall Times (10% - 90%) ..... ≤3 ns
Input and Output Timing Reference Levels ..... 1.5V

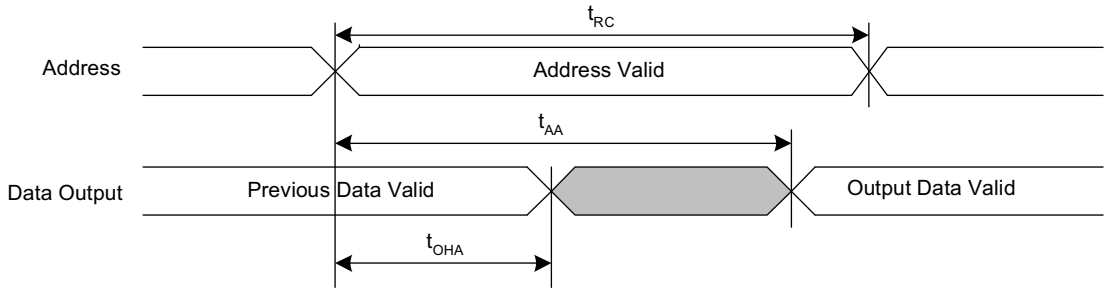
**Note**
13. These parameters are guaranteed by design and are not tested.

## AC Switching Characteristics

| Parameters | | Description | 20 ns | | 25 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Cypress Parameters | Alt Parameters | | Min | Max | Min | Max | Min | Max | |
| **SRAM Read Cycle** | | | | | | | | | |
| $t_{ACE}$ | $t_{ACS}$ | Chip Enable Access Time | | 20 | | 25 | | 45 | ns |
| $t_{RC}$[14] | $t_{RC}$ | Read Cycle Time | 20 | | 25 | | 45 | | ns |
| $t_{AA}$[15] | $t_{AA}$ | Address Access Time | | 20 | | 25 | | 45 | ns |
| $t_{DOE}$ | $t_{OE}$ | Output Enable to Data Valid | | 10 | | 12 | | 20 | ns |
| $t_{OHA}$[15] | $t_{OH}$ | Output Hold After Address Change | 3 | | 3 | | 3 | | ns |
| $t_{LZCE}$[13, 16] | $t_{LZ}$ | Chip Enable to Output Active | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$[13, 16] | $t_{HZ}$ | Chip Disable to Output Inactive | | 8 | | 10 | | 15 | ns |
| $t_{LZOE}$[13, 16] | $t_{OLZ}$ | Output Enable to Output Active | 0 | | 0 | | 0 | | ns |
| $t_{HZOE}$[13, 16] | $t_{OHZ}$ | Output Disable to Output Inactive | | 8 | | 10 | | 15 | ns |
| $t_{PU}$[13] | $t_{PA}$ | Chip Enable to Power Active | 0 | | 0 | | 0 | | ns |
| $t_{PD}$[13] | $t_{PS}$ | Chip Disable to Power Standby | | 20 | | 25 | | 45 | ns |
| $t_{DBE}$[13] | - | Byte Enable to Data Valid | | 10 | | 12 | | 20 | ns |
| $t_{LZBE}$[13] | - | Byte Enable to Output Active | 0 | | 0 | | 0 | | ns |
| $t_{HZBE}$[13] | - | Byte Disable to Output Inactive | | 8 | | 10 | | 15 | ns |
| **SRAM Write Cycle** | | | | | | | | | |
| $t_{WC}$ | $t_{WC}$ | Write Cycle Time | 20 | | 25 | | 45 | | ns |
| $t_{PWE}$ | $t_{WP}$ | Write Pulse Width | 15 | | 20 | | 30 | | ns |
| $t_{SCE}$ | $t_{CW}$ | Chip Enable To End of Write | 15 | | 20 | | 30 | | ns |
| $t_{SD}$ | $t_{DW}$ | Data Setup to End of Write | 8 | | 10 | | 15 | | ns |
| $t_{HD}$ | $t_{DH}$ | Data Hold After End of Write | 0 | | 0 | | 0 | | ns |
| $t_{AW}$ | $t_{AW}$ | Address Setup to End of Write | 15 | | 20 | | 30 | | ns |
| $t_{SA}$ | $t_{AS}$ | Address Setup to Start of Write | 0 | | 0 | | 0 | | ns |
| $t_{HA}$ | $t_{WR}$ | Address Hold After End of Write | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$[13, 16,17] | $t_{WZ}$ | Write Enable to Output Disable | | 8 | | 10 | | 15 | ns |
| $t_{LZWE}$[13, 16] | $t_{OW}$ | Output Active after End of Write | 3 | | 3 | | 3 | | ns |
| $t_{BW}$ | - | Byte Enable to End of Write | 15 | | 20 | | 30 | | ns |

## Switching Waveforms

**Figure 6. SRAM Read Cycle #1: Address Controlled** [14, 15, 18]




**Notes**
14. WE must be HIGH during SRAM read cycles.
15. Device is continuously selected with CE, OE and BHE/BLE LOW.
16. Measured ±200 mV from steady state output voltage.
17. If WE is low when CE goes low, the outputs remain in the high impedance state.
18. HSB must remain HIGH during Read and Write cycles.

**Figure 7. SRAM Read Cycle #2: $\overline{CE}$ and $\overline{OE}$ Controlled** [3, 14, 18]

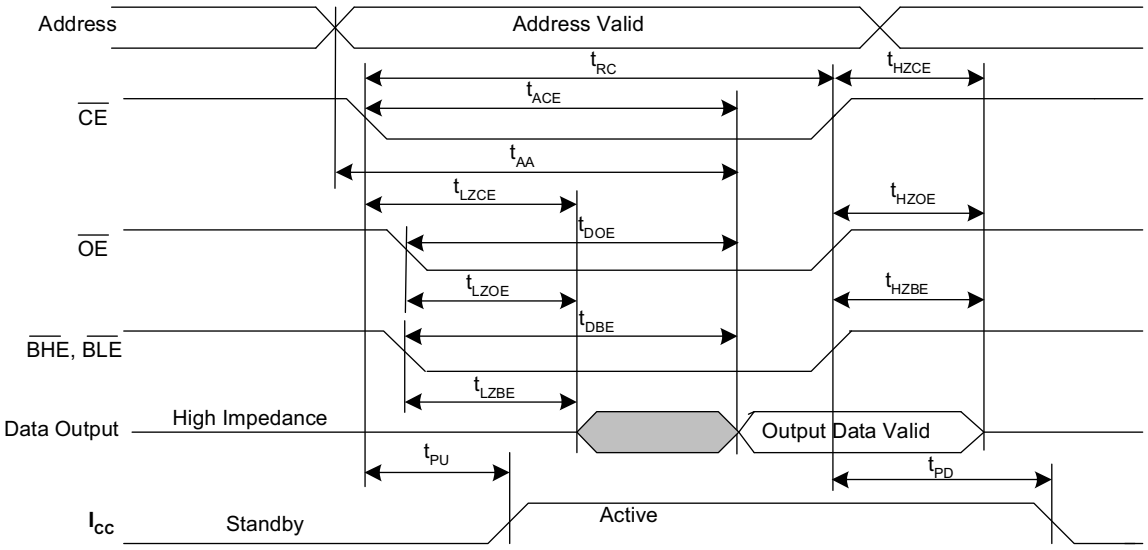
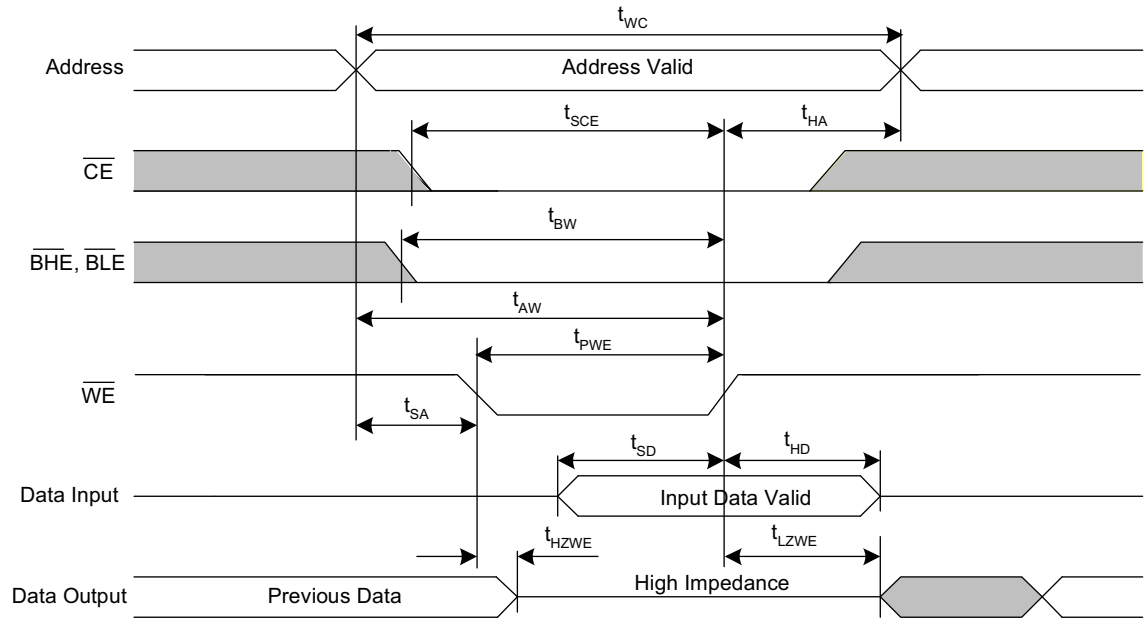



**Figure 8. SRAM Write Cycle #1: $\overline{WE}$ Controlled** [3, 17, 18, 21]




**Note**
21. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

**Figure 9. SRAM Write Cycle #2: $\overline{CE}$ Controlled** [3, 17, 18, 21]

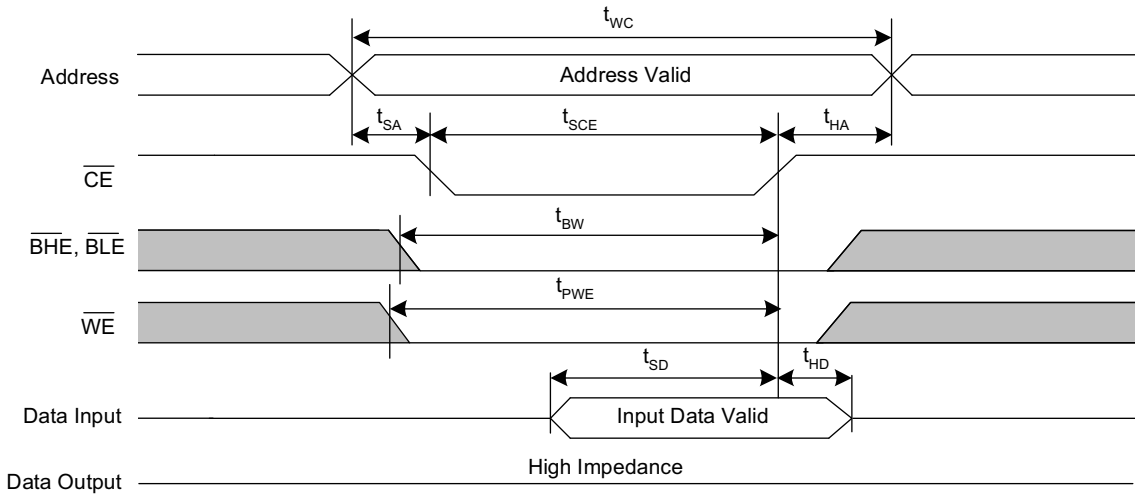
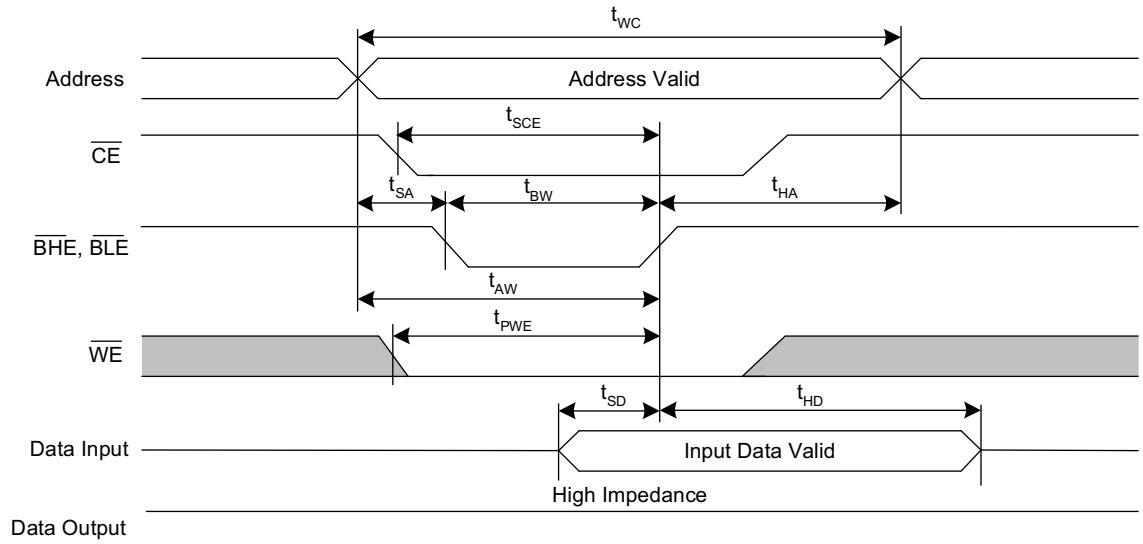



**Figure 10. SRAM Write Cycle #3: $\overline{BHE}$ and $\overline{BLE}$ Controlled** [3, 17, 18, 21]

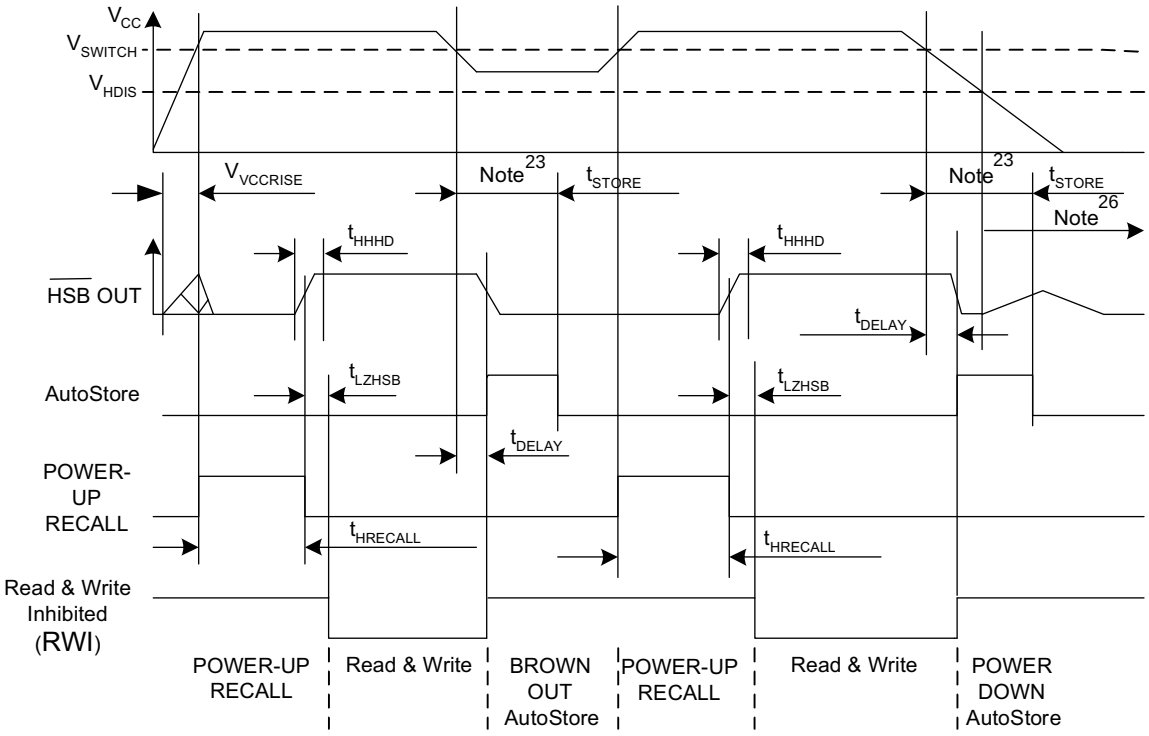


## AutoStore/Power Up RECALL

| Parameters | Description | 20 ns | | 25 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{HRECALL}$ [27] | Power Up RECALL Duration | | 20 | | 20 | | 20 | ms |
| $t_{STORE}$ [23] | STORE Cycle Duration | | 8 | | 8 | | 8 | ms |
| $t_{DELAY}$ [24] | Time Allowed to Complete SRAM Write Cycle | | 20 | | 25 | | 25 | ns |
| $V_{SWITCH}$ | Low Voltage Trigger Level | | 2.65 | | 2.65 | | 2.65 | V |
| $t_{VCCRISE}$ [13] | VCC Rise Time | 150 | | 150 | | 150 | | µs |
| $V_{HDIS}$ [13] | $\overline{HSB}$ Output Disable Voltage | | 1.9 | | 1.9 | | 1.9 | V |
| $t_{LZHSB}$ [13] | $\overline{HSB}$ To Output Active Time | | 5 | | 5 | | 5 | µs |
| $t_{HHHD}$ [13] | HSB High Active Time | | 500 | | 500 | | 500 | ns |

## Switching Waveforms

**Figure 11. AutoStore or Power Up RECALL** [27]




**Notes**
22. $t_{HRECALL}$ starts from the time $V_{CC}$ rises above $V_{SWITCH}$.
23. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
24. On a Hardware Store and AutoStore initiation, SRAM write operation continues to be enabled for time $t_{DELAY}$.
25. Read and Write cycles are ignored during STORE, RECALL, and while VCC is below $V_{SWITCH}$.
26. HSB pin is driven high to VCC only by internal 100 kΩ resistor, HSB driver is disabled.

## Software Controlled STORE/RECALL Cycle

| Parameters[27, 28] | Description | 20 ns | | 25 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | STORE/RECALL Initiation Cycle Time | 20 | | 25 | | 45 | | ns |
| $t_{SA}$ | Address Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{CW}$ | Clock Pulse Width | 15 | | 20 | | 30 | | ns |
| $t_{HA}$ | Address Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{RECALL}$ | RECALL Duration | | 200 | | 200 | | 200 | µs |

## Switching Waveforms

**Figure 12. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle[28]**

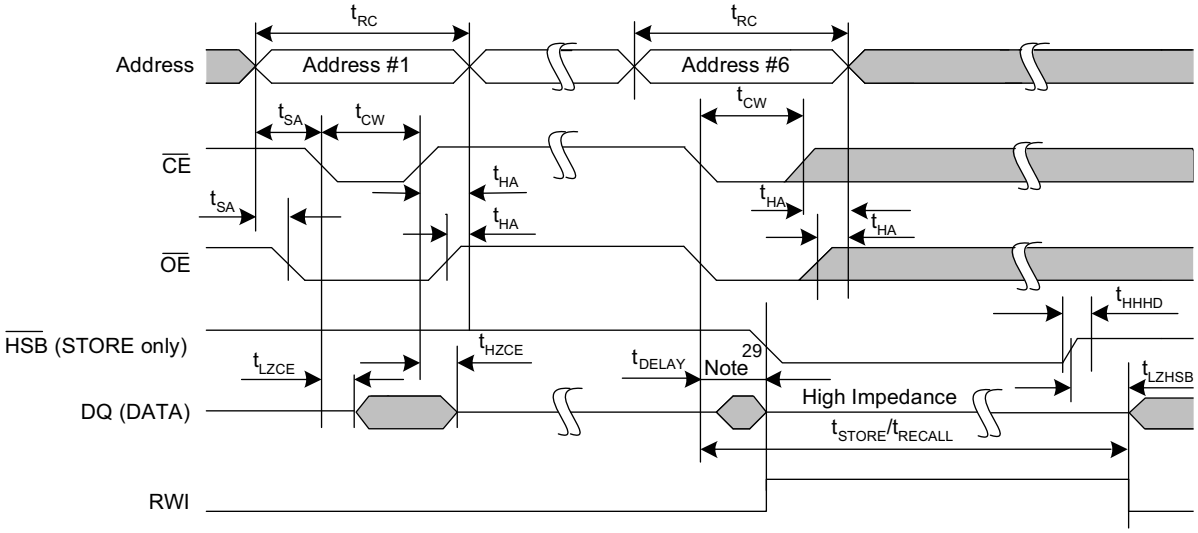
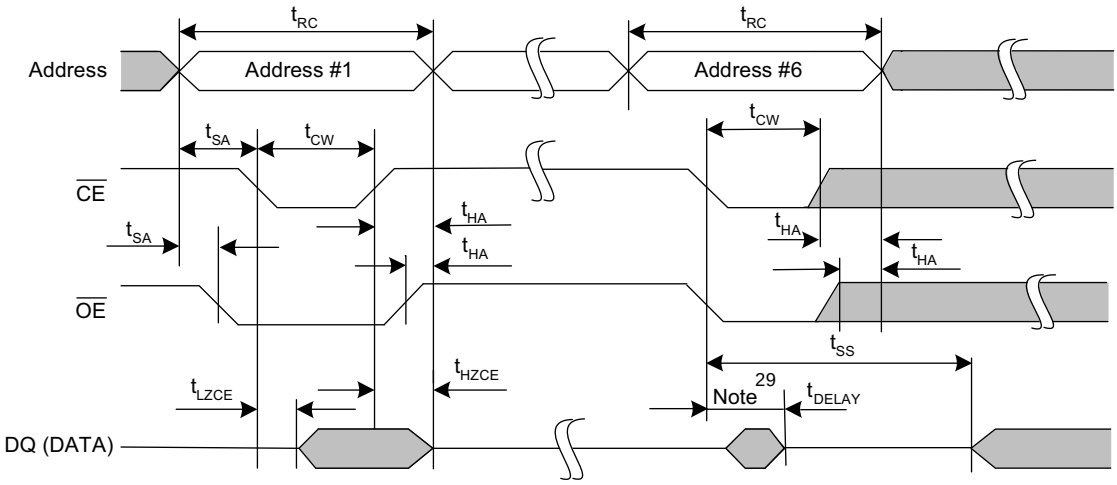



**Figure 13. Autostore Enable/Disable Cycle**




**Notes**
27. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
28. The six consecutive addresses must be read in the order listed in Table 2 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles.
29. DQ output data at the sixth read may be invalid since the output is disabled at $t_{DELAY}$ time.

## Hardware STORE Cycle

| Parameters | Description | 20 ns | | 25 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{DHSB}$ | $\overline{HSB}$ To Output Active Time when write latch not set | | 20 | | 25 | | 25 | ns |
| $t_{PHSB}$ | Hardware STORE Pulse Width | 15 | | 15 | | 15 | | ns |
| $t_{SS}$ [29, 30] | Soft Sequence Processing Time | | 100 | | 100 | | 100 | µs |

## Switching Waveforms

**Figure 14. Hardware STORE Cycle**[23]

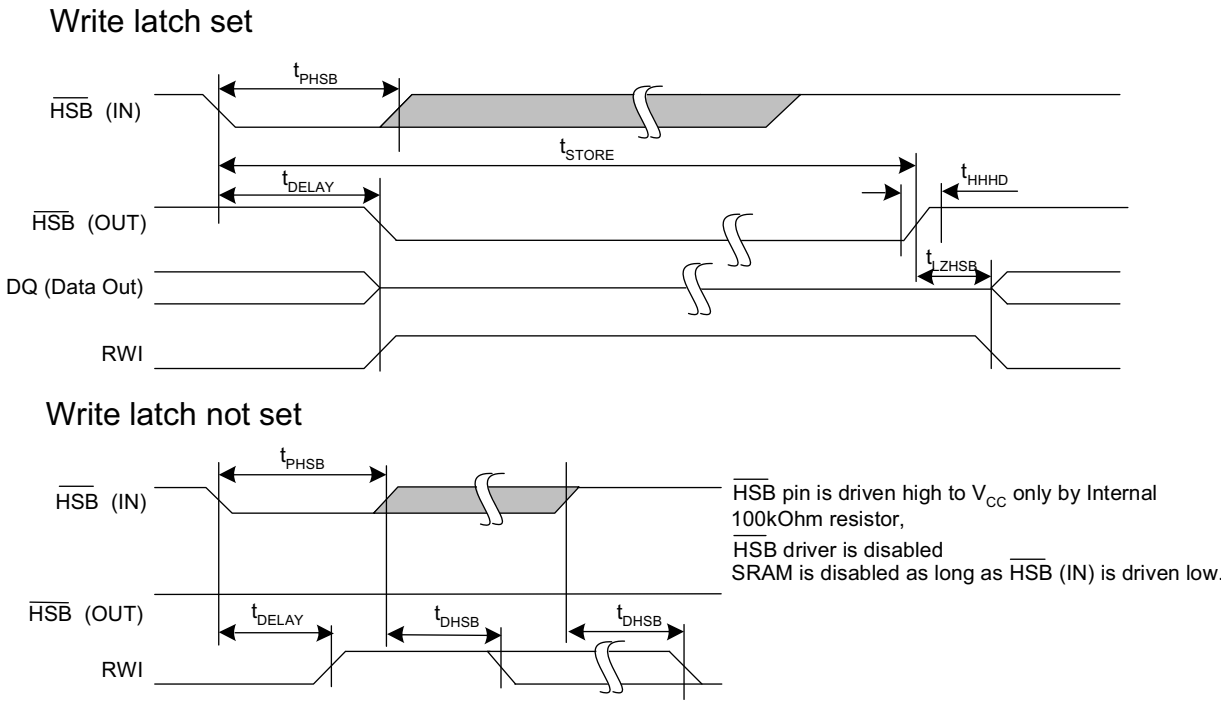
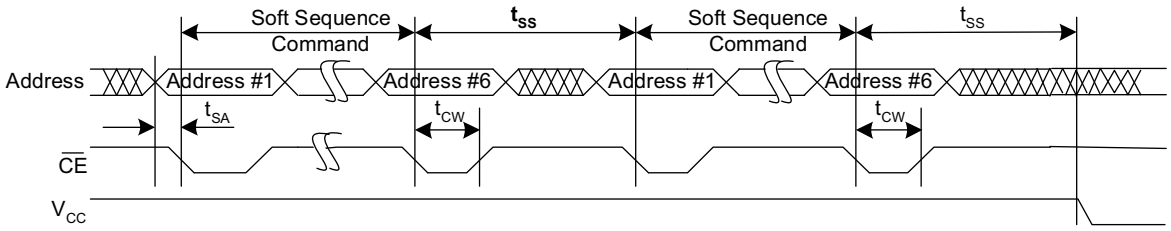



**Figure 15. Soft Sequence Processing**[29, 30]




**Notes**
29. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
30. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

## Truth Table For SRAM Operations

$\overline{HSB}$ must remain HIGH for SRAM operations.

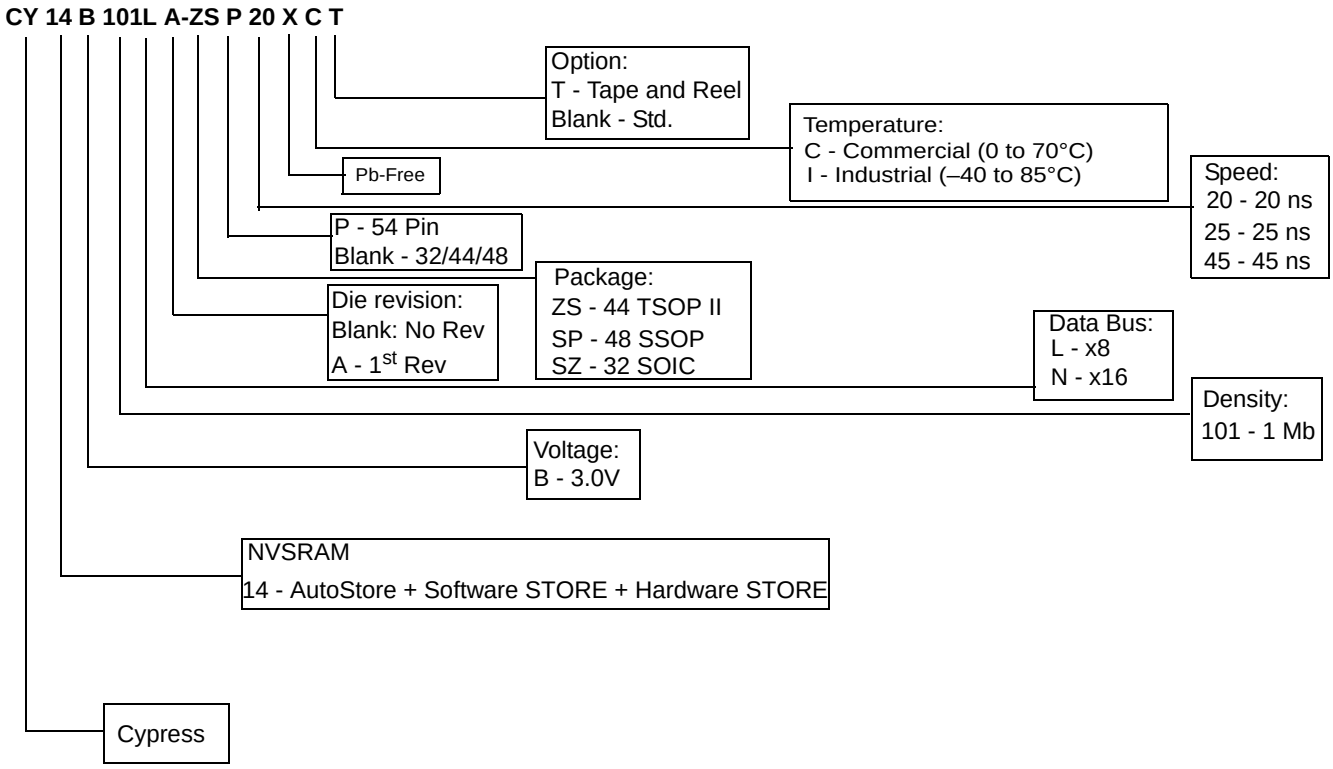
**Table 3. Truth Table for x8 Configuration**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs[2] | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power Down | Standby |
| L | H | L | Data Out ($DQ_0$–$DQ_7$); | Read | Active |
| L | H | H | High Z | Output Disabled | Active |
| L | L | X | Data in ($DQ_0$–$DQ_7$); | Write | Active |

**Table 4. Truth Table for x16 Configuration**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$[3] | $\overline{BLE}$[3] | Inputs/Outputs[2] | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | Deselect/Power Down | Standby |
| L | X | X | H | H | High-Z | Output Disabled | Active |
| L | H | L | L | L | Data Out ($DQ_0$–$DQ_{15}$) | Read | Active |
| L | H | L | H | L | Data Out ($DQ_0$–$DQ_7$); $DQ_8$–$DQ_{15}$ in High-Z | Read | Active |
| L | H | L | L | H | Data Out ($DQ_8$–$DQ_{15}$); $DQ_0$–$DQ_7$ in High-Z | Read | Active |
| L | H | H | L | L | High-Z | Output Disabled | Active |
| L | H | H | H | L | High-Z | Output Disabled | Active |
| L | H | H | L | H | High-Z | Output Disabled | Active |
| L | L | X | L | L | Data In ($DQ_0$–$DQ_{15}$) | Write | Active |
| L | L | X | H | L | Data In ($DQ_0$–$DQ_7$); $DQ_8$–$DQ_{15}$ in High-Z | Write | Active |
| L | L | X | L | H | Data In ($DQ_8$–$DQ_{15}$); $DQ_0$–$DQ_7$ in High-Z | Write | Active |

## Part Numbering Nomenclature



## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 20 | CY14B101LA-ZS20XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14B101LA-ZS20XC | 51-85087 | 44-pin TSOP II | |
| | CY14B101LA-SP20XCT | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SP20XC | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SZ20XCT | 51-85127 | 32-pin SOIC | |
| | CY14B101LA-SZ20XC | 51-85127 | 32-pin SOIC | |
| | CY14B101NA-ZS20XCT | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZS20XC | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZSP20XCT | 51-85160 | 54-pin TSOP II | |
| | CY14B101NA-ZSP20XC | 51-85160 | 54-pin TSOP II | |
| | CY14B101LA-ZS20XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14B101LA-ZS20XI | 51-85087 | 44-pin TSOP II | |
| | CY14B101LA-SP20XIT | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SP20XI | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SZ20XIT | 51-85127 | 32-pin SOIC | |
| | CY14B101LA-SZ20XI | 51-85127 | 32-pin SOIC | |
| | CY14B101NA-ZS20XIT | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZS20XI | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZSP20XIT | 51-85160 | 54-pin TSOP II | |
| | CY14B101NA-ZSP20XI | 51-85160 | 54-pin TSOP II | |
| 25 | CY14B101LA-ZS25XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14B101LA-ZS25XC | 51-85087 | 44-pin TSOP II | |
| | CY14B101LA-SP25XCT | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SP25XC | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SZ25XCT | 51-85127 | 32-pin SOIC | |
| | CY14B101LA-SZ25XC | 51-85127 | 32-pin SOIC | |
| | CY14B101NA-ZS25XCT | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZS25XC | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZSP25XCT | 51-85160 | 54-pin TSOP II | |
| | CY14B101NA-ZSP25XC | 51-85160 | 54-pin TSOP II | |
| | CY14B101LA-ZS25XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14B101LA-ZS25XI | 51-85087 | 44-pin TSOP II | |
| | CY14B101LA-SP25XIT | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SP25XI | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SZ25XIT | 51-85127 | 32-pin SOIC | |
| | CY14B101LA-SZ25XI | 51-85127 | 32-pin SOIC | |
| | CY14B101NA-ZS25XIT | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZS25XI | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZSP25XIT | 51-85160 | 54-pin TSOP II | |
| | CY14B101NA-ZSP25XI | 51-85160 | 54-pin TSOP II | |

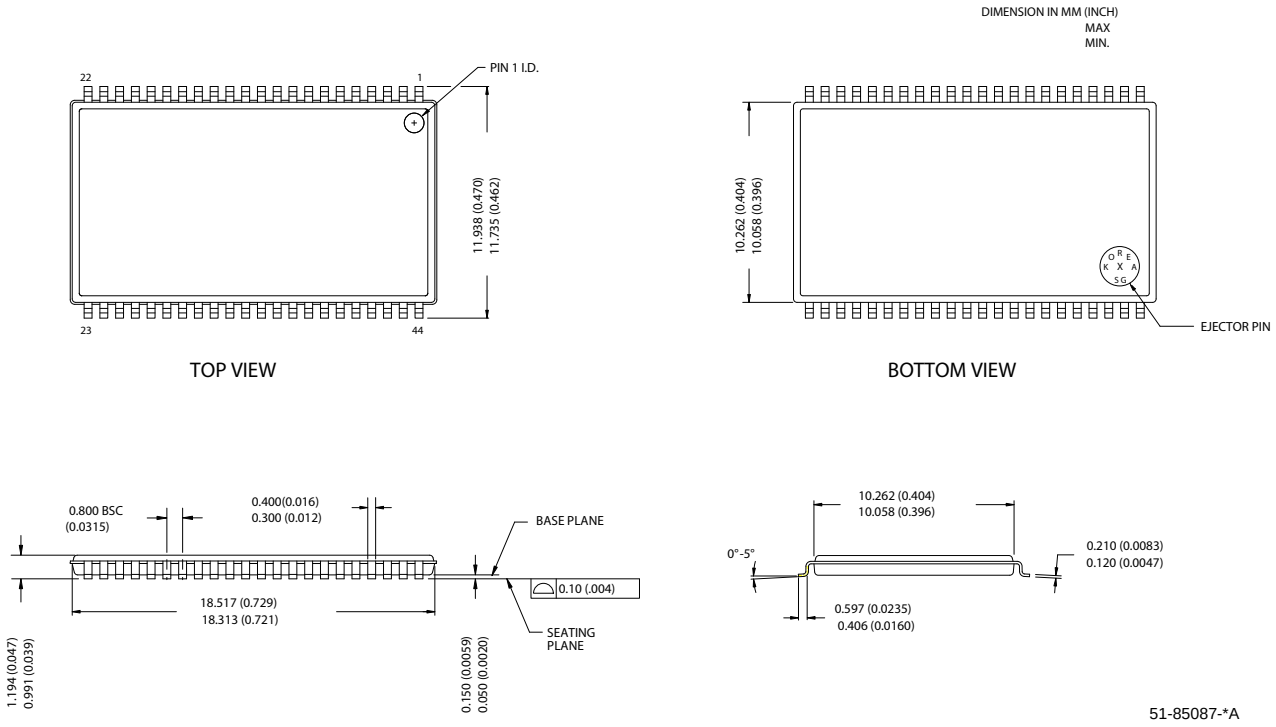
## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY14B101LA-ZS45XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14B101LA-ZS45XC | 51-85087 | 44-pin TSOP II | |
| | CY14B101LA-SP45XCT | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SP45XC | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SZ45XCT | 51-85127 | 32-pin SOIC | |
| | CY14B101LA-SZ45XC | 51-85127 | 32-pin SOIC | |
| | CY14B101NA-ZS45XCT | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZS45XC | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZSP45XCT | 51-85160 | 54-pin TSOP II | |
| | CY14B101NA-ZSP45XC | 51-85160 | 54-pin TSOP II | |
| | CY14B101LA-ZS45XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14B101LA-ZS45XI | 51-85087 | 44-pin TSOP II | |
| | CY14B101LA-SP45XIT | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SP45XI | 51-85061 | 48-pin SSOP | |
| | CY14B101LA-SZ45XIT | 51-85127 | 32-pin SOIC | |
| | CY14B101LA-SZ45XI | 51-85127 | 32-pin SOIC | |
| | CY14B101NA-ZS45XIT | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZS45XI | 51-85087 | 44-pin TSOP II | |
| | CY14B101NA-ZSP45XIT | 51-85160 | 54-pin TSOP II | |
| | CY14B101NA-ZSP45XI | 51-85160 | 54-pin TSOP II | |

All parts are Pb-free. This table contains Preliminary information. Contact your local Cypress sales representative for availability of these parts.

## Package Diagrams

**Figure 16. 44-Pin TSOP II (51-85087)**



## Package Diagrams (continued)

**Figure 17. 48-Pin SSOP (51-85061)**

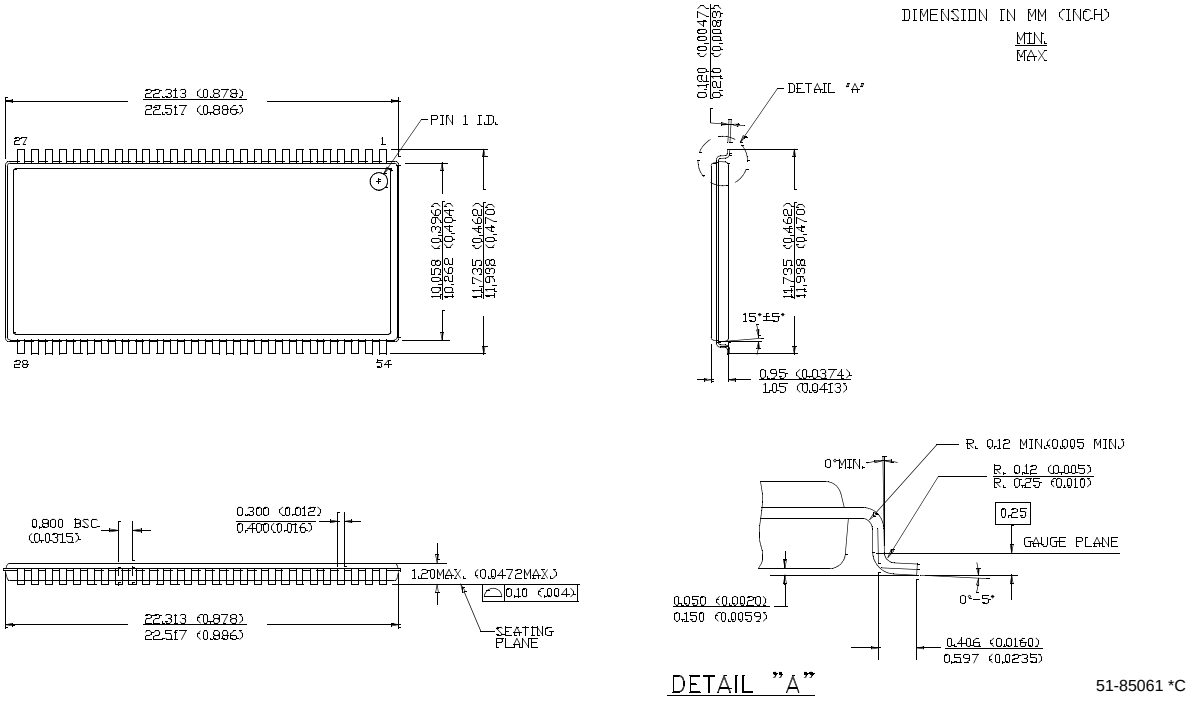
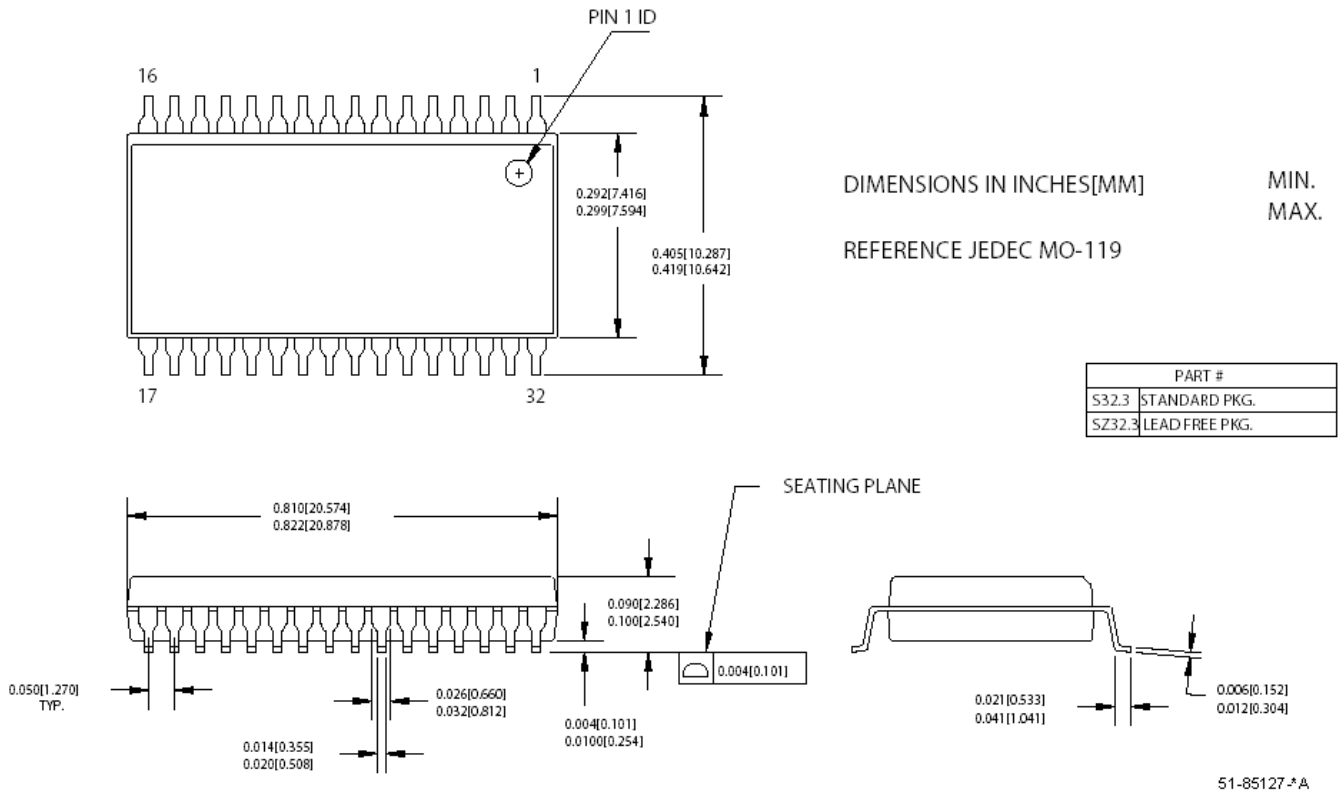
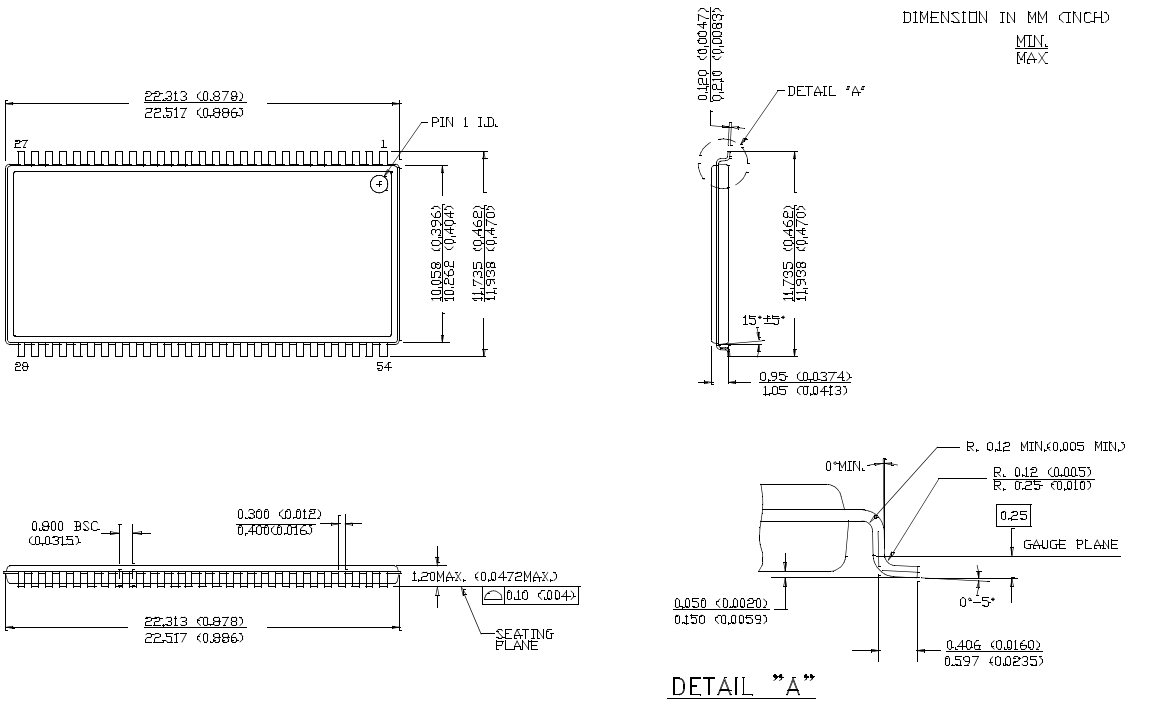



**Figure 18. 32-Pin SOIC (51-85127)**



## Package Diagrams (continued)

**Figure 19. 54-Pin TSOP II (51-85160)**



## Document History Page

| Document Title: CY14B101LA, CY14B101NA 1 Mbit (128K x 8/64K x 16) nvSRAM<br>Document Number: 001-42879 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 2050747 | See ECN | UNC/PYRS | New Data Sheet |
| *A | 2607447 | 11/14/2008 | GVCH/AESA | Removed 15 ns access speed<br>Updated “Features”<br>Updated Logic block diagram<br>Added footnote 1 2, 3 and 7<br>Pin definition: Updated WE, HSB and NC pin description<br>Page 4: Updated SRAM READ, SRAM WRITE, Autostore operation description<br>Updated Figure 4<br>Page 4: Updated Hardware store operation and Hardware RECALL (Power up)description<br>Page 4: Updated Software store and software recall description<br>Footnote 1 and 11 referenced for Mode selection Table<br>Added footnote 11<br>Updated footnote 9 and 10<br>Page 6: updated Data protection description<br>Maximum Ratings:Added Max. Accumulated storage time<br>Changed Output short circuit current parameter name to DC output current<br>Changed $I_{CC2}$ from 6mA to 10mA<br>Changed $I_{CC3}$ from 15mA to 35mA<br>Changed $I_{CC4}$ from 6mA to 5mA<br>Changed $I_{SB}$ from 3mA to 5mA<br>Added $I_{IX}$ for HSB<br>Updated $I_{CC1}$, $I_{CC3}$, $I_{SB}$ and $I_{OZ}$ Test conditions<br>Changed $V_{CAP}$ voltage min value from 68uF to 61uF<br>Added $V_{CAP}$ voltage max value to 180uF<br>Updated footnote 12 and 13<br>Added footnote 14<br>Added Data retention and Endurance Table<br>Added thermal resistance value to 48-pin FBGA and 44-pin TSOP II packages<br>Updated Input Rise and Fall time in AC test Conditions<br>Referenced footnote 17 to $t_{OHA}$ parameter<br>Updated All switching waveforms<br>Updated footnote 17<br>Added footnote 20<br>Added Figure 10 (SRAM WRITE CYCLE:BHE and BLE controlled)<br>Changed $t_{STORE}$ max value from 12.5ms to 8ms<br>Updated $t_{DELAY}$ value<br>Added $V_{HDIS}$, $t_{HHHD}$ and $t_{LZHSB}$ parameters<br>Updated footnote 24<br>Added footnote 26 and 27<br>Software controlled STORE/RECALL Table: Changed $t_{AS}$ to $t_{SA}$<br>Changed $t_{GHAX}$ to $t_{HA}$<br>Changed $t_{HA}$ value from 1ns to 0 ns<br>Added Figure 13<br>Added $t_{DHSB}$ parameter<br>Changed $t_{HLHX}$ to $t_{PHSB}$<br>Updated $t_{SS}$ from 70us to 100us<br>Added truth table for SRAM operations<br>Updated ordering information and part numbering nomenclature |
| *B | 2654484 | 02/05/09 | GVCH/PYRS | Changed the data sheet from Advance information to Preliminary<br>Referenced Note 15 to parameters $t_{LZCE}$, $t_{HZCE}$, $t_{LZOE}$, $t_{HZOE}$, $t_{LZWE}$ and $t_{HZWE}$<br>Updated Figure 12 |

| Document Title: CY14B101LA, CY14B101NA 1 Mbit (128K x 8/64K x 16) nvSRAM<br>Document Number: 001-42879 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| *C | 2733909 | 07/09/09 | GVCH/AESA | Removed 48-ball FBGA package and added 54-pin TSOP II Package<br>Corrected typo error in pin diagram of 48-pin SSOP<br>Page 4; Added note to AutoStore Operation description<br>Page 4; Updated Hardware STORE (HSB) Operation description<br>Page 5; Updated Software STORE Operation description<br>Added best practices<br>Updated $V_{HDIS}$ parameter description<br>Updated $t_{DELAY}$ parameter description<br>Updated footnote 24 and added footnote 29 |

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