Low-Voltage, Low r_{ON}, SPDT Audio Switch with Negative Swing Capability

DESCRIPTION

The DG2612/2613 is a low on-resistance, single-pole/double-throw monolithic CMOS analog switch with negative signal swing capability. It is designed for low voltage applications. The DG2612/2613 is ideal for portable and battery powered equipment, requiring high performance and efficient use of board space. In additional to the low on-resistance (1.0 Ω at 2.7 V), the DG2613 has a typical OFF Isolation and Crosstalk of - 67 dB and - 73 dB respectively.

The DG2612/2613 is built on Vishay Siliconix's low voltage process.

Break-before-make is guaranteed.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON}: 1.0 Ω at 2.7 V
- High Bandwidth

Pb-free
RoHS
COMPLIANT

BENEFITS

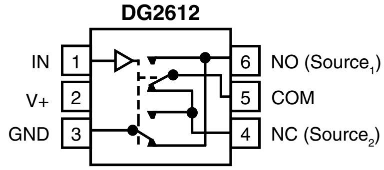
- Negative Signal Swing Capability
- Shunt Switch to Eliminate Switching Noise
- Simplified Design with Direct DC Coupling
- Space Saving SC-89 Package

APPLICATIONS

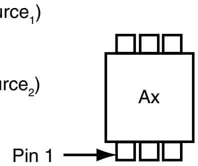
- Cellular Phones
- Portable Multimedia Players
- PDAs and Hand-held Devices
- Laptop Computers

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2612

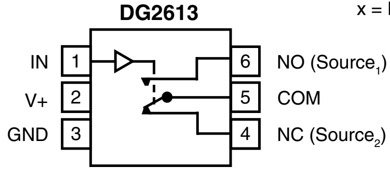


Top View
Device Marking: Dx



x = Date/Lot Traceability Code

DG2613



Top View
Device Marking: Ex

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

COMMERCIAL ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	SC-89 (SOT-666) Lead (Pb)-free with Tape and Reel	DG2612DX-T1-E3 DG2613DX-T1-E3

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Reference GND	V+		- 0.3 to + 6	V
	IN[a]		- 0.3 to (V+ + 0.3)	
	COM, NC, NO[a]		(V+ -6) to (V+ + 0.3)	
Continuous Current (NO, NC, COM pins)			± 150	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)			± 300	
Storage Temperature	D Suffix		- 65 to 150	°C
Power Dissipation (Packages)[b]	SC-89[c]		172	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 2.15 mW/°C above 70 °C.

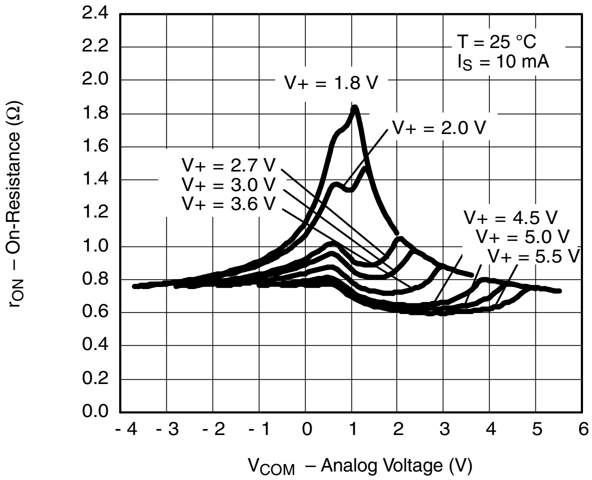
SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 V or 1.4 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	 Typ[c]	 Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = - 1 V/0 V/1 V/2 V I_{NO}, I_{NC} = 10 mA	Room Full		1.0	1.4 1.6	Ω
r_{ON} Match[d]	Δr_{ON}		Room			0.1	
r_{ON} Flatness[d]	r_{ON} Flatness		Room			0.3	
Shunt Switch Resistance	R_{SH}	I_{NO} or I_{NC} = 10 mA, V+ = 2.7 V, DG2612 only	Full		150	300	Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC}= 1 V/3 V, V_{COM} = 3 V/1 V	Room Full	- 2 - 100		2 100	nA
	$I_{COM(off)}$		Room Full	- 2 - 100		2 100	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	- 2 - 100		2 100	
Digital Control							
Input High Voltage	V_{INH}	V+ = 1.8 V to 2.0 V	Full	1.0			V
		V+ = 2.7 V to 3.6 V		1.4			
		V+ = 4.2 V to 5.5 V		2.0			
Input Low Voltage	V_{INL}	V+ = 1.8 V to 2.0 V				0.4	
		V+ = 2.7 V to 3.6 V				0.5	
		V+ = 4.2 V to 5.5 V				0.8	
Input Capacitance	C_{in}		Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room Full		34	60 63	ns
Turn-Off Time	t_{OFF}		Room Full		10	35 37	
Break-Before-Make Time	t_{BBM}		Room	4	16		
Charge Injection[d] (DG2613)	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		2.4		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz DG2612	Room		- 61		dB
Crosstalk[d]	X_{TALK}		Room		- 67		
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz DG2613	Room		- 67		dB
Crosstalk[d]	X_{TALK}		Room		- 73		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		36		pF
Channel-On Capacitance[d]	C_{ON}		Room		95		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA

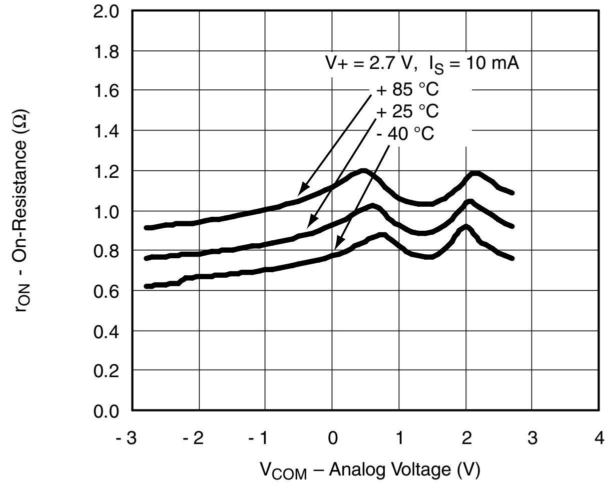
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

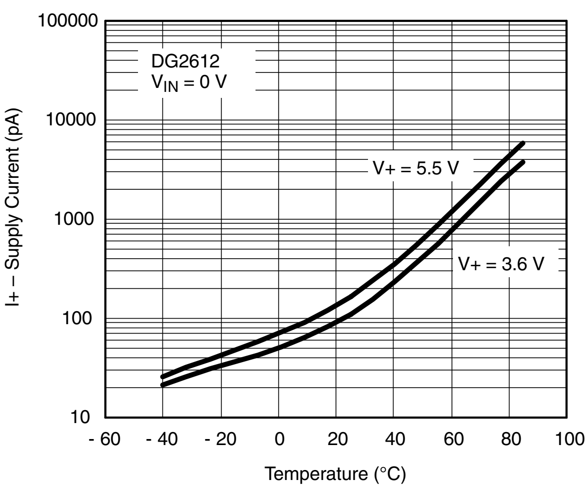
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



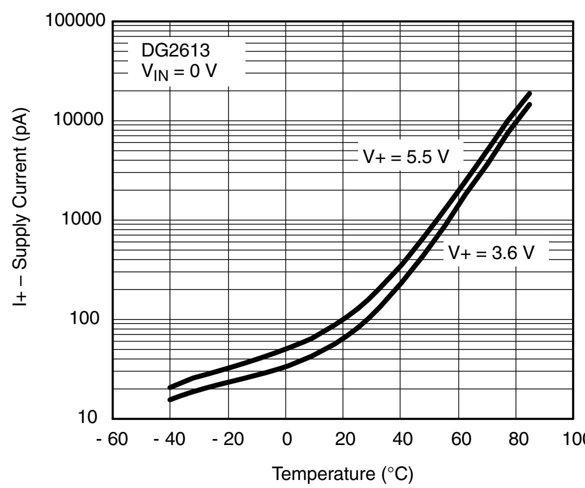
r_{ON} vs. V_{COM} and Supply Voltage



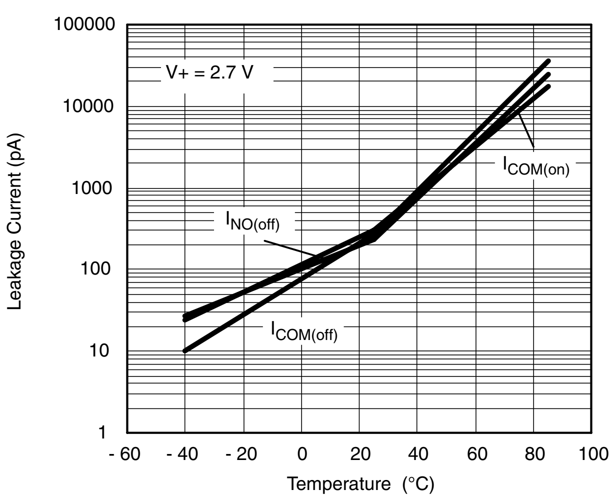
r_{ON} vs. Analog Voltage and Temperature



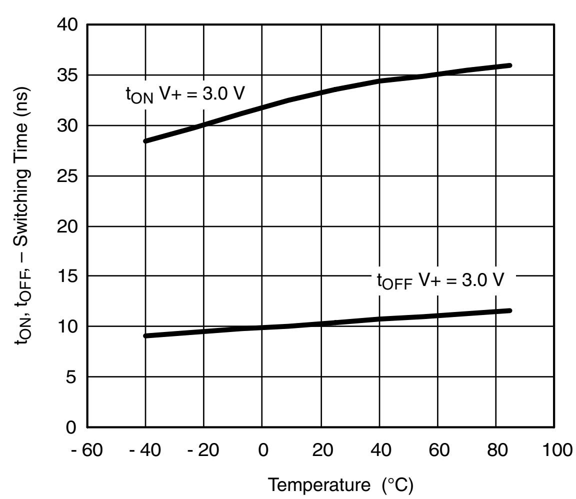
Supply Current vs. Temperature



Supply Current vs. Temperature

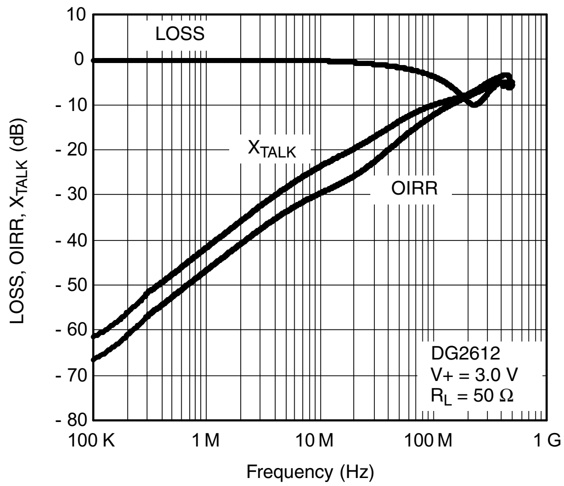


Leakage Current vs. Temperature

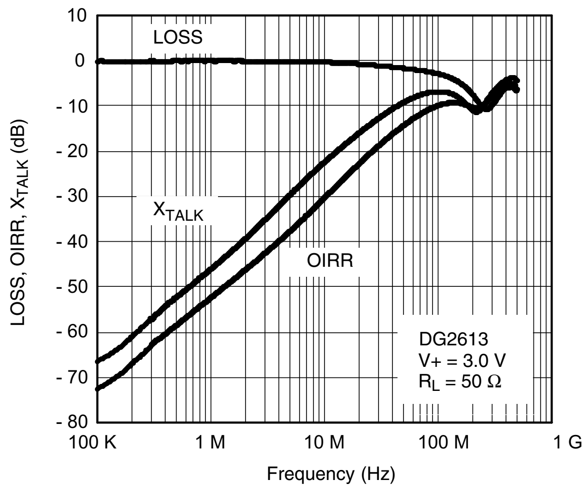


Switching Time vs. Temperature and Supply Voltage

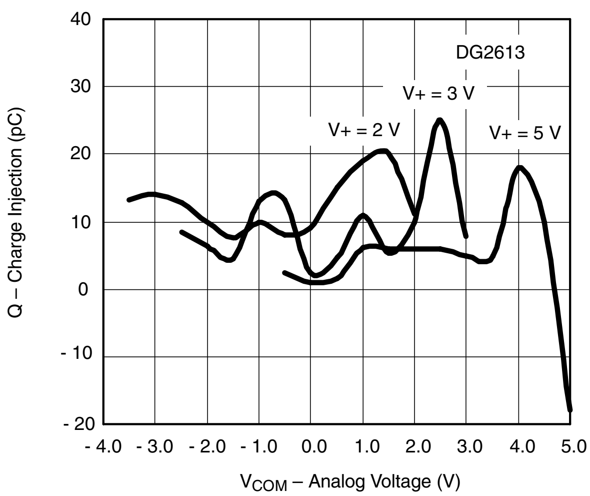
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



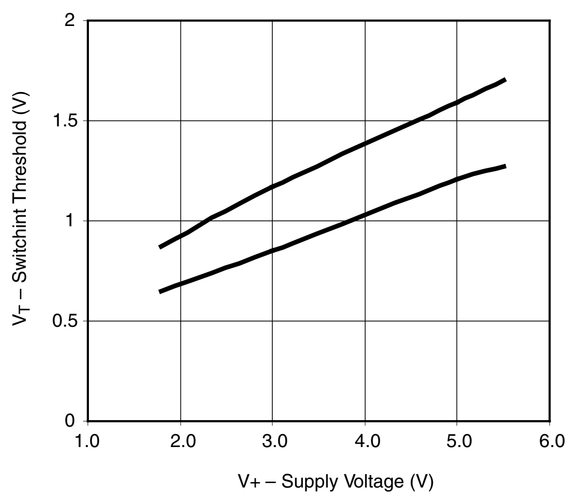
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

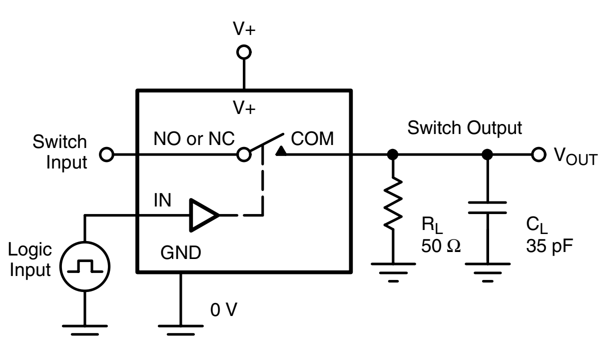


Charge Injection vs. Analog Voltage



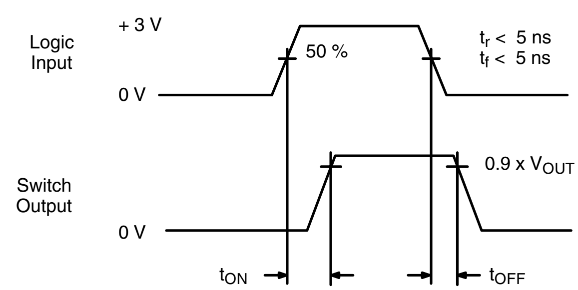
Switching Threshold vs. Supply Voltage

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

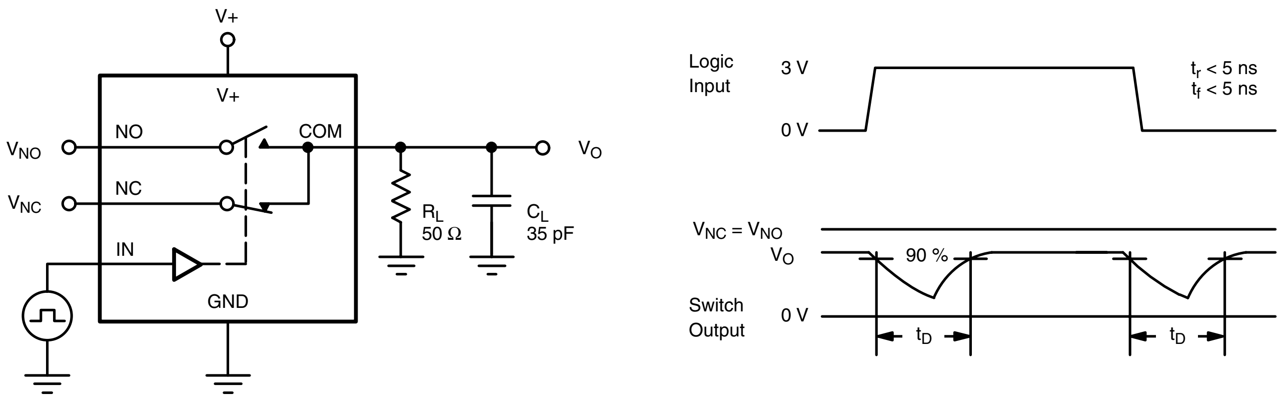
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

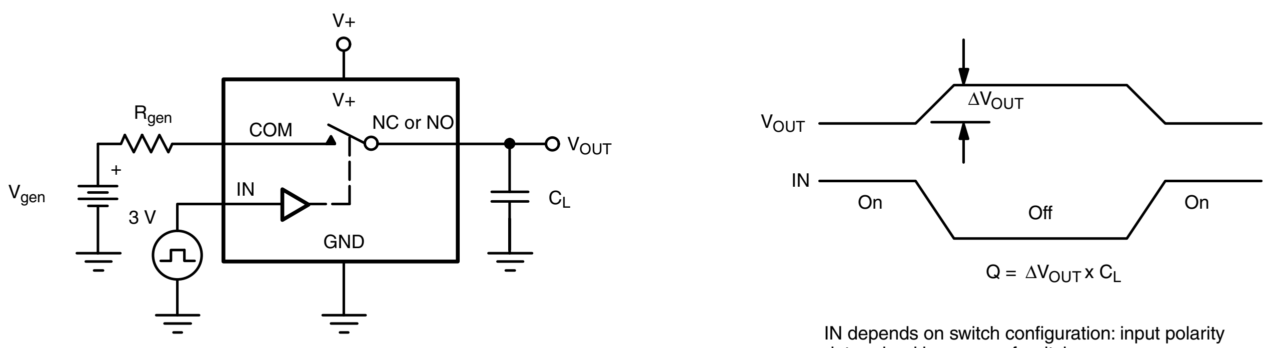
Figure 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

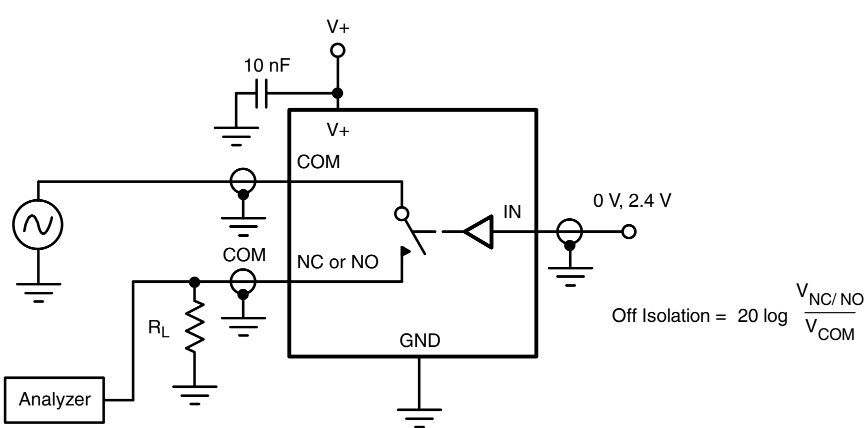


Figure 4. Off-Isolation

TEST CIRCUITS

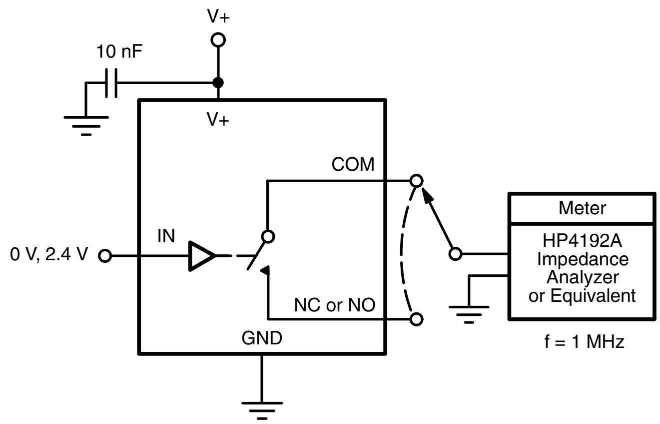


Figure 5. Channel Off/On Capacitance

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