CADEKA
Amplify the Human Experience

SPT7938

12-BIT, 40 MSPS, 170 mW A/D CONVERTER

FEATURES

- Monolithic 40 MSPS Analog-to-Digital Converter
- 170 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 20 pF Input Capacitance
- Selectable +3 V or +5 V Logic I/O

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation Is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Digital Communications

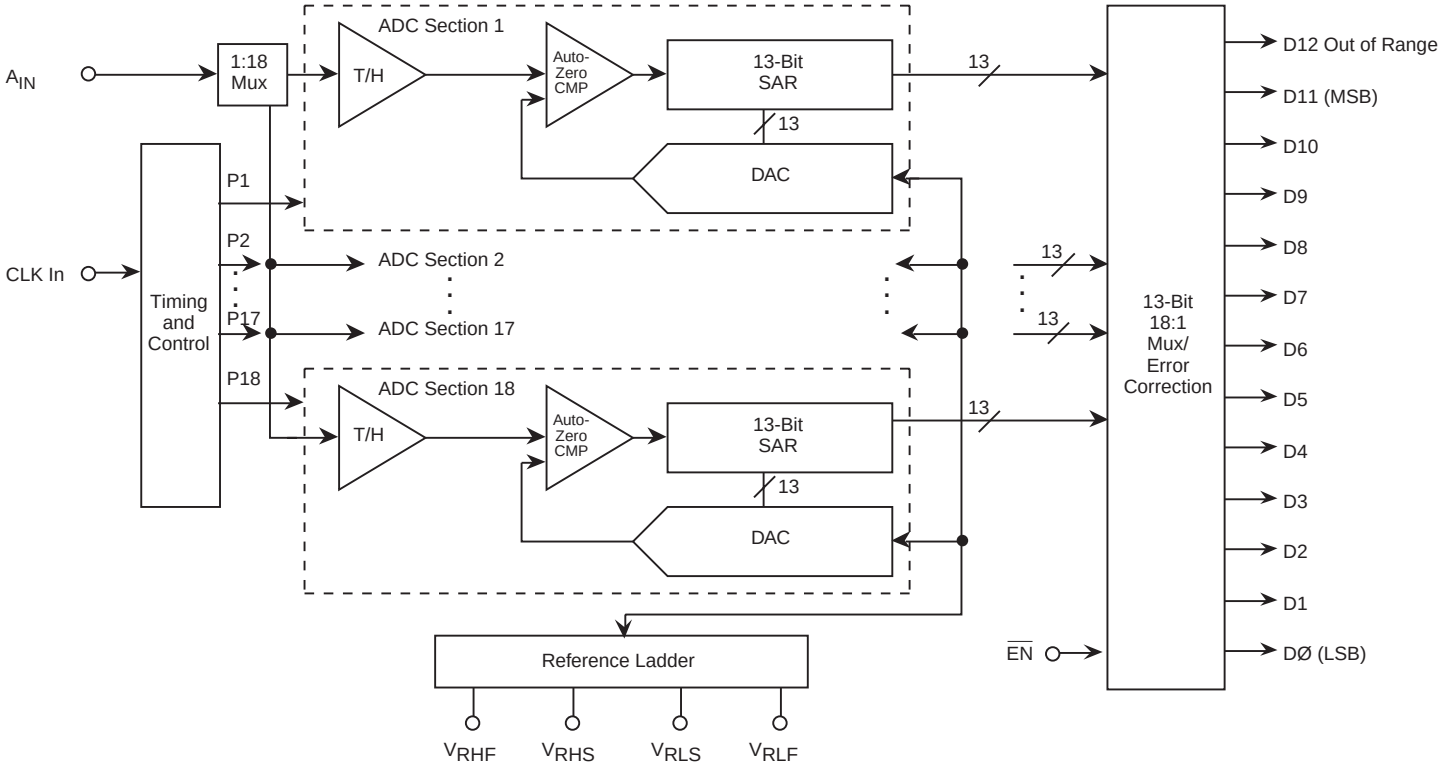
GENERAL DESCRIPTION

The SPT7938 is a 12-bit monolithic, low-cost, low-power analog-to-digital converter capable of minimum word rates of 40 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7938's low input capacitance of only 20 pF.

Power dissipation is extremely low at only 170 mW typical at 40 MSPS with a power supply of +5.0 V. The digital outputs are +3 V or +5 V, and are user selectable. The SPT7938 has incorporated proprietary circuit design and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7938 is available in a 28-lead SSOP package over the industrial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD} ..... +6 V

Input Voltages

Analog Input ..... –0.5 V to V_{DD} +0.5 V
CLK Input ..... V_{DD}
AGND – DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... –40 to +85 °C
Junction Temperature ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=+5.0 V, f_S=40 MSPS, V_{IN}=0 to 4 V, V_{RHS}=4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7938 MIN	SPT7938 TYP	SPT7938 MAX	UNITS
Resolution			12			Bits
DC Accuracy						
Integral Nonlinearity		V		±3		LSB
Differential Nonlinearity		V		±1		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range		VI	V_{RLS}		V_{RHS}	V
Input Resistance		V		25		kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	V_{IN} = 2 V_{PP}	V		250		MHz
–Full-Scale Error[1]		V		0.035		%FS
+Full-Scale Error[1]		V		–0.12		%FS
Conversion Characteristics						
Maximum Conversion Rate		VI	40			MHz
Minimum Conversion Rate		V	1			MHz
Pipeline Delay (Latency)		IV			14	Clock Cycles
Aperture Delay Time		V		1.0		ns
Aperture Jitter Time		V		5.0		ps(p-p)
Over-Voltage Recovery Time[2]					25	ns
Reference Input						
Resistance		VI	420	465	520	Ω
Voltage Range						
V_{RHS}		IV	3.0		V_{DD}	V
V_{RLS}		IV	0.0		2.0	V
V_{RHS} – V_{RLS}		V	2.0	4.0	5.0	V
Dynamic Performance						
Effective Number of Bits						
f_{IN}=3.58 MHz	T_A = +25 °C	I	9.9	10.1		Bits
f_{IN}=3.58 MHz	T_A = T_{MIN} to T_{MAX}	IV	9.4	10.1		Bits
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=3.58 MHz	T_A = +25 °C	I	61.2	62.5		dB
f_{IN}=3.58 MHz	T_A = T_{MIN} to T_{MAX}	IV	58.0	62.5		dB

[1] The full-scale range spans the reference ladder sense pins, V_{RHS} and V_{RLS}. Refer to the Voltage Reference section for discussion.
[2] Due to internal architecture, over-voltage recovery time is less than one clock cycle (i.e., 25 ns at f_{CLK} = 40 MHz).

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=+5.0 V, f_S=40 MSPS, V_{IN}=0 to 4 V, V_{RHS}=4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7938 MIN	SPT7938 TYP	SPT7938 MAX	UNITS
Dynamic Performance						
Harmonic Distortion						
f_{IN}=3.58 MHz	T_A = +25 °C	I	–62.5	–71		dB
f_{IN}=3.58 MHz	T_A = T_{MIN} to T_{MAX}	IV	–62.0	–71		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=3.58 MHz	T_A = +25 °C	I	60.2	62		dB
f_{IN}=3.58 MHz	T_A = T_{MIN} to T_{MAX}	IV	57.5	62		dB
Spurious Free Dynamic Range						
f_{IN}=3.58 MHz		V		73		dB
Differential Phase		V		0.25		Degree
Differential Gain		V		0.5		%
Clock Input						
Logic 1 Voltage		VI	2.0			V
Logic 0 Voltage		VI			0.8	V
Maximum Input Current Low		VI	–10		+10	µA
Maximum Input Current High		VI	–10		+10	µA
Input Capacitance		V		5		pF
Input Duty Cycle		V	45	50	55	%
Output Enable						
Logic 1 Voltage		VI	3.5			V
Logic 0 Voltage		VI			1.5	V
Maximum Input Current Low		VI	–10		+10	µA
Maximum Input Current High		VI	–10		+10	µA
Digital Outputs						
Logic 1 Voltage	I_{OH} = 0.5 mA		V_{DD}–0.5			V
Logic 0 Voltage	I_{OL} = 1.6 mA				0.42	V
CLK to Output Delay Time (t_D)		IV		15		ns
Output Enable to Data Output Delay	20 pF load	IV		10		ns
Power Supply Requirements						
Voltages OV_{DD}		IV	3.0		5.0	V
V_{DD}		IV	4.75	5.0	5.25	V
Currents I_{DD}		VI		34	40	mA
Power Dissipation		VI		170	200	mW
Power Supply Rejection Ratio				60		dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A – Timing Diagram 1

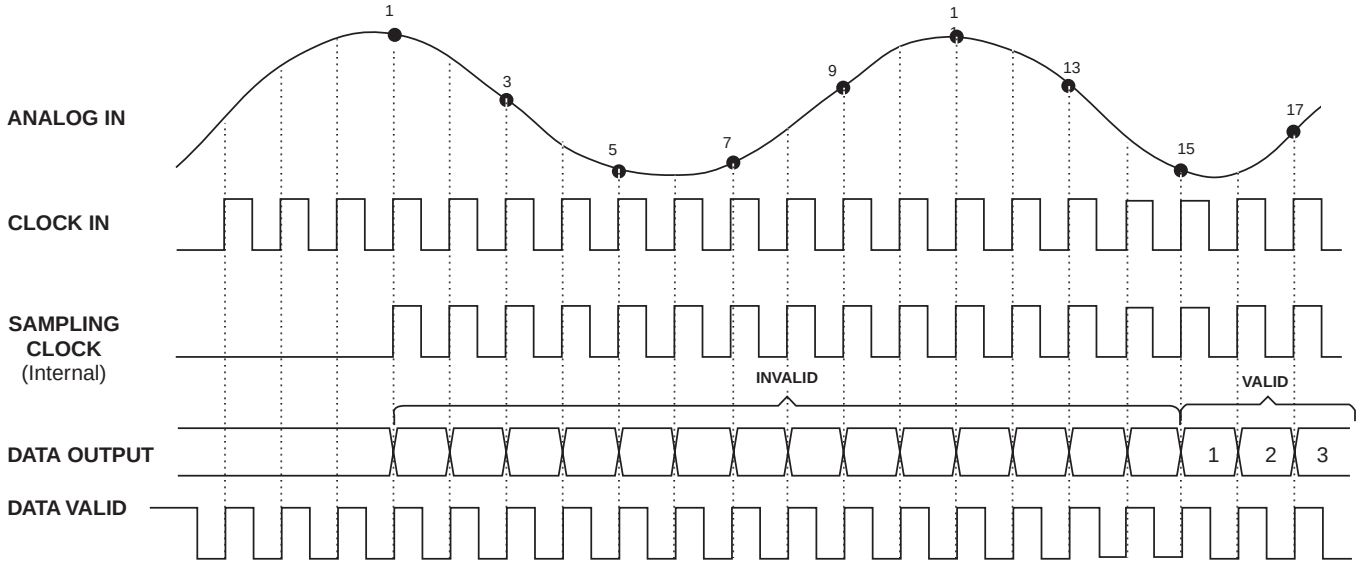


Figure 1B – Timing Diagram 2

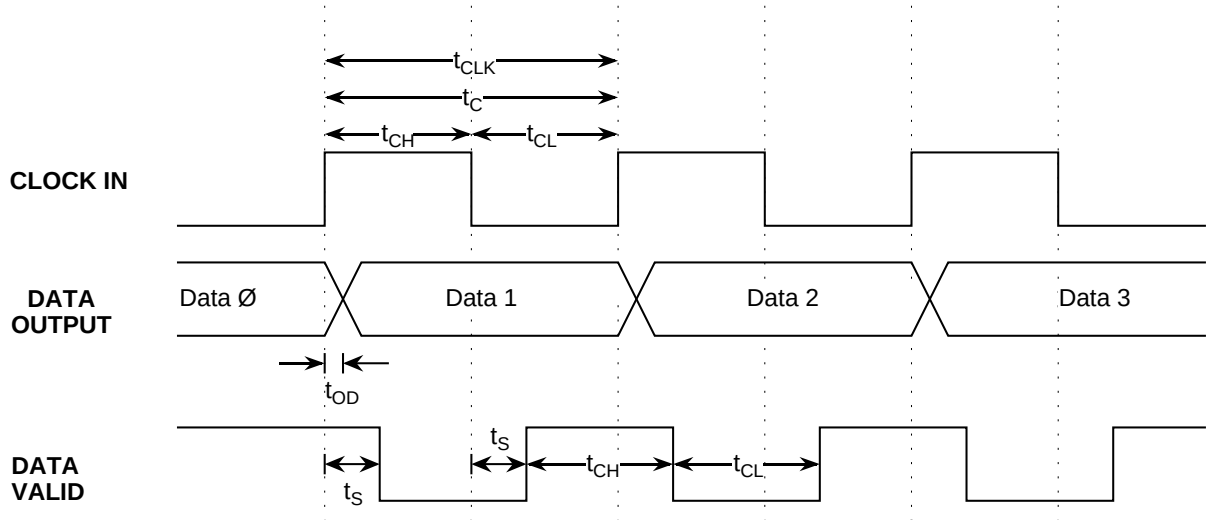
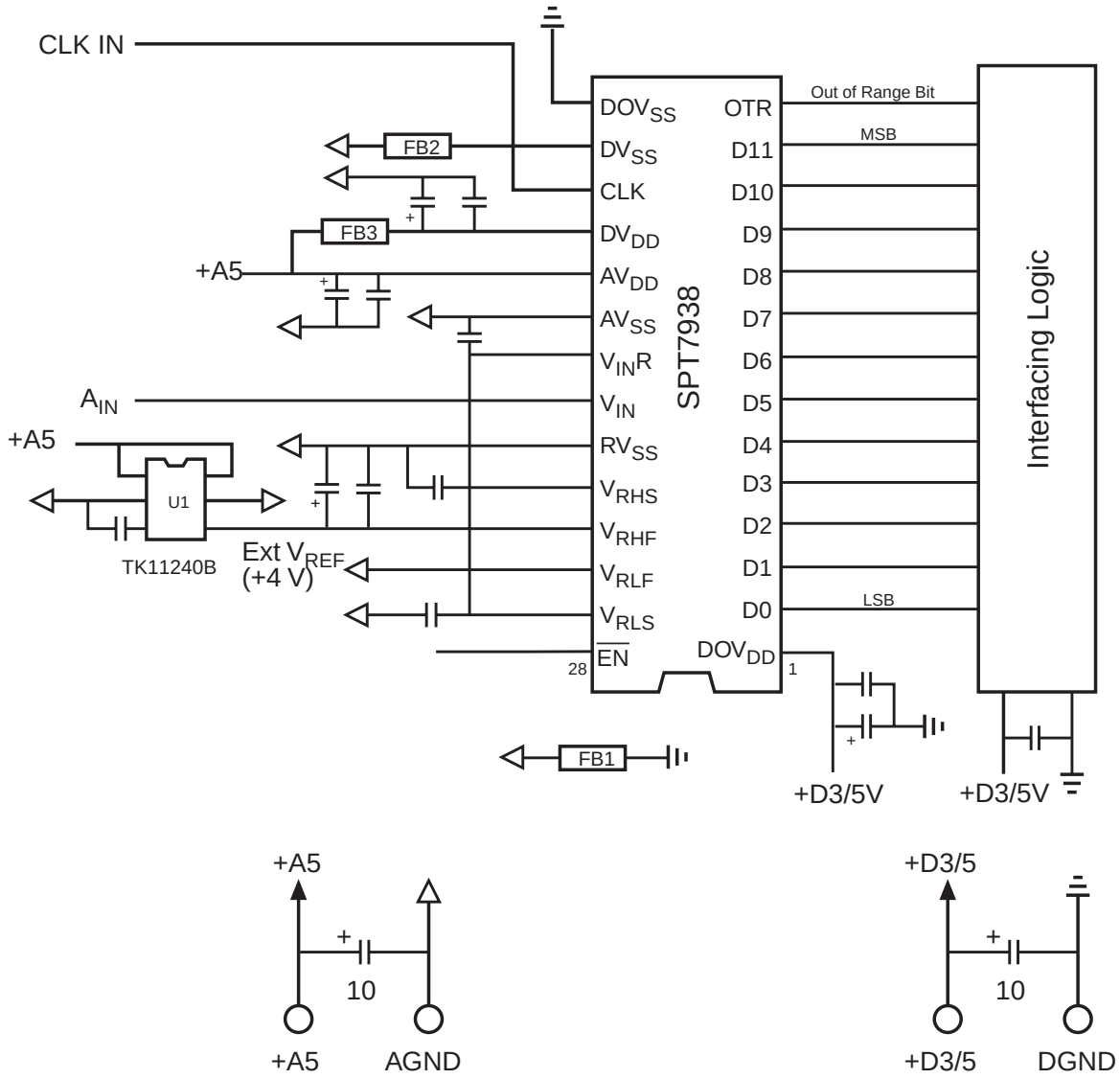


Figure 2 – Typical Interface Circuit



Notes:
1) Unless otherwise specified, all non-polarized capacitors are 0.01 microfarad surface-mount chip capacitors. They need to be placed as close to the pin as possible.
2) All polarized capacitors are 4.7 to 10 microfarad tantalum surface-mount capacitors.
3) FB1, FB2 and FB3 are ferrite beads. Place FB1 as close to the SPT7938 as possible.
4) U1 is a TOKO regulator, TK112XXB. XX is the regulated output voltage ranging from 1.3 V to 4.8 V with 100 mV increment. For example, TK11240B is a 4.0 V regulator.

TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 2 shows the typical interface requirements when using the SPT7938 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

CADEKA suggests that both the digital (DV_{DD}) and the analog (AV_{DD}) supply voltages on the SPT7938 be derived from a single analog supply as shown in figure 2. A separate digital supply should be used for the digital output driver supply (OV_{DD}) and all interface circuitry. CADEKA suggests using this power supply configuration to prevent a possible latch-up condition on power up. In addition, the power supplies must be powered up before the analog input is applied.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains 18 identical successive approximation ADC sections (all operating in parallel), an 18-phase clock generator, a 13-bit 18:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 18 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Table II – Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-17	13-bit SAR conversion
18	Data transfer

The 18-phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 18 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 14 clock cycles.

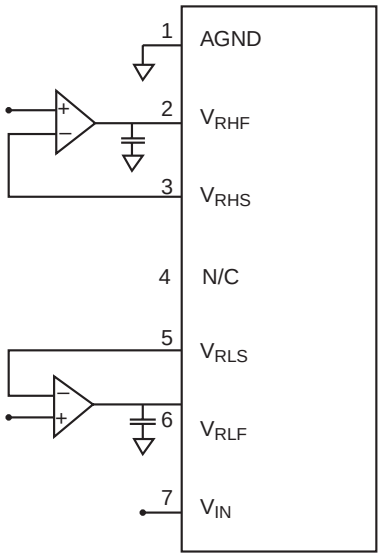
- Since only 18 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparator's response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7938 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage full-scale range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}. For optimum performance the full-scale voltage range (V_{RHS}–V_{RLS}) should be between 3 V to 5 V.

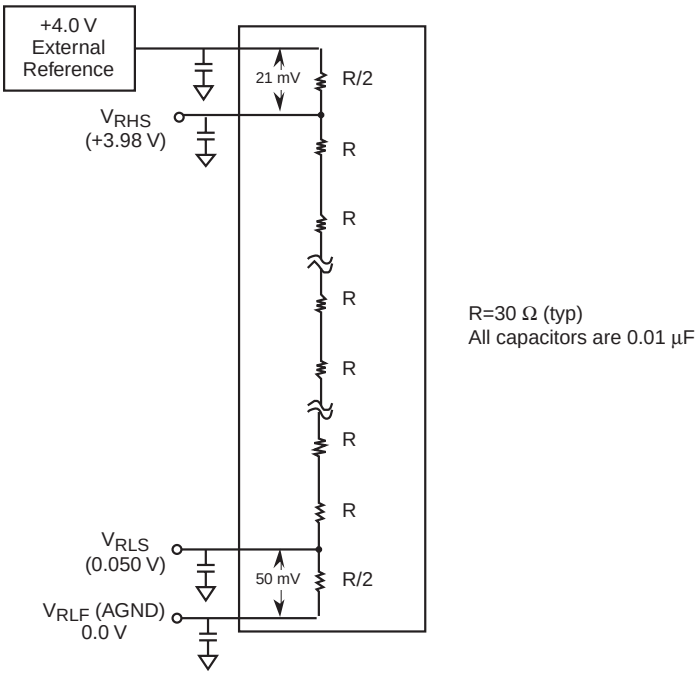
Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 3, offset and gain errors of less than ±3 LSB can be obtained.

Figure 3 – Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 4 – Simplified Reference Ladder Drive Circuit Without Force/Sense Circuit



In cases in which wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 4. Decouple force and sense lines to AGND with a 0.01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 4 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} – V_{RHS}$ = 0.5% of ($V_{RHF} – V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} – V_{RLF}$ = 1.25% of ($V_{RHF} – V_{RLF}$) (typical).

Figure 4 shows an example of expected voltage drops for a specific case. V_{REF} of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 21 mV drop is seen at V_{RHS} (= 3.98 V) and a 50 mV increase is seen at V_{RLS} (= 0.050 V).

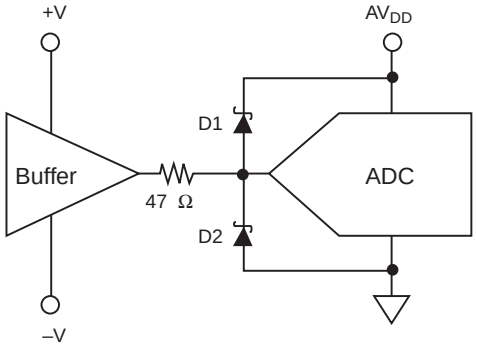
ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See the Voltage Reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7938's extremely low input capacitance of only 20 pF and very high input resistance in excess of 25 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 5. To prevent possible latch-up condition, the power supplies must be powered up before the input is applied.

Figure 5 – Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

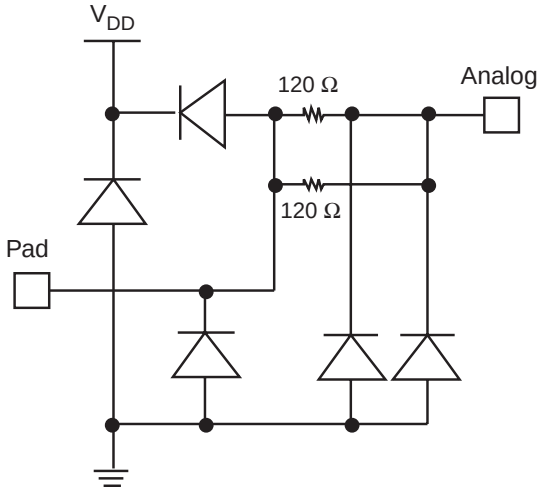
CALIBRATION

The SPT7938 uses a user-transparent, auto-calibration scheme to ensure 12-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 12-bit accuracy during device operation.

Upon powerup, the SPT7938 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 12-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec (for a 40 MHz clock). Once calibrated, the SPT7938 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7938 to remain in calibration.

Figure 6 – On-Chip Protection Circuit



INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 6. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

CLOCK INPUT

The SPT7938 is driven from a single-ended TTL-input clock. The duty cycle of the clock should be kept as close to 50% (±5%) as possible.

DIGITAL OUTPUTS

The digital outputs (D0–D12) are driven by a separate supply (OV_{DD}) ranging from +3 V to +5 V. This feature makes it possible to drive the SPT7938's TTL/CMOS-compatible outputs with the user's logic system supply. The format of the output data (D0–D11) is straight binary. (See table III.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table III – Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11–D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. –1/2 LSB	0	11 1111 111Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	00 0000 000Ø
0.0 V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The Overrange Output (D12) is an indication that the analog input signal has exceeded the positive full-scale input voltage by 1 LSB. When this condition occurs, D12 will switch to logic 1. All other data outputs (D0 to D11) will remain at logic 1 as long as D12 remains at logic 1. This feature makes it possible to include the SPT7938 in higher resolution systems.

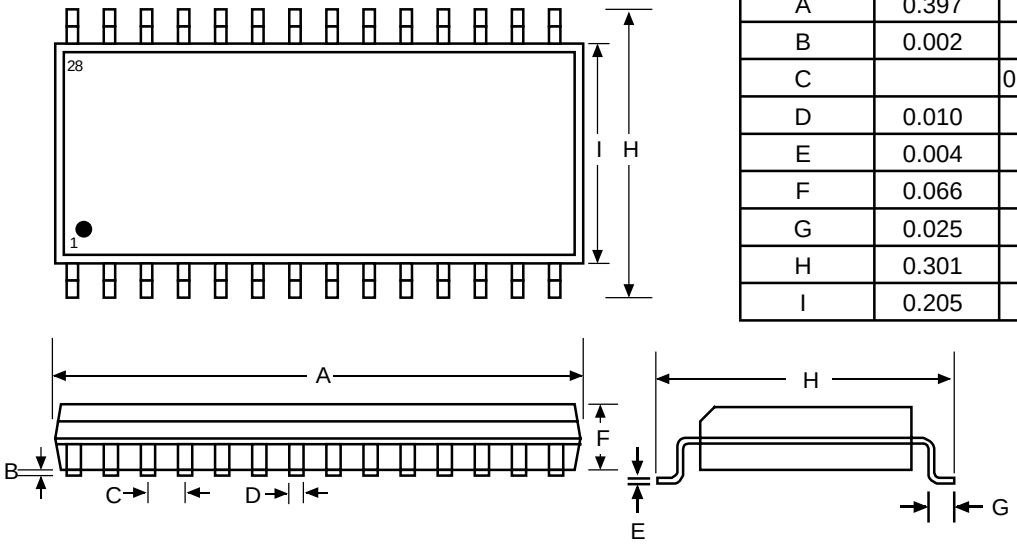
EVALUATION BOARD

The EB7938 evaluation board is available to aid designers in demonstrating the full performance of the SPT7938. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7938) describing the operation of this board, as well as information on the testing of the SPT7938, is also available. Contact the factory for price and availability.

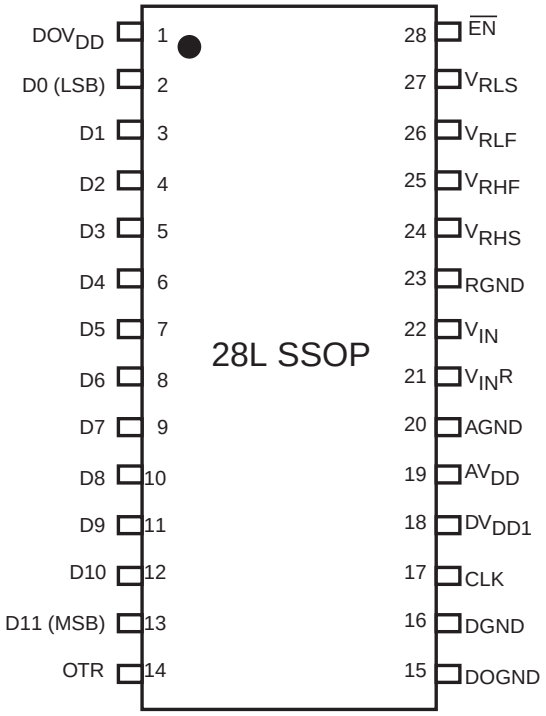
PACKAGE OUTLINE

28-Lead SSOP

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.397	0.407	10.07	10.33
B	0.002	0.008	0.05	0.21
C		0.0256 typ		0.65 typ
D	0.010	0.015	0.25	0.38
E	0.004	0.008	0.09	0.20
F	0.066	0.070	1.68	1.78
G	0.025	0.037	0.63	0.95
H	0.301	0.311	7.65	7.90
I	0.205	0.212	5.20	5.38



PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
DOV_{DD}	Digital Output Driver Supply
D0–D11	Data Output, Bits 0 – Bit 11
OTR	Out of Range
DOGND	Digital Output Driver Ground
DGND	Digital Ground
CLK	Input Clock
DV_{DD1}	Digital V_{DD}
AV_{DD}	Analog V_{DD}
AGND	Analog Ground
$V_{IN}R$	Analog Input Return
V_{IN}	Analog Input, Full Scale from V_{RLS} to V_{RHS}
RGND	Analog Ground Shield (Junction Isolated)
V_{RHS}	Reference High Sense
V_{RHF}	Reference High Force ($V_{RHF} \leq AV_{DD}$)
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
$\overline{EN}$	Output Enable (Active Low)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7938SIR	–40 to +85 °C	28L SSOP