# 32-Channel High Voltage Sample and Hold Amplifier Array

## Features

- 32 independent high voltage amplifiers
- 300V operating voltage
- 295V output voltage
- 2.2V/µs typical output slew rate
- Adjustable output current source limit
- Adjustable output current sink limit
- Internal closed loop gain of 72V/V
- 12MΩ feedback impedance
- Layout ideal for die applications

## Applications

- MEMS (microelectromechanical systems) driver
- Piezoelectric transducer driver
- Optical crosspoint switches (using MEMS technology)

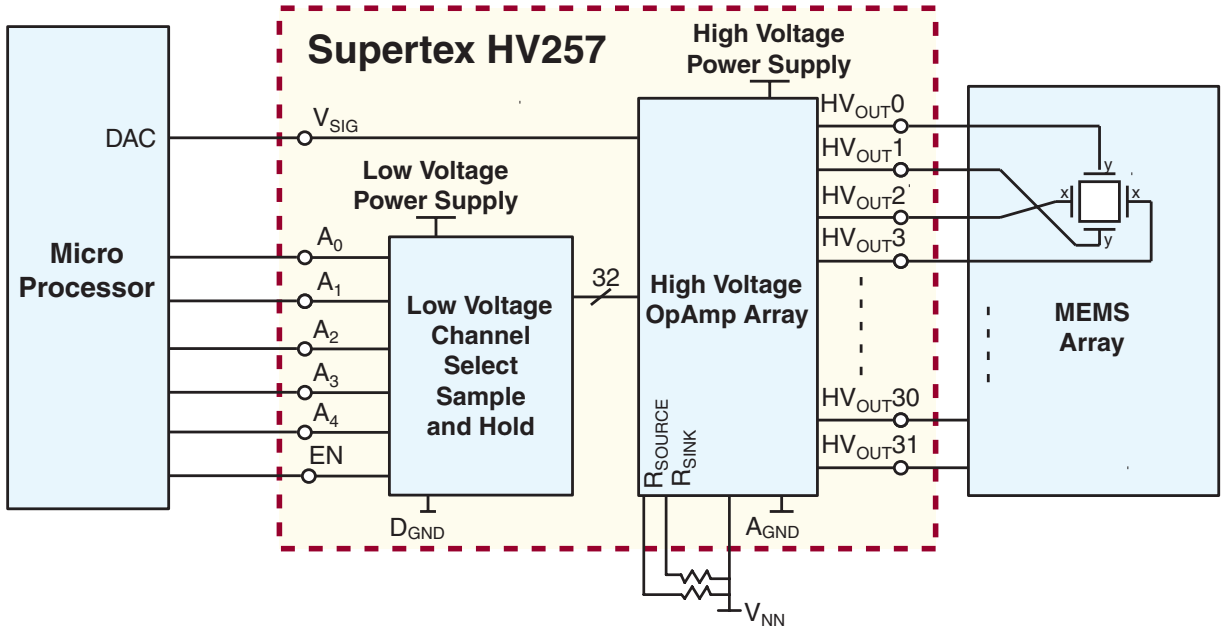
## General Description

The Supertex HV257 is a 32 channel high voltage sample and hold amplifier array integrated circuit. It operates on a single high voltage supply, up to 300V, and two low voltage supplies, $V_{DD}$ and $V_{NN}$.

All 32 sample and hold circuits share a common analog input, $V_{SIG}$. The individual sample and hold circuits are selected by a 5 to 32 logic decoder. The sampled voltage on the holding capacitor is buffered by a low voltage amplifier and amplified by a high voltage amplifier with a closed loop gain of 72V/V. The internal closed loop gain is set for an input voltage range of 0V to 4.096V. The input voltage can be up to 5.0V but the output will saturate. The maximum output voltage swing is 5V below the $V_{PP}$ high voltage supply. The outputs can drive capacitive loads of up to 3000pF.

The maximum output source and sink current can be adjusted by using two external resistors. An external $R_{SOURCE}$ resistor controls the maximum sourcing current, and an external $R_{SINK}$ resistor controls the maximum sinking current. The current limit is approximated 12.5V divided by the external resistor value. The setting is common for all 32 outputs. A low voltage silicon junction diode is made available to help monitor the die temperature.

## Typical Application Circuit



## Absolute Maximum Ratings

| | |
|---|---|
| $V_{PP}$, High voltage supply | 310V |
| $AV_{DD}$, Analog low voltage positive supply | 8.0V |
| $DV_{DD}$, Digital low voltage positive supply | 8.0V |
| $AV_{NN}$, Analog low voltage negative supply | -7.0V |
| $DV_{NN}$, Digital low voltage negative supply | -7.0V |
| Logic input voltage | -0.5V to $DV_{DD}$ |
| $V_{SIG}$, Analog input signal | 0V to 6.0V |
| $SRV_{PP}$, $V_{PP}$ ramp up/down | TBDV/usec |
| Storage temperature range | -65°C to 150°C |
| Maximum junction temperature | 150°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

| Device | Package Options |
|---|---|
| | 100 Lead MQFP |
| HV257 | HV257FG |
| | HV257FG-G |

*-G indicates package is RoHS compliant ('Green')*

## Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{PP}$ | High voltage positive supply | 125 | - | 300 | V | --- |
| $V_{DD}$ | Low voltage positive supply | 6.0 | - | 7.5 | V | --- |
| $V_{NN}$ | Low voltage negative supply | -4.5 | - | -6.5 | V | --- |
| $I_{PP}$ | $V_{PP}$ supply current | - | - | 0.8 | mA | $V_{PP}$ = 300V, All $HV_{OUT}$ = 0V No load |
| $I_{DD}$ | $V_{DD}$ supply current | - | - | 5.0 | mA | $V_{DD}$ = 6.0V to 7.5V |
| $I_{NN}$ | $V_{NN}$ supply current | -6.0 | - | - | mA | $V_{NN}$ = -4.5V to -6.5V |
| $T_J$ | Operating temperature range | -10 | - | 85 | °C | --- |

## Electrical Characteristics *(over operating conditions, unless otherwise specified)*

**High Voltage Amplifier**

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $HV_{OUT}$ | $HV_{OUT}$ voltage swing | 0 | - | $V_{PP}$-5 | V | --- |
| $V_{INOS}$ | Input offset | - | - | ±50 | mV | Input referred |
| SR | $HV_{OUT}$ slew rate rise | - | 2.2 | - | V/µs | No Load |
| | $HV_{OUT}$ slew rate fall | - | 2.0 | - | V/µs | No Load |
| BW | $HV_{OUT}$ -3dB channel bandwidth | - | 4.0 | - | KHz | $V_{PP}$ = 300V |
| $A_O$ | Open loop gain | 70 | 100 | - | dB | --- |
| $A_V$ | Closed loop gain | 68.4 | 72 | 75.6 | V/V | --- |
| $R_{FB}$ | Feedback resistance from $HV_{OUT}$ to ground | 9.6 | 12 | - | MΩ | --- |
| $C_{LOAD}$ | $HV_{OUT}$t capacitive load | 0 | - | 3000 | pF | --- |
| $I_{SOURCE}$ | $HV_{OUT}$ sourcing current limiting range | 50 | - | 500 | µA | $I_{SOURCE}$ = 12.5V/$R_{SOURCE}$ |
| $I_{SINK}$ | $HV_{OUT}$ sinking current limiting range | 50 | - | 500 | µA | $I_{SINK}$ = 12.5V/$R_{SINK}$ |
| $R_{SOURCE}$ | External resistance range for setting maximum current source | 25 | - | 250 | KΩ | --- |
| $R_{SINK}$ | External resistance range for setting maximum current sink | 25 | - | 250 | KΩ | --- |
| $CT_{DC}$ | DC channel to channel crosstalk | -80 | - | - | dB | --- |
| PSRR | Power supply rejection ratio for $V_{PP}$, $V_{DD}$, $V_{NN}$ | -40 | - | - | dB | --- |

# Electrical Characteristics *(over operating conditions, unless otherwise specified)*

### Sample and Hold

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $t_{AQ}$ | Acquisition time | - | 4.0 | - | µs | --- |
| $V_{PED}$ | Pedestal voltage | - | 1.0 | - | mV | input referred |
| $R_{SW}$ | Sample and Hold Switch resistance | - | 5.0 | - | kΩ | --- |
| $C_H$ | Sample and Hold capacitor | - | 10 | 12 | pF | --- |
| $V_{DROOP}$ | Voltage droop rate during hold time relative to input | - | 6.0 | - | V/s | output referred |
| $V_{SIG}$ | Input signal voltage range | 0 | - | 5.0 | V | --- |
| $C_{SIG}$ | $V_{SIG}$ input capacitance | - | 33 | - | pF | --- |

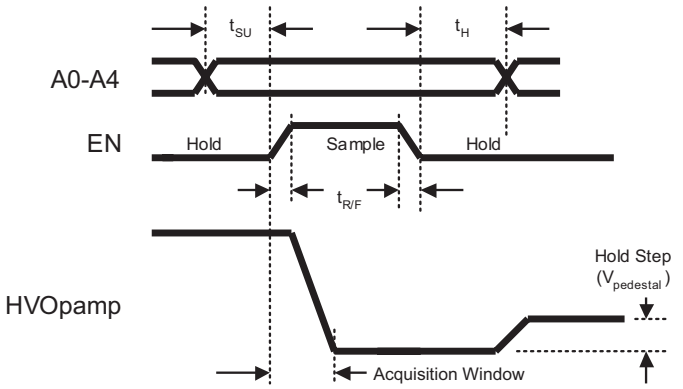
### Logic Decoder

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $t_{SU}$ | Set-up time-address to enable | 75 | - | - | ns | --- |
| $t_H$ | Hold time-address to enable bar | 75 | - | - | ns | --- |
| $V_{IH}$ | Input logic high voltage | 2.4 | - | $V_{DD}$ | V | --- |
| $V_{IL}$ | Input logic low voltage | 0 | - | 1.2 | V | --- |
| $I_{IH}$ | Input logic high current | - | - | 1.0 | µA | $V_{IL} = V_{DD}$ |
| $I_{IL}$ | Input logic low current | -1.0 | - | - | µA | $V_{IL} = 0V$ |
| $C_{IN}$ | Logic input capacitance | - | - | 15 | pF | --- |

## Decoder Truth Table

| $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | EN | Selected S/H |
|---|---|---|---|---|---|---|
| L | L | L | L | L | H | 0 |
| L | L | L | L | H | H | 1 |
| L | L | L | H | L | H | 2 |
| L | L | L | H | H | H | 3 |
| | | | | | | |
| H | H | H | H | L | H | 30 |
| H | H | H | H | H | H | 31 |
| X | X | X | X | X | L | All Open |

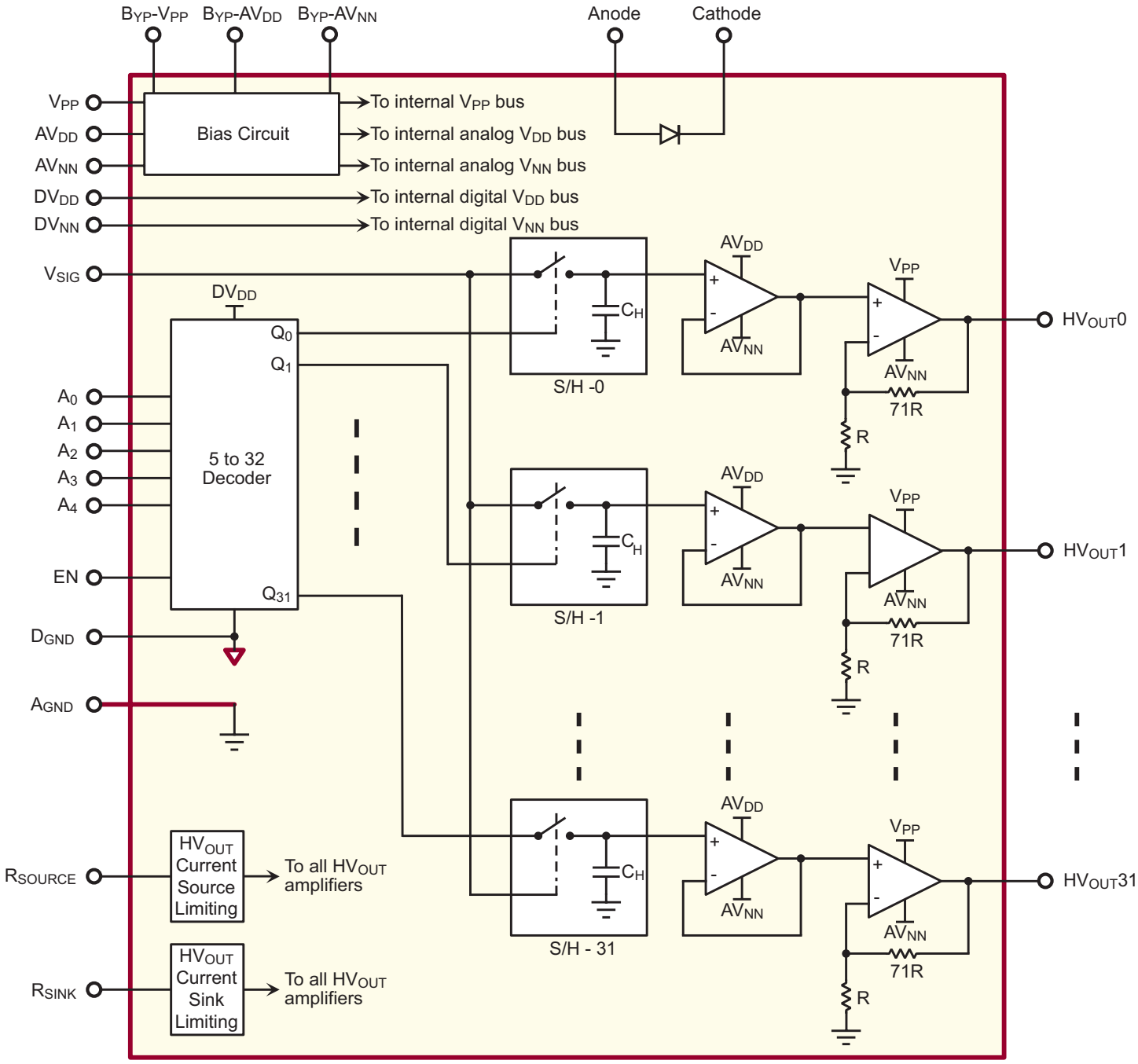
## Sample and Hold Timing




## Temperature Diode

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| PIV | Peak inverse voltage | - | - | 5.0 | V | cathode to anode |
| $V_F$ | Forward diode drop | - | 0.6 | - | V | $I_F$ = 100µA, anode to cathode at $T_A$ = 25°C |
| $I_F$ | Forward diode current | - | - | 100 | µA | anode to cathode |
| $T_C$ | $V_F$ temperature coefficient | - | -2.2 | - | mV/°C | anode to cathode |

## Block Diagram



# Power Up/Down Issues

### External Diode Protection

The device can be damaged due to improper power up / down sequence. To prevent damage, please follow the acceptable power up / down sequences, and add two external diodes as shown in the diagram on the right. The first diode is a high voltage diode across $V_{PP}$ and $V_{DD}$ , where the anode of the diode is connected to $V_{DD}$ and the cathode of the diode is connected to $V_{PP}$. Any low current, high voltage diode, such as a 1N4004, will be adequate. The second diode is a Schottky diode across $V_{NN}$ and $D_{GND}$ , where the anode of the Schottky diode is connected to $V_{NN}$ , and the cathode is connected to $D_{GND}$. Any low current Schottky diode such as a 1N5817 will be adequate.

### Acceptable Power Up Sequences

The HV257 can be powered up with any of the following sequences listed below.

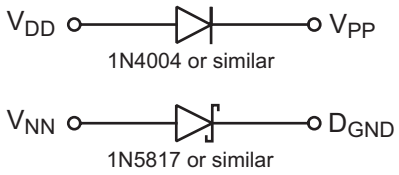
1) $V_{PP}$ 2) $V_{NN}$ 3) $V_{DD}$ 4) Inputs and Anode
1) $V_{NN}$ 2) $V_{DD}$ 3) $V_{PP}$ 4) Inputs and Anode
1) $V_{DD}$ & $V_{NN}$ 2) Inputs 3) $V_{PP}$ 4) Anode

### Acceptable Power Down Sequences

The HV257 can be powered down with any of the following sequences listed below.

1) Inputs and Anode 2) $V_{DD}$ 3) $V_{NN}$ 4) $V_{PP}$
1) Inputs and Anode 2) $V_{PP}$ 3) $V_{DD}$ 4) $V_{NN}$
1) Anode 2) $V_{PP}$ 3) Inputs 4) $V_{NN}$ & $V_{DD}$

### External Diode Protection Connection



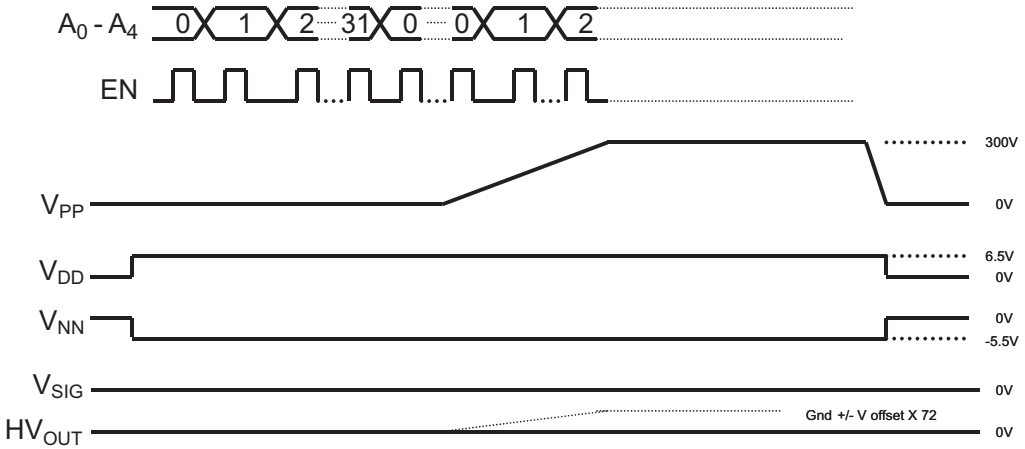

### Suggested Power Up/Down Sequence

The HV257 needs all power supplies to be fully up and all channels refreshed with $V_{SIG}$ = 0V to force all high voltage outputs to 0V. Before that time, the high voltage outputs may have temporary voltage excursions above or below Gnd level depending on selected power up sequence. To minimize the excursions:

1. The $V_{DD}$ and $V_{NN}$ power supplies should be applied at the same time (or within a few nanoseconds).

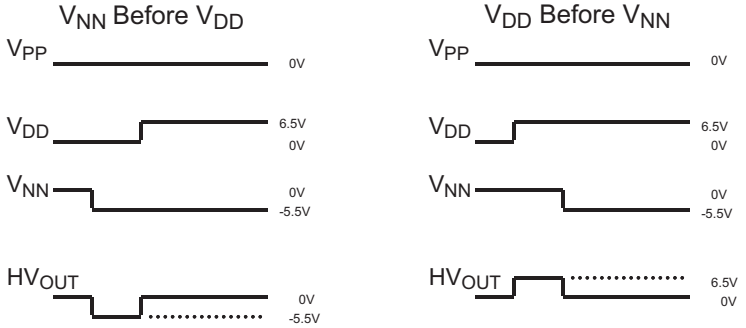
2. All channels should be continuously refreshed with $V_{SIG}$ = 0V, just before, and while the $V_{PP}$ is ramping up. Suggested $V_{PP}$ ramp up speed should be 10msec or longer and ramp down to be 1msec or longer.

# Recommended Power Up/Down Timing



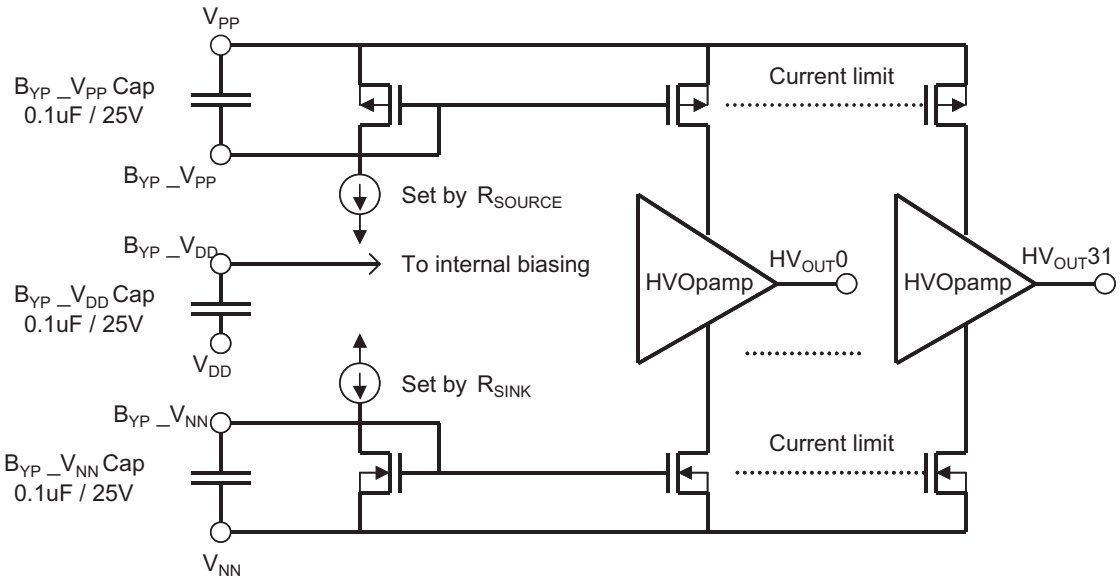

# $HV_{OUT}$ Level at Power UP

## Power Up Sequence



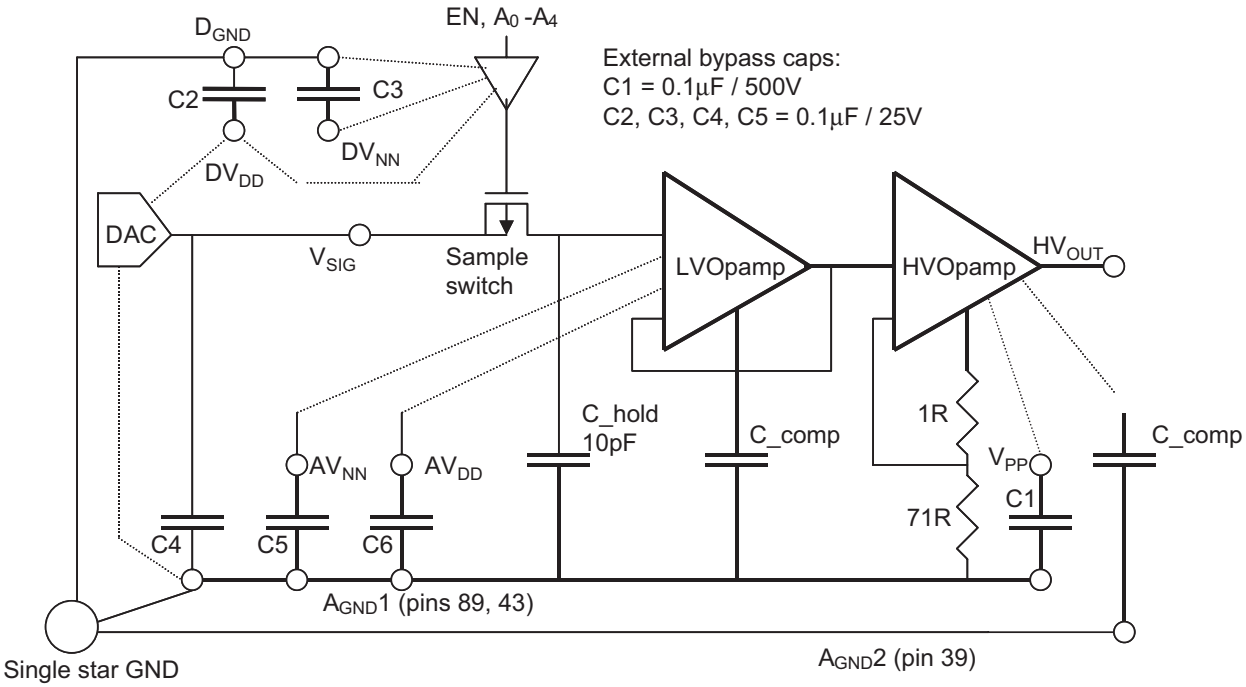
## $R_{SINK}$ / $R_{SOURCE}$

The $V_{DD\_BYP}$ ,$V_{DD\_BYP}$ ,and $V_{NN\_BYP}$ pins are internal. high impedance current. mirror gate nodes, brought out to mantain stable opamp biasing currents in noisy power supply environments. 0.1uF/25V bypass capacitors, added from $V_{PP\_BYP}$ pin to $V_{PP}$ , from $V_{DD\_BYP}$ pin to $V_{DD}$ , and from $V_{NN\_BYP}$ to $V_{NN}$,will force the high impedance gate nodes to follow fluctuation of power lines. The expected voltages at the $V_{DD\_BYP}$, and $V_{NN\_BYP}$ pins are typically 1.5 volts from their respectful power supply. The expected voltage at $V_{PP\_BYP}$ is typically 3V below $V_{PP}$.




## Ground Isolation ($A_{GND}$/$D_{GND}$ Isolation)

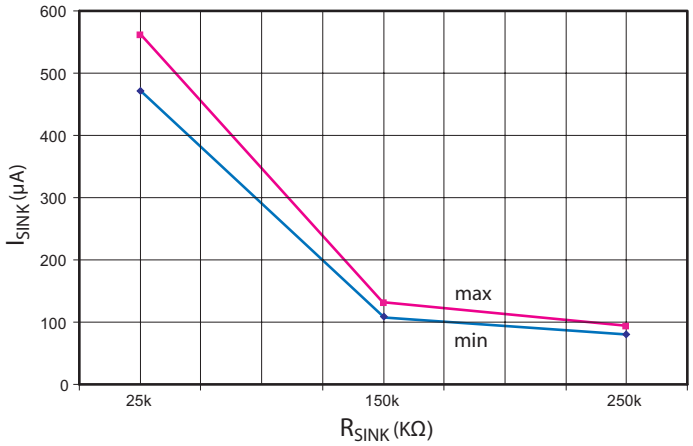
It is important that the $A_{GND}$ pin is connected to a clean ground. The hold capacitors are internally connected to the $A_{GND}$, and any ground noise will directly couple to the high voltage outputs (with a gain of 72). The analog and digital ground traces on the PCB should be physically separated to reduce digital switching noise degrading the signal to noise performance.



## Typical Characteristics

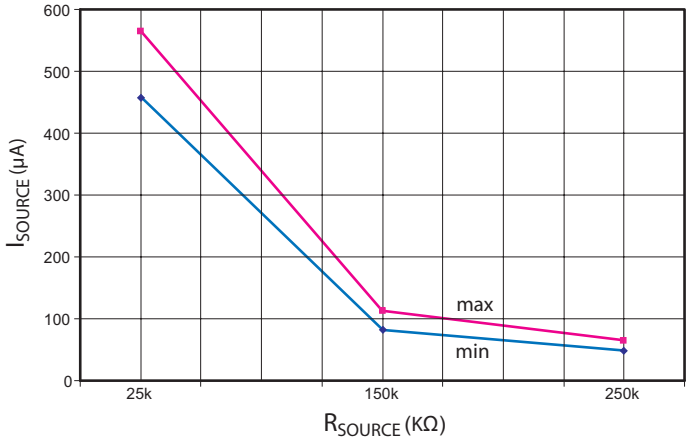
$I_{SINK}$ vs $R_{SINK}$

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)




$I_{SOURCE}$ vs $R_{SOURCE}$

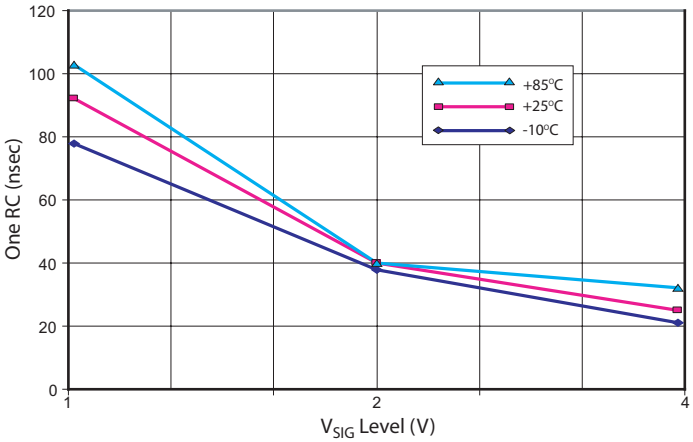
($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)




Acquisition Window

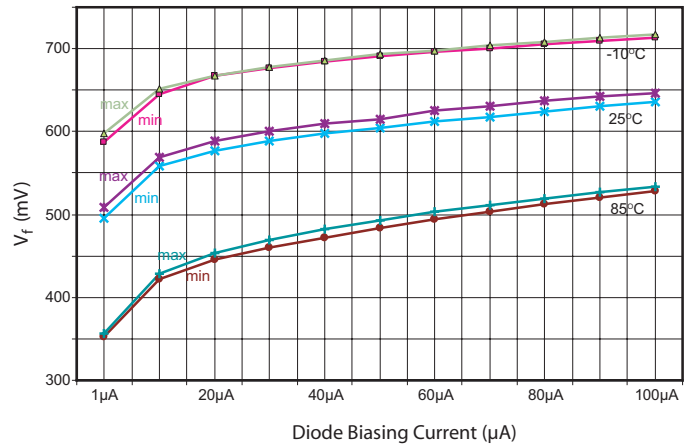
("one RC" response to one volt input step)

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)



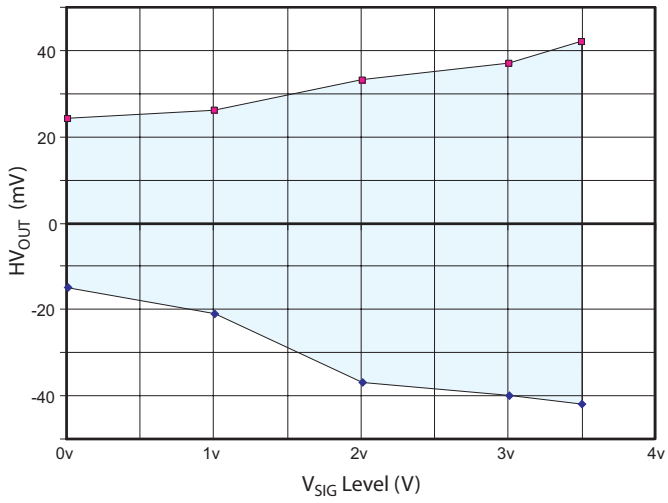

Temperature Diode vs Temperature

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V)



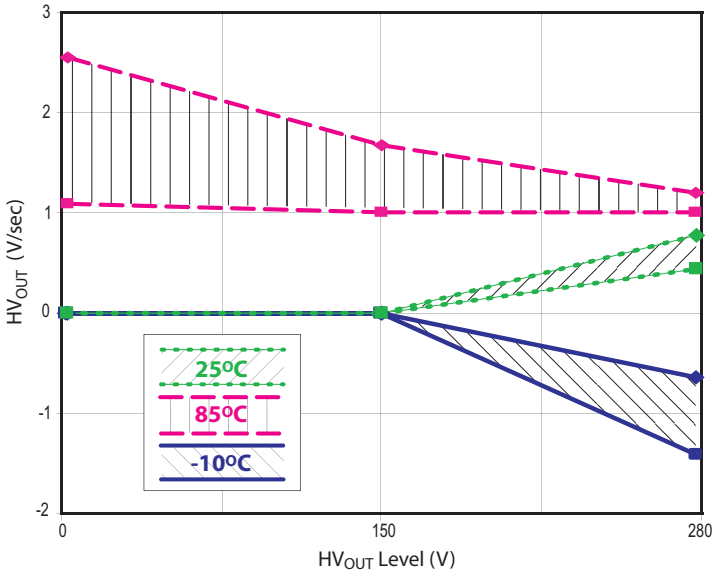

$HV_{OUT}$ Charge Injection vs $V_{SIG}$

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)




$HV_{OUT}$ Droop

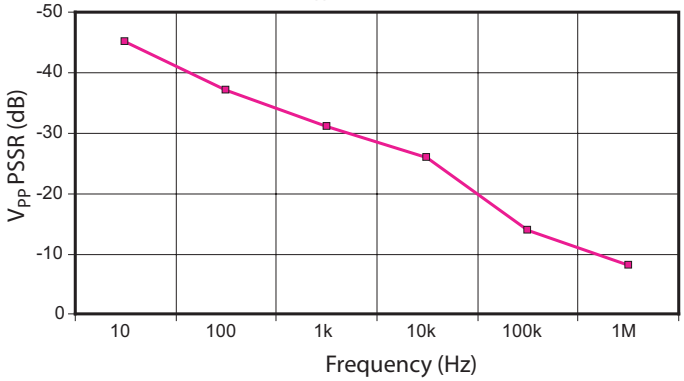
($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V)



## Typical Characteristics (cont.)

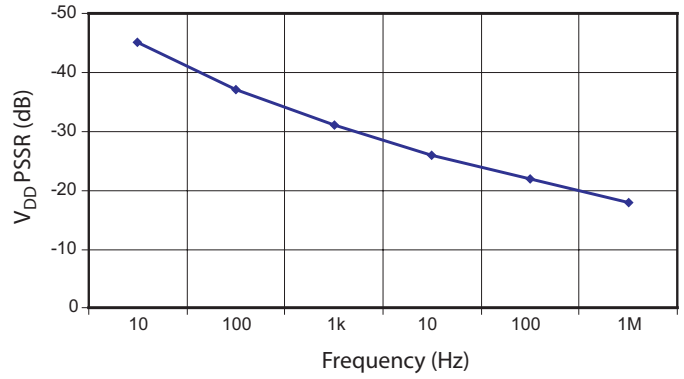
$V_{PP}$ PSSR vs Frequency

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)



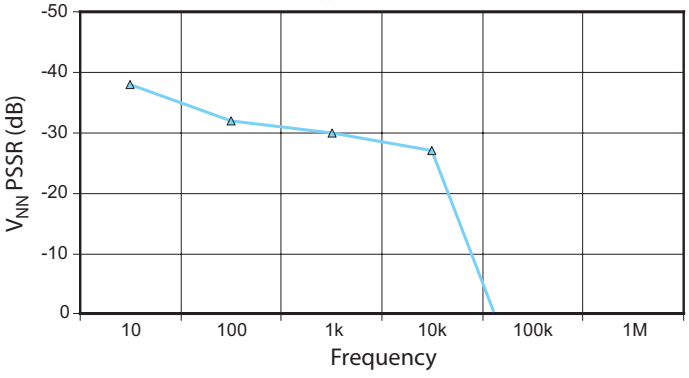

$V_{DD}$ PSSR vs Frequency

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)



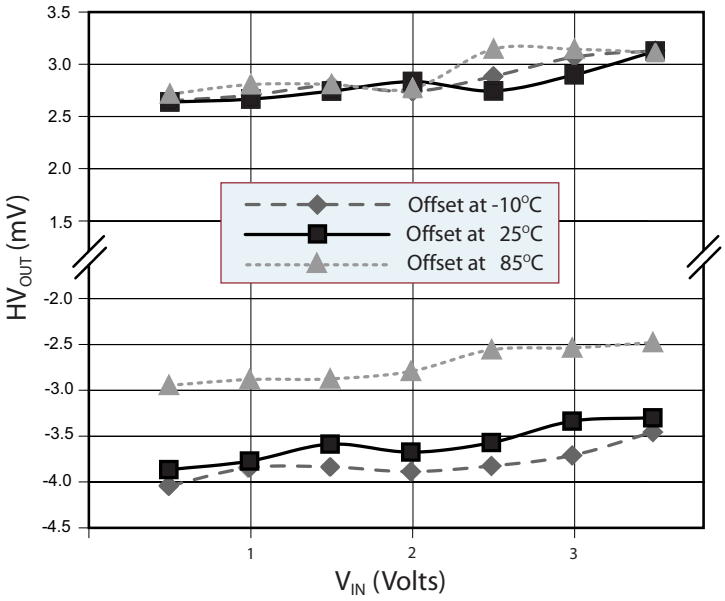

$V_{NN}$ PSSR vs Frequency

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = 25°C)



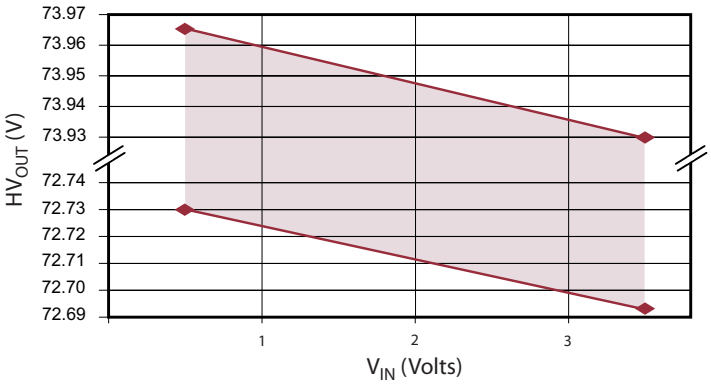

Input Offset vs $V_{IN}$ and Temperature

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V)




Gain vs $V_{IN}$

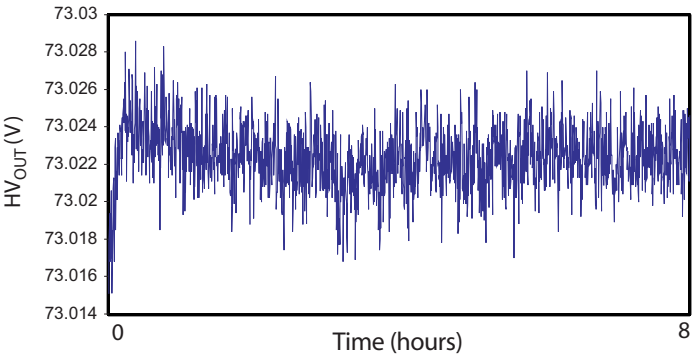
($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = 5.5V, $T_A$ = -10°, +25°, +85°C)



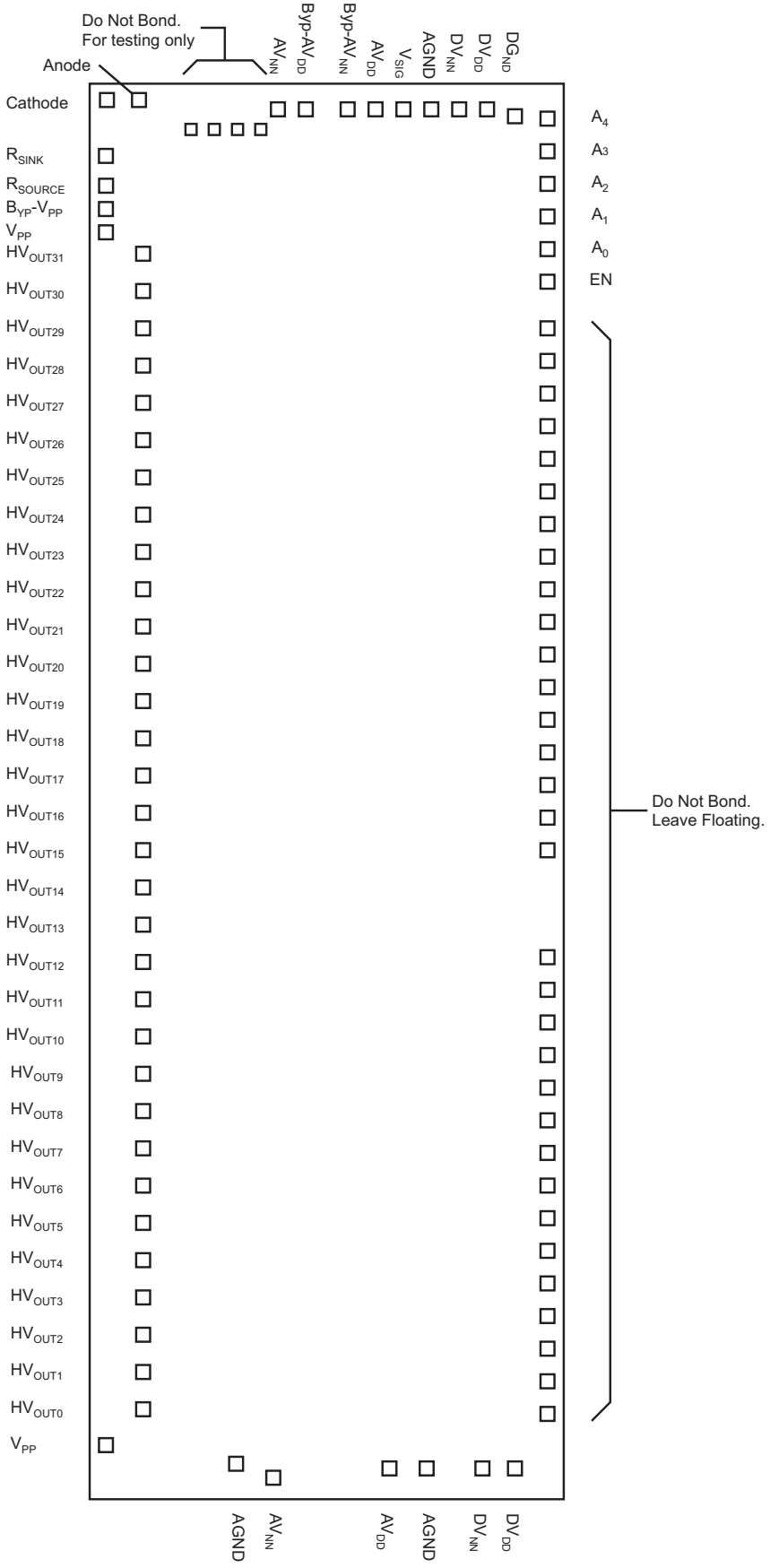

$HV_{OUT}$ Drift

HV257DFG-5037047 Q3 Dev # 3, Channel 16

($V_{PP}$ = 300V, $V_{DD}$ = 6.5V, $V_{NN}$ = -5V, $V_{SIG}$=1V, $T_A$ = 25°C)



## Pad Configuration *(not drawn to scale)*



# Pad Coordinates

*Chip size: 17160µm x 5830µm*
*Center of die is (0,0)*

| Pad Name | X (µm) | Y(µm) |
|---|---|---|
| $V_{PP}$ | -8338.5 | 2708.5 |
| $HV_{OUT}0$ | -7895.0 | 2305.5 |
| $HV_{OUT}1$ | -7448.5 | 2305.5 |
| $HV_{OUT}2$ | -7001.5 | 2305.5 |
| $HV_{OUT}3$ | -6554.5 | 2305.5 |
| $HV_{OUT}4$ | -6107.5 | 2305.5 |
| $HV_{OUT}5$ | -5660.5 | 2305.5 |
| $HV_{OUT}6$ | -5213.5 | 2305.5 |
| $HV_{OUT}7$ | -4766.5 | 2305.5 |
| $HV_{OUT}8$ | -4319.5 | 2305.5 |
| $HV_{OUT}9$ | -3872.5 | 2305.5 |
| $HV_{OUT}10$ | -3425.5 | 2305.5 |
| $HV_{OUT}11$ | -2978.5 | 2305.5 |
| $HV_{OUT}12$ | -2531.5 | 2305.5 |
| $HV_{OUT}13$ | -2084.5 | 2305.5 |
| $HV_{OUT}14$ | -1637.5 | 2305.5 |
| $HV_{OUT}15$ | -1190.5 | 2305.5 |
| $HV_{OUT}16$ | -743.5 | 2305.5 |
| $HV_{OUT}17$ | -296.5 | 2305.5 |
| $HV_{OUT}18$ | 150.0 | 2305.5 |
| $HV_{OUT}19$ | 597.5 | 2305.5 |
| $HV_{OUT}20$ | 1044.5 | 2305.5 |
| $HV_{OUT}21$ | 1491.5 | 2305.5 |
| $HV_{OUT}22$ | 1938.5 | 2305.5 |
| $HV_{OUT}23$ | 2385.5 | 2305.5 |
| $HV_{OUT}24$ | 2832.5 | 2305.5 |
| $HV_{OUT}25$ | 3279.5 | 2305.5 |
| $HV_{OUT}26$ | 3726.5 | 2305.5 |
| $HV_{OUT}27$ | 4173.5 | 2305.5 |
| $HV_{OUT}28$ | 4620.5 | 2305.5 |
| $HV_{OUT}29$ | 5067.5 | 2305.5 |

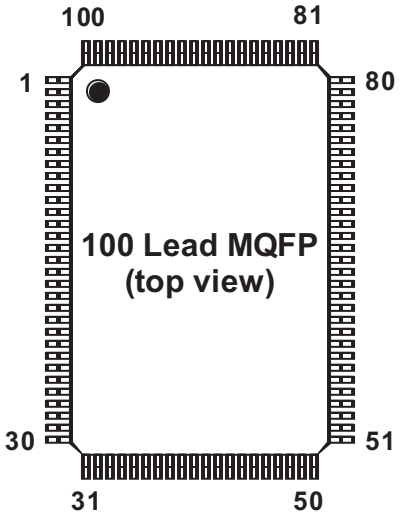
| Pad Name | X (µm) | Y (µm) |
|---|---|---|
| $HV_{OUT}30$ | 5514.5 | 2305.5 |
| $HV_{OUT}31$ | 5961.5 | 2305.5 |
| $V_{PP}$ | 6659 | 2709 |
| Byp_$V_{PP}$ | 7045 | 2709 |
| $R_{SOURCE}$ | 7489 | 2709 |
| $R_{SINK}$ | 7969 | 2709 |
| Cathode | 8366 | 2709 |
| Anode | 8366 | 2199 |
| $AV_{NN}$ | 8047 | 425.0 |
| Byp_$AV_{DD}$ | 8047 | 125.5 |
| Byp_$AV_{NN}$ | 8047 | -345.5 |
| $AV_{DD}$ | 8047 | -704.5 |
| VSIG | 8047 | -1072.5 |
| AGND | 8047 | -1424.5 |
| $DV_{NN}$ | 8066.5 | -1590.0 |
| $DV_{DD}$ | 8066.5 | -1958.5 |
| DGND | 7867.0 | -2192.0 |
| $A_4$ | 7723 | -2684.0 |
| $A_3$ | 7319.0 | -2684.0 |
| $A_2$ | 6913.0 | -2684.0 |
| $A_1$ | 6508.5 | -2684.0 |
| $A_0$ | 6103.0 | -2684.0 |
| EN | 5698.0 | -2684.0 |
| NC | 5043.5 | -2686.0 |
| NC | 4638.5 | -2686.0 |
| NC | 4233.5 | -2686.0 |
| NC | 3828.5 | -2686.0 |
| NC | 3423.5 | -2686.0 |
| NC | 3018.5 | -2686.0 |
| NC | 2613.5 | -2686.0 |
| NC | 2208.5 | -2686.0 |

| Pad Name | X (µm) | Y (µm) |
|---|---|---|
| NC | 1803.5 | -2686.0 |
| NC | 1398.5 | -2686.0 |
| NC | 993.5 | -2686.0 |
| NC | 588.5 | -2686.0 |
| NC | 183.5 | -2686.0 |
| NC | -221.5 | -2686.0 |
| NC | -626.5 | -2686.0 |
| NC | -1031.5 | -2686.0 |
| NC | -1436.5 | -2686.0 |
| NC | -2412.0 | -2686.0 |
| NC | -2817 | -2686.0 |
| NC | -3222 | -2686.0 |
| NC | -3627 | 2686.0 |
| NC | -4032 | 2686.0 |
| NC | -4437 | -2686.0 |
| NC | -4842 | -2686.0 |
| NC | -5247 | -2686.0 |
| NC | -5652 | -2686.0 |
| NC | -6052 | -2686.0 |
| NC | -6462 | -2686.0 |
| NC | -6867 | -2686.0 |
| NC | -7272 | -2686.0 |
| NC | -7677 | -2686.0 |
| NC | -8082 | -2686.0 |
| $DV_{DD}$ | -8373.0 | -2250.0 |
| $DV_{NN}$ | -8373.0 | -1949.0 |
| AGND | -8367.0 | -1561.0 |
| $AV_{DD}$ | -8387.0 | -1143.0 |
| $AV_{NN}$ | -8338.5 | 577.5 |
| AGND | -8341.0 | 916.5 |

## Pin Description

| Pin # | Function | Description |
|---|---|---|
| 33,100 | $V_{PP}$ | High voltage positive supply. There are two pads. |
| 99 | $B_{YP-}V_{PP}$ | For additional $V_{PP}$ decoupling capacitor. |
| 42,91 | $AV_{DD}$ | Analog low voltage positive supply. This should be at the same potential as $DV_{DD}$. There are two pads. |
| 93 | $B_{YP-}AV_{DD}$ | For additional $AV_{DD}$ decoupling capacitor. |
| 40,94 | $AV_{NN}$ | Analog low voltage negative supply. This should be at the same potential as $DV_{NN}$. There are two pads. |
| 92 | $B_{YP-}AV_{NN}$ | For additional $AV_{NN}$ decoupling capacitor. |
| 45, 87 | $DV_{DD}$ | Digital low voltage positive supply. This should be at the same potential as $AV_{DD}$. There are two pads. |
| 44, 88 | $DV_{NN}$ | Digital low voltage negative supply. This should be at the same potential as $AV_{NN}$. There are two pads. |
| 86 | $D_{GND}$ | Digital ground. |
| 39, 43, 89 | $A_{GND}$ | Analog Ground. There are three pads. They need to be externally connected together. |
| 81-85 | $A_0$ to $A_4$ | Decoder logic input. Addressed channel will close the sample and hold switch. Sample and hold switches for unaddressed channels are kept open. |
| 80 | EN | Active logic high input. Logic low will keep sample and hold switches open. |
| 90 | $V_{SIG}$ | Common input signal for all 32 sample and hold circuits. |
| 98 | $R_{SOURCE}$ | External resistor from $R_{SOURCE}$ to $V_{NN}$ sets output current sourcing limit. Current limit is approximately 12.5V divided by $R_{SOURCE}$ resistor value. |
| 97 | $R_{SINK}$ | External resistor from $R_{SINK}$ to $V_{NN}$ sets output current sinking limit. Current limit is approximately 12.5V divided by $R_{SINK}$ resistor value. |
| 95 | Anode | Anode side of a low voltage silicon diode that can be used to monitor die temperature. |
| 96 | Cathode | Cathode side of a low voltage silicon diode that can be used to monitor die temperature. |
| 1-32 | $HV_{OUT0}$ to $V_{OUT31}$ | Amplifier outputs. |
| 34-38, 41, 46-79 | NC | No Connect |

## Pin Layout




## Pin Configuration

| Pin | Function |
|---|---|
| 1 | $HV_{OUT}31$ |
| 2 | $HV_{OUT}30$ |
| 3 | $HV_{OUT}29$ |
| 4 | $HV_{OUT}28$ |
| 5 | $HV_{OUT}27$ |
| 6 | $HV_{OUT}26$ |
| 7 | $HV_{OUT}25$ |
| 8 | $HV_{OUT}24$ |
| 9 | $HV_{OUT}23$ |
| 10 | $HV_{OUT}22$ |
| 11 | $HV_{OUT}21$ |
| 12 | $HV_{OUT}20$ |
| 13 | $HV_{OUT}19$ |
| 14 | $HV_{OUT}18$ |
| 15 | $HV_{OUT}17$ |
| 16 | $HV_{OUT}16$ |
| 17 | $HV_{OUT}15$ |
| 18 | $HV_{OUT}14$ |
| 19 | $HV_{OUT}13$ |
| 20 | $HV_{OUT}12$ |
| 21 | $HV_{OUT}11$ |
| 22 | $HV_{OUT}10$ |
| 23 | $HV_{OUT}9$ |
| 24 | $HV_{OUT}8$ |
| 25 | $HV_{OUT}7$ |

| Pin | Function |
|---|---|
| 26 | $HV_{OUT}6$ |
| 27 | $HV_{OUT}5$ |
| 28 | $HV_{OUT}4$ |
| 29 | $HV_{OUT}3$ |
| 30 | $HV_{OUT}2$ |
| 31 | $HV_{OUT}1$ |
| 32 | $HV_{OUT}0$ |
| 33 | $V_{PP}$ |
| 34 | NC |
| 35 | NC |
| 36 | NC |
| 37 | NC |
| 38 | NC |
| 39 | $A_{GND}$ |
| 40 | $AV_{NN}$ |
| 41 | NC |
| 42 | $AV_{DD}$ |
| 43 | $A_{GND}$ |
| 44 | $DV_{NN}$ |
| 45 | $DV_{DD}$ |
| 46 | NC |
| 47 | NC |
| 48 | NC |
| 49 | NC |
| 50 | NC |

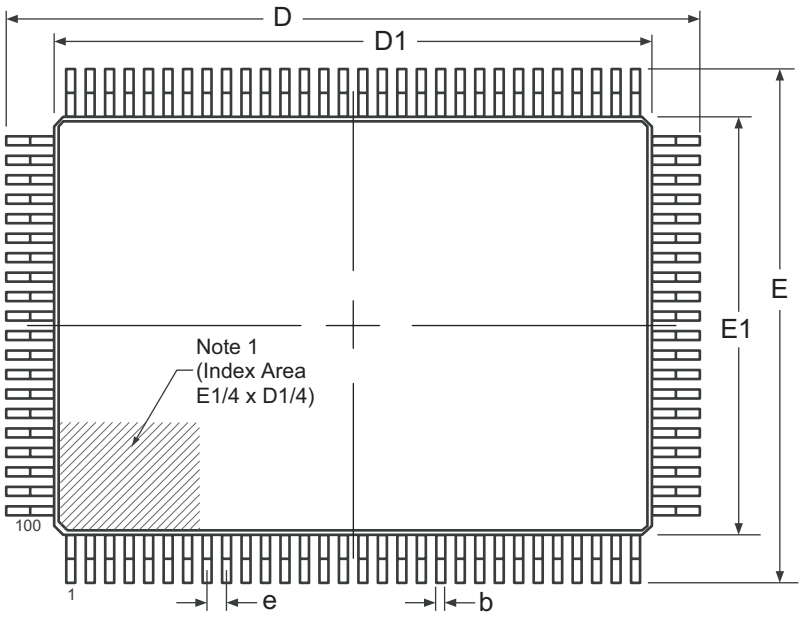
| Pin | Function |
|---|---|
| 51 | NC |
| 52 | NC |
| 53 | NC |
| 54 | NC |
| 55 | NC |
| 56 | NC |
| 57 | NC |
| 58 | NC |
| 59 | NC |
| 60 | NC |
| 61 | NC |
| 62 | NC |
| 63 | NC |
| 64 | NC |
| 65 | NC |
| 66 | NC |
| 67 | NC |
| 68 | NC |
| 69 | NC |
| 70 | NC |
| 71 | NC |
| 72 | NC |
| 73 | NC |
| 74 | NC |
| 75 | NC |

| Pin | Function |
|---|---|
| 76 | NC |
| 77 | NC |
| 78 | NC |
| 79 | NC |
| 80 | EN |
| 81 | $A_0$ |
| 82 | $A_1$ |
| 83 | $A_2$ |
| 84 | $A_3$ |
| 85 | $A_4$ |
| 86 | $D_{GND}$ |
| 87 | $DV_{DD}$ |
| 88 | $DV_{NN}$ |
| 89 | $A_{GND}$ |
| 90 | $V_{SIG}$ |
| 91 | $AV_{DD}$ |
| 92 | $B_{YP}$-$AV_{NN}$ |
| 93 | $B_{YP}$-$AV_{DD}$ |
| 94 | $AV_{NN}$ |
| 95 | Anode |
| 96 | Cathode |
| 97 | $R_{SINK}$ |
| 98 | $R_{SOURCE}$ |
| 99 | $B_{YP}$-$V_{PP}$ |
| 100 | $V_{PP}$ |

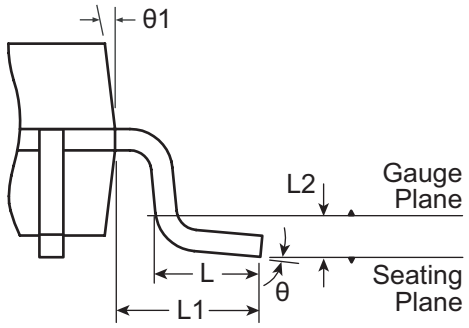
*Note: NC = No Connect*

# 100-Lead MQFP Package Outline (FG)

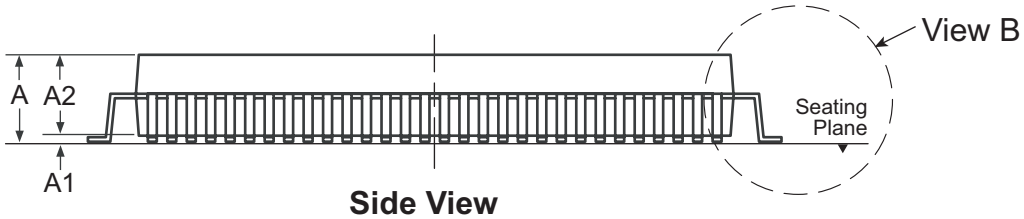
***20x14mm body, 3.15mm height (max.), 0.65mm pitch, 3.2mm footprint***




**Top View**




**View B**




**Side View**

***Note 1:***

*A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*

| Symbol | | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | θ1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 2.50 | 0.00 | 2.50 | 0.22 | 22.95 | 19.80 | 16.95 | 13.90 | 0.65 BSC | 0.73 | 1.60 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | 2.70 | - | 23.20 | 20.00 | 17.20 | 14.00 | | 0.88 | | | - | - |
| | MAX | 3.15 | 0.25 | 2.90 | 0.40 | 23.45 | 20.20 | 17.45 | 14.20 | | 1.03 | | | 7° | 16° |

*JEDEC Registration MS-022, Variation GC-2, Issue B, Dec. 1996.*

***Drawings not to scale.***



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*B121106*