Low Power Peak EMI Reducing clock synthesizer

Features

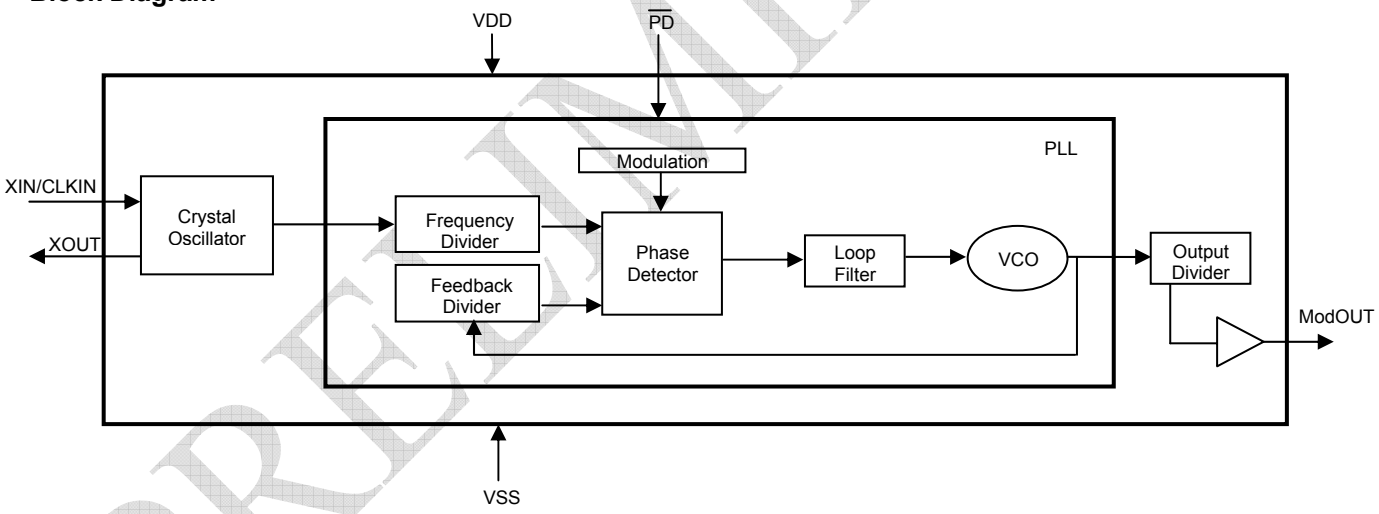
- Generates a 4x low EMI clock at the output
- Input frequency: 25 MHz
- Integrated loop filter components.
- Frequency deviation: ±0.25% (Typ) center spread
- Operates with a 3.3V Supply.
- Low power CMOS design.
- Available in 8-pin SOIC package.
- Pin compatible with ICS 341-22

Product Description

The PCS3P7101A is a low cost, single-output, clock synthesizer. The PCS3P7101A generates a 4x output clock from a 25 MHz standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving valuable board space and cost. The device employs Spread Spectrum technique to reduce system electro-magnetic interference (EMI).

The device also has a power-down feature that tri-state the clock output and turns off the PLL when the $\overline{PD}$ pin is taken low.

Block Diagram



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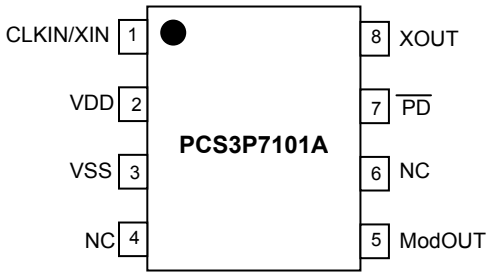
rev 0.1

Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
1	CLKIN/XIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or to an external reference clock.
2	VDD	P	Power supply for the entire chip.
3	VSS	P	Ground connection
4	NC	-	No Connection
5	ModOUT	O	Spread spectrum low EMI 4x clock output.
6	NC	-	No Connection
7	$\overline{PD}$	I	Powers down entire chip. Tri-states CLK outputs when low. Has an Internal pull-up resistor.
8	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to +70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD 22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended Operating Conditions[1]

Parameter		Min	Typ	Max	Unit
Supply voltage, V_{DD}		3.15	3.3	3.45	V
Low-level input voltage, V_{IL}	V_{DD} = 3.15V to3.45V	-	-	0.8	V
High-level input voltage, V_{IH}	V_{DD} = 3.15V to3.45V	2	-	-	V
High-level output current, I_{OH}	V_{DD} = 3.15V to3.45V	-	-	12	mA
Low-level output current, I_{OL}	V_{DD} = 3.15V to3.45V	-	-	12	mA
Operating free-air temperature, T_A		0	-	70	°C

Note:1 Unused inputs must be held high or low to prevent them from floating.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
V_{IL}	Input low voltage		VSS - 0.3	-	0.8	V
V_{IH}	Input high voltage		2.0	-	VDD + 0.5	V
I_{IL}	Input low current		-	-	-35	µA
I_{IH}	Input high current		-	-	35	µA
V_{OL}	Output low voltage (VDD = 3.3 V, I_{OL} = 12 mA)		-	-	0.4	V
V_{OH}	Output high voltage (VDD = 3.3 V, I_{OH} = 12 mA)		2.4	-	-	V
I_{DD}	Static supply current*		-	50	_	uA
I_{CC}	Dynamic supply current (3.3V, 25MHz and no load)		-	TBD	-	
VDD	Operating voltage		3.15	3.3	3.45	V
Z_{OUT}	Output impedance		-	20	-	Ω
C_{IN}	Input Capacitance		-	4	-	pF
RPD	Internal pull-up resistor	$\overline{PD}$	-	250	-	KΩ
RPUP		CLK output	-	525	-	kΩ

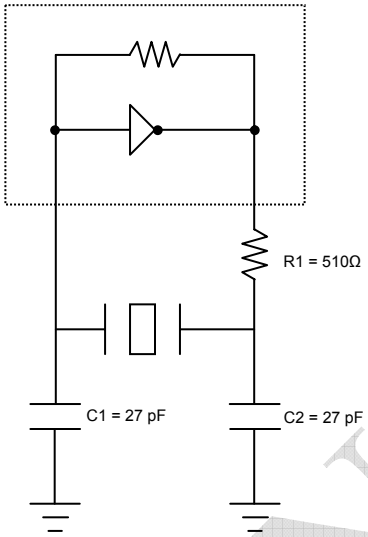
* XIN/CLKIN pin and $\overline{PD}$ pin are pulled low

AC Electrical Characteristics for 3.3V Supply

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN/XIN	Input frequency	-	25	-	MHz
ModOUT	Output frequency	-	100	-	MHz
t_{LH}*	Output rise time (measured from 0.8 to 2.0V)	-	1	-	nS
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)	-	1	-	nS
t_{PU}	Power-up time(PLL lock time from power-up)	-	4	10	mS
t_{ON}	Power-up time (first locked cycle after power-up)**	-	4	7	mS
	Synthesis Error(Output Frequency)	-	0	-	ppm
t_{JC}	Jitter (cycle to cycle)	-	TBD	-	pS
t_{JP}	Period Jitter	-	TBD	-	pS
t_D	Output duty cycle	40	50	60	%
t_{ja}	Maximum Absolute Jitter	-	TBD	-	pS

*t_{LH} and t_{HL} are measured into a capacitive load of 15pF
** V_{DD} and XIN/CLKIN input are stable, PD pin is made high from low.

Typical Crystal Oscillator Circuit

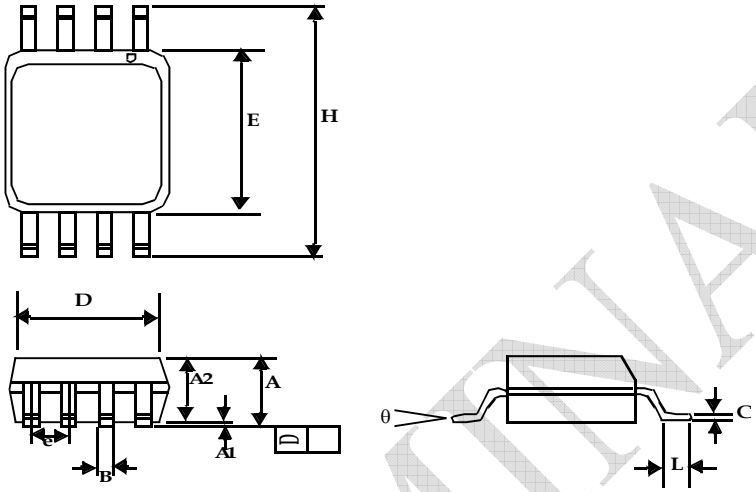


Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	25MHz
Frequency tolerance	± 50 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25Ω

Package Information

8-Pin SOIC Package

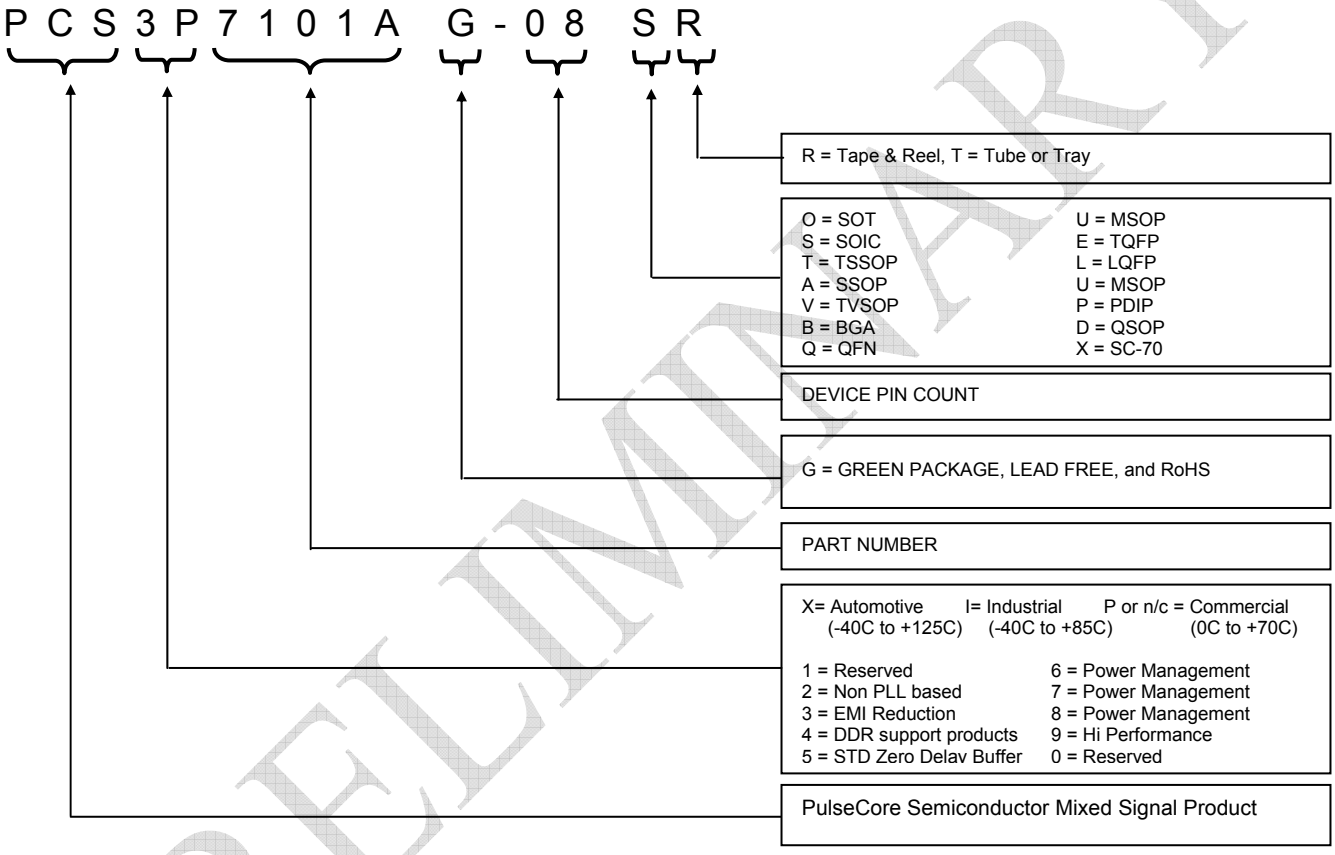


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Temperature
PCS3P7101AG-08SR	3P7101AG	8-Pin SOIC, TAPE & REEL, Green	Commercial
PCS3P7101AG-08ST	3P7101AG	8-Pin SOIC, TUBE, Green	Commercial

Device Ordering Information



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Part Number: PCS3P7101A
Document Version: v0.1

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003