

GENERAL DESCRIPTION

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

PIN CONFIGURATION

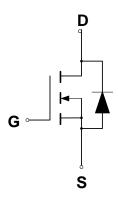
TO-220/TO-220FP Top View

GATE SOURCE SOURCE SOURCE

FEATURES

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and V_{DS}(on) Specified at Elevated Temperature

SYMBOL



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current – Continuous		8.0	А
- Pulsed	I _{DM}	24	
Gate-to-Source Voltage – Continue		±30	V
 Non-repetitive 	V_{GSM}	±40	V
Total Power Dissipation	P _{D(Max)}		W
TO-220		83	
TO-220FP		30	
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy $-$ T _J = 25 $^\circ\!\!\mathbb{C}$		320	mJ
$(V_{DD} = 100V, V_{GS} = 10V, I_L = 8A, L = 10mH, R_G = 25\Omega)$			
Thermal Resistance – Junction to Case		1.0	°C/W
 Junction to Ambient 	θ _{JA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T∟	260	°C



ORDERING INFORMATION

Part Number	Package
CMT08N50GN220*	TO-220
CMT08N50GN220FP*	TO-220 Full Package
CMT08N50XN220*	TO-220
CMT08N50XN220FP*	TO-220 Full Package

*Note : G : Suffix for PB Free Product

X : Suffix for Halogen Free and PB Free Product

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_{\rm J}$ = 25 $^\circ\!{\rm C}$.

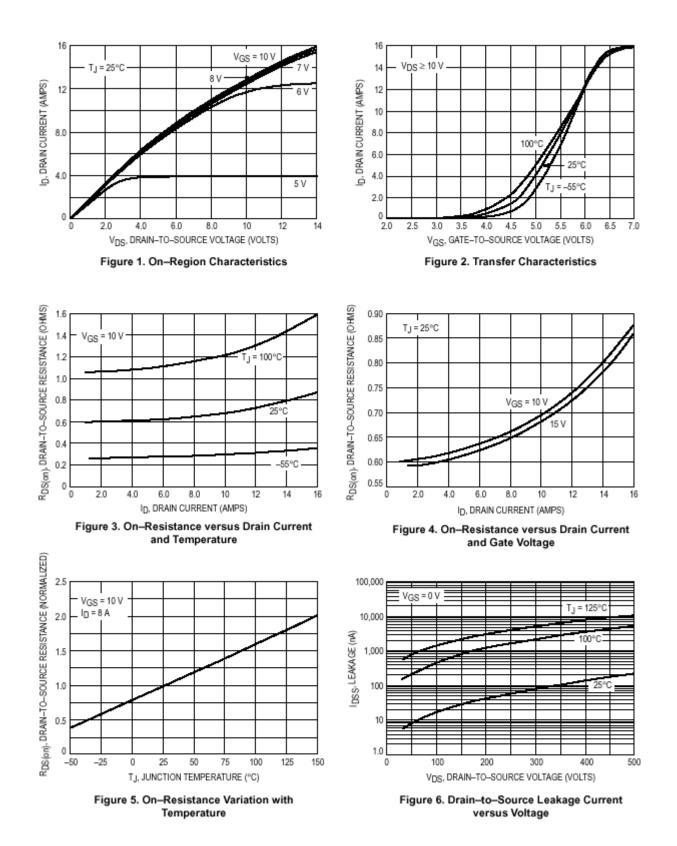
			CMT08N50			
Characteristic		Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		V _{(BR)DSS}	500			V
$(V_{GS} = 0 \text{ V}, I_D = 250 \ \mu \text{ A})$						
Drain-Source Leakage Current		I _{DSS}				$\mu \mathbf{A}$
$(V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V})$					1	
(V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125℃)					3	
Gate-Source Leakage Current-Forward		I _{GSSF}			100	nA
$(V_{gsf} = 30 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate-Source Leakage Current-Reverse		I _{GSSR}			100	nA
$(V_{gsr} = -30 \text{ V}, \text{ V}_{DS} = 0 \text{ V})$						
Gate Threshold Voltage		V _{GS(th)}	2.0		4.0	V
$(V_{DS} = V_{GS}, I_D = 250 \ \mu A)$						
Static Drain-Source On-Resistance (V _{GS} = 10 V, I _D = 4.0A) *		R _{DS(on)}			0.7	Ω
Drain-Source On-Voltage (V _{GS} =	10 V)	V _{DS(on)}		5.0	7.2	V
(I _D = 8.0 A)						
Forward Transconductance (V_{DS} = 50 V, I_D = 4.0A) *		g fs	4.9			mmhos
Input Capacitance		Ciss		1450		pF
Output Capacitance	(V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz)	Coss		190		pF
Reverse Transfer Capacitance	1 – 1.0 Wi 12)	Crss		45.4		pF
Turn-On Delay Time		t _{d(on)}		15		ns
Rise Time		tr		33		ns
Turn-Off Delay Time	$(R_{Go} + C17n = 9.1\Omega) *$	t _{d(off)}		40		ns
Fall Time		t _f		32		ns
Total Gate Charge		Qg		40		nC
Gate-Source Charge	$(V_{DS} = 400 \text{ V}, I_D = 8.0 \text{ A},$	Q _{gs}		8.0		nC
Gate-Drain Charge	V _{GS} = 10 V)*	Q _{gd}		17		nC
Internal Drain Inductance		LD		4.5		nH
(Measured from the drain lead 0.25" from package to center of die)						
Internal Drain Inductance		Ls		7.5		nH
(Measured from the source lead 0.25" from package to source bond						
pad)	·					
SOURCE-DRAIN DIODE CHAR	ACTERISTICS					
Forward On-Voltage(1)		V _{SD}			1.5	V
Forward Turn-On Time	$(I_{\rm S} = 8.0 \text{ A}, V_{\rm GS} = 0 \text{ V},$	t _{on}		35		ns
Reverse Recovery Time	d _{ιS} /d _t = 100A/μs)	t _{rr}		75		ns

* Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%

** Negligible, Dominated by circuit inductance

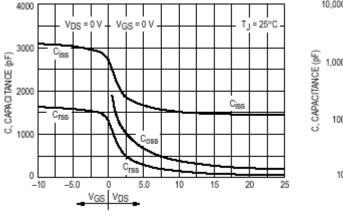


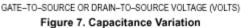
TYPICAL ELECTRICAL CHARACTERISTICS



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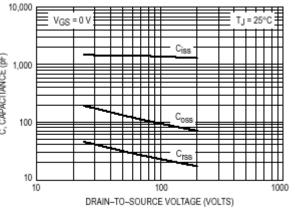
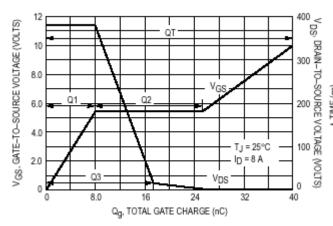
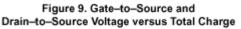
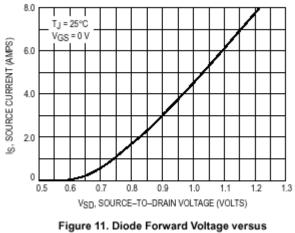


Figure 8. High Voltage Capacitance Variation







Current

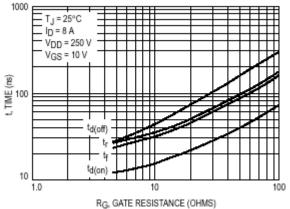


Figure 10. Resistive Switching Time Variation versus Gate Resistance

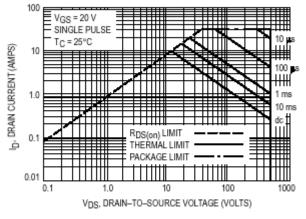


Figure 12. Maximum Rated Forward Biased Safe Operating Area



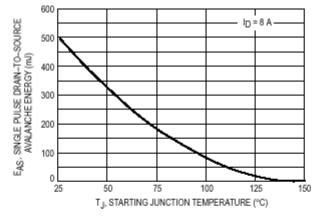


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

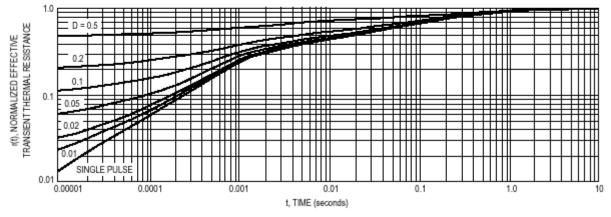
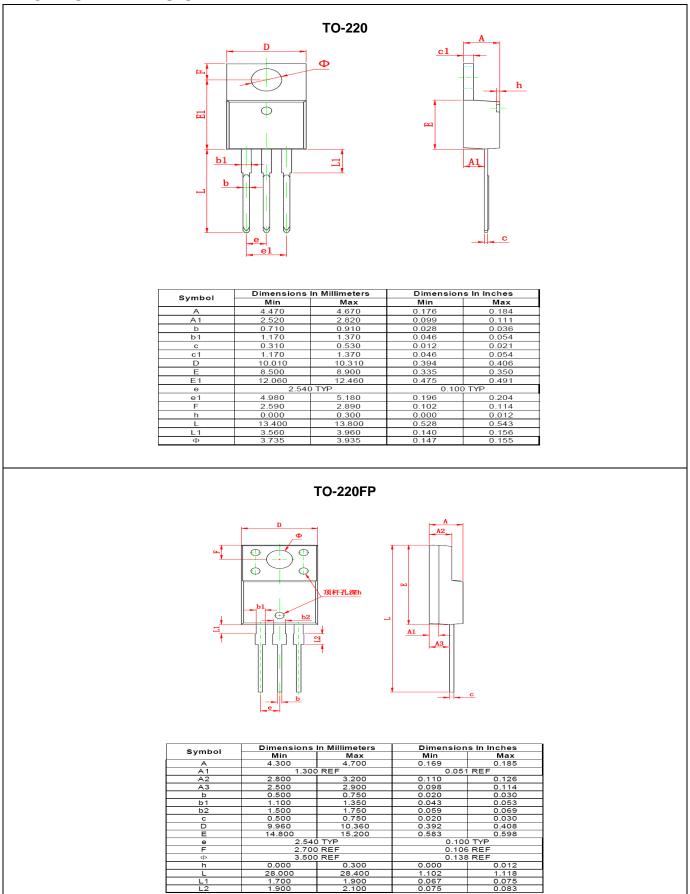


Figure 14. Thermal Response



PACKAGE DIMENSION





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HsinChu Headquarter	Sales & Marketing
5F, No. 11, Park Avenue II, Science-Based Industrial Park, HsinChu City, Taiwan	21F., No. 96, Sec. 1, Sintai 5th Rd., Sijhih City, Taipei County 22102, Taiwan, R.O.C.
TEL: +886-3-567 9979	TEL: +886-2-2696 3558
FAX: +886-3-567 9909	FAX: +886-2-2696 3559