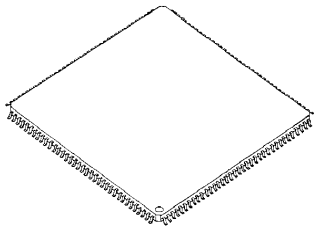
Static 1/2 1/3 1/4 Duty LCD Driver

■ GENERAL DESCRIPTION

The **NJU6541A** is a Static or 1/2,1/3,1/4 duty segment type LCD driver. It incorporates 4 common driver circuits and 120 segment driver circuits. The **NJU6541A** can drive maximum 480 segments in 1/4 duty ratio, and can use I^2C F/S mode.
In addition, the **NJU6541A**'s useful functions meet a wide range of applications.

■ PACKAGE OUTLINE

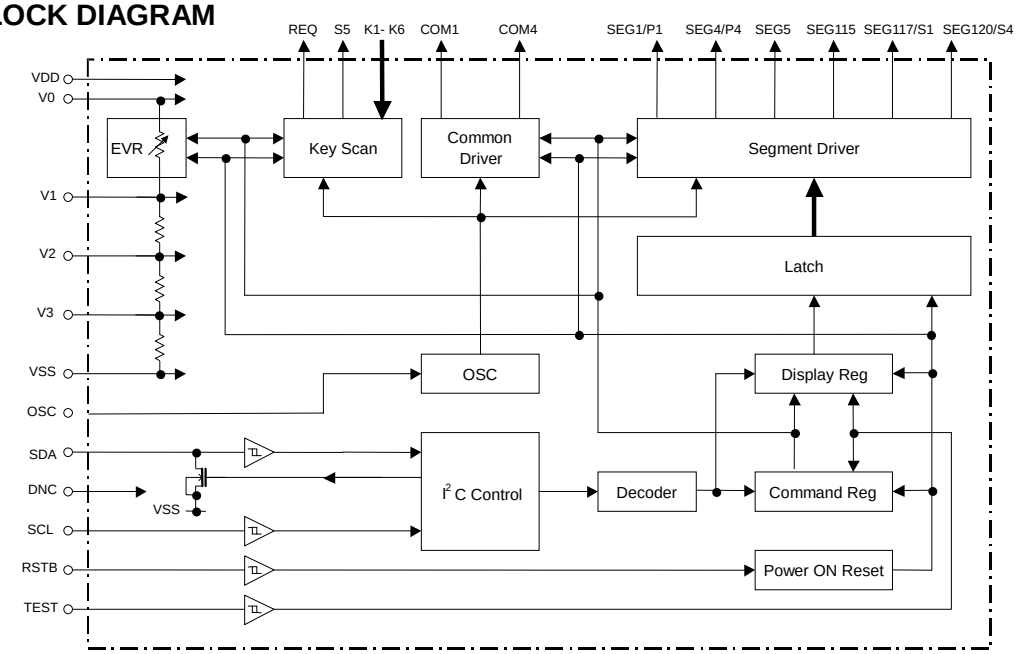


NJU6541A

■ FEATURES

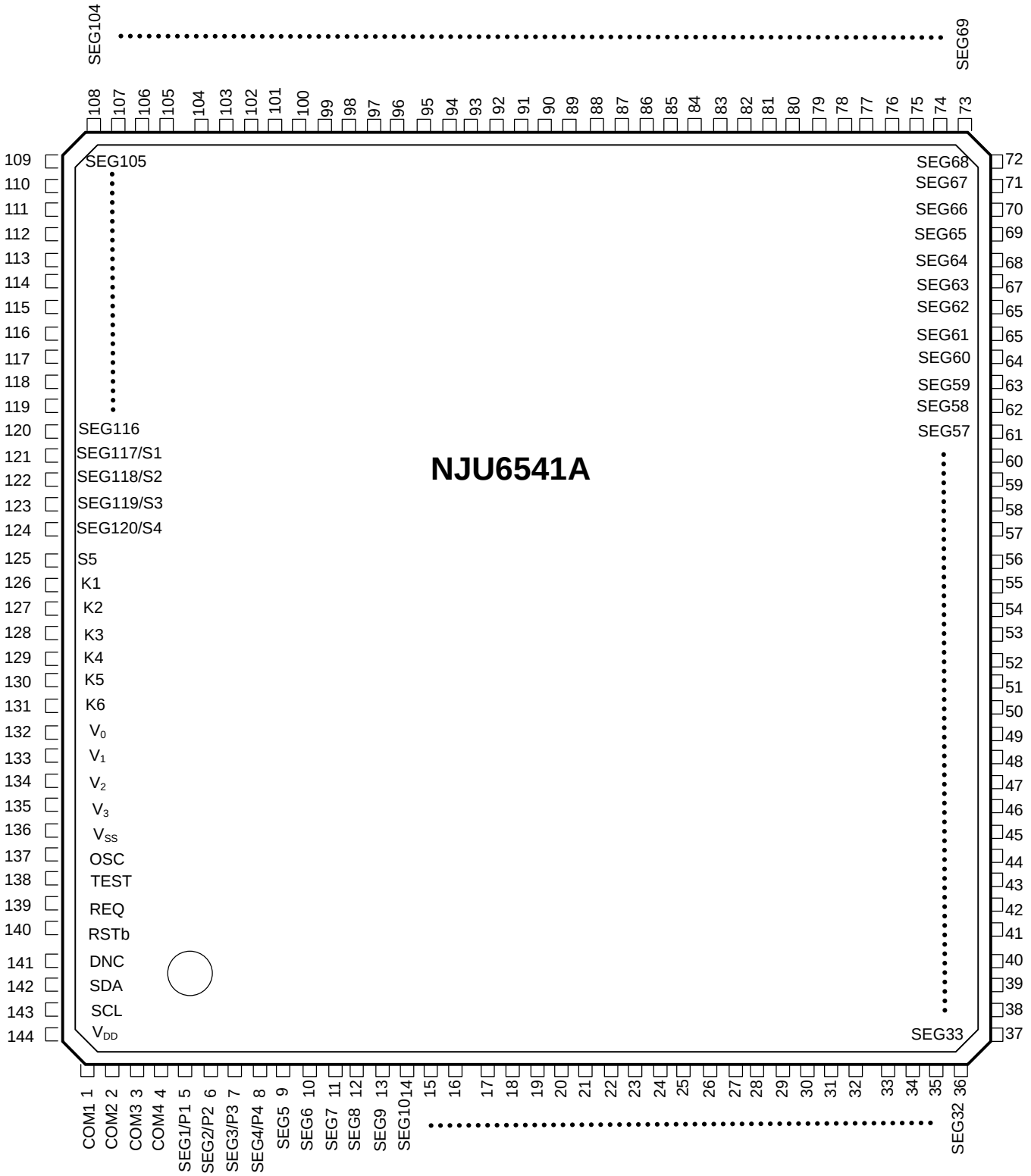
- LCD driving circuit :Max. 120outputs (4 outputs as for general purpose ports)
- Programmable Duty Ratio
  - Static :Driving max. 120 segments
  - 1/2 Duty Ratio :Driving max. 240 segments
  - 1/3 Duty Ratio :Driving max. 360 segments
  - 1/4 Duty Ratio :Driving max. 480 segments
- General Purpose Port :Driving max 4outputs (SEG1-SEG4:4outputs as for general purpose ports)
- Key Scan Function :Max 30Key(5-out x 6-in matrix)
- Programmable Bias Ratio :1/2, 1/3 bias ratio (Static:1/1)
- I^2C-bus Interface :F/S mode slave address 0111_000*
  (*: Read/ Write mode distinction: 0=write, 1=read)
- Oscillator :CR oscillation with external resistor and capacitance, or external oscillation signal input
- Operating Wave Form :A wave form, B wave form
- Electrical Variable Resistance :8-steps
- Power ON Initialize Circuit On-Chip
- Useful Instruction Set :Duty select, Bias select, Wave form select, Oscillation select, Segment or general purpose ports select, Segment or Key scan output select, E.V.R select, Display ON/OFF, Key scan ON/OFF
- Operating Voltage :3.0V / 5.0V
- C-MOS Technology :P-Sub
- Package Outline :LQFP144 20mm*20mm t=1.7mm(max) Pin-pitch=0.5mm

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

• QFP144



■ TERMINAL DISCRIPTION

No.	Pad Name	Function
132	V_0	LCD driving voltage $V_0 \geq V_{DD}$
133 134 135	V_1 V_2 V_3	Bias At 1/3 bias ratio, keep V_2- V_3 open. At 1/2 bias ratio, short V_2- V_3.
136	V_{SS}	GND V_{SS} =0V
137	OSC	External resistor and capacitance connection terminal for CR oscillation, or external clock input terminal
138	TEST	TEST Keep TEST-V_{SS} short
139	REQ	Request operation outputs for Key scan
140	RSTb	Reset When RSTb is “L", command register and latch circuit is reset. When this terminal is not used, should be V_{DD} short. (keep power supply condition when hardware reset circuit is used)
141	DNC	Don’t connect
142	SDA	I^2C Serial data I/O terminal
143	SCL	Serial data Transmission clock input
144	V_{DD}	Power supply: 3V /5V
1-4	COM1 ~ COM4	Common driver outputs
5-8	SEG1/P1~SEG4/P4	Segment driver outputs/general purpose output ports These 4 terminals can be used as segment outputs or general purpose output ports by setting Command Register. When selected as general purpose ports, data can be outputted via these ports during COM1 timing. According to transferred data, "H"=V_{DD} or "L"=V_{SS} will be outputted.
9~120	SEG5 ~ SEG116	Segment driver outputs
121~124	SEG117/S1 ~ SEG120/S4	Segment driver outputs / Key scanning output These 4 terminals can be used as segment outputs or Key scanning output terminal by the instruction.
125	S5	Key scanning output
126~131	K1 ~ K6	Key scanning inputs

■ FUNCTION DESCRIPTION

(1) Block Function

- Interface
  I^2C Interface circuit. F/S mode control

- Oscillator
  The oscillator includes an external capacitor and an resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC.

- Decoder
  Input serial data is decoded and sent to the appropriate block.

- Command Register
  Command data is written to this 8 bits command register to control the **NJU6541A** operation.

- Display Data Register
  Data is written to this 8 bits register as display data.

- Latch Circuit
  Data stored in display data register is assigned to the corresponding SEG/port.

- Segment Driver/Key scan/General Purpose Ports
  Basing on display data, segment drivers output LCD SEG driving signal.
  And, SEG1/P1 ~ SEG4/P4 terminals can be selected as segment driver output or general-purpose ports by instruction, SEG117/S1~SEG120/S4 terminals can be selected as segment driver output or Key scan outputs by instruction.

- Common Driver
  Common drivers output LCD COM driving signal.

- Power On Reset
  When power is on, The **NJU6541A** is automatically initialized. And if RSTb="L", The **NJU6541A** is reset too.

- Electrical Variable Resistance (E.V.R.)
  The Electrical Variable Resistance adjusts LCD Driving Voltage from V1 to V3.

- Key scan
  The Key scan controls to input from external Key data.

(2) I²C Serial Data Transfer

The NJU6541A transfer of data comply with I²C specification.

Data format is show below(Fig1). After input the slave address, the input of the instruction data or the display data becomes possible.

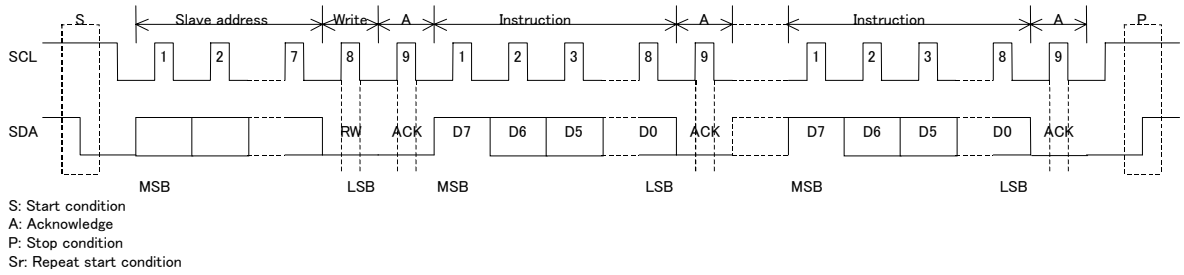


Fig1

After input the instruction data, It becomes possible to write the display data continuously by setting the display address.

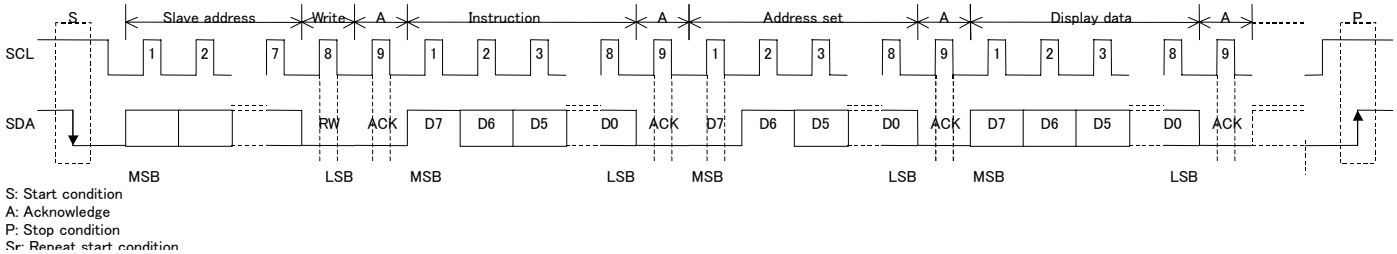


Fig2

However, after setting the display address, it becomes possible to input only the display data. Therefore, the acceptance of the instruction data is impossible as long as the repeat start condition or the stop condition is not executed.

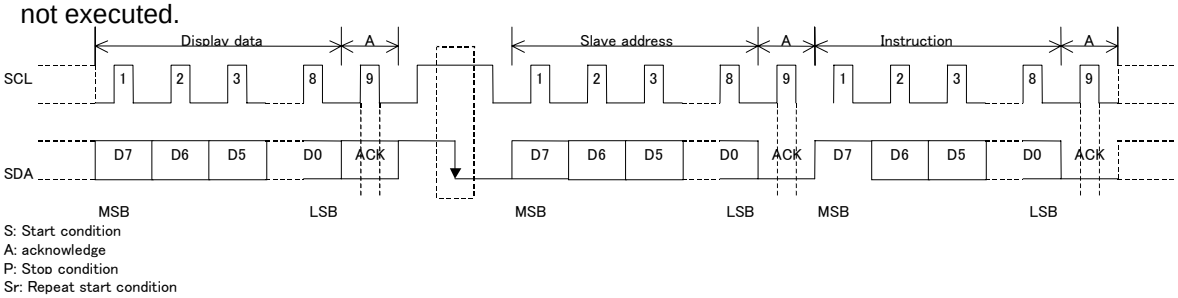
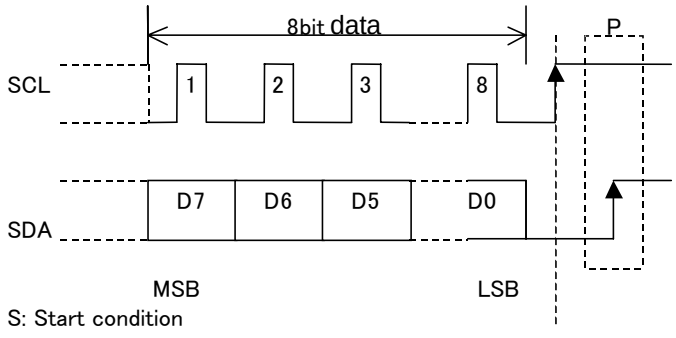


Fig3

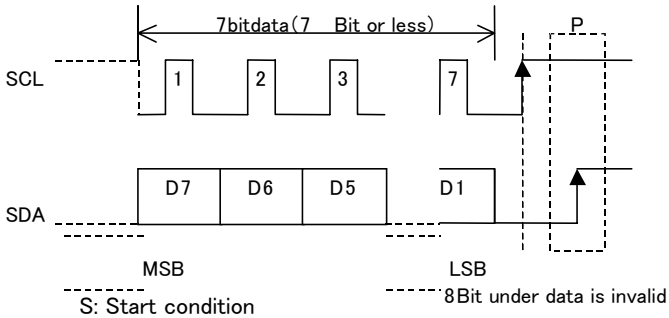
1) Start condition
   A fall edge of the SDA terminal while the SCL terminals “H”, which situation define the Start conditions.
2) Slave address
   First bite defines the slave address of the NJU6541A. Slave address is (0111_000*). When the NJU6062 acknowledge coincidence its own address with the address in the first byte, it output the acknowledge just the first byte(at ninth bit timing) through the SDA terminal.
3) Read/Write condition
   The data is R/W signal in the first byte(at eighth bit timing) . The eighth bit timing “H” is write. The eighth bit timing “L” is read.
4) Data
   After 2nd bite, transfer the display bite. After input the slave address, the input of the instruction data or the display data(series) becomes possible.
5) Stop condition
   A rise edge of the SDA terminal while the SCL terminal is “H”, which situation defines the STOP condition.
6) Repeat start condition
   After start condition set, a fall edge of the SDA terminal while the SCL terminals “H”, which situation next data read start.

Note)
The NJU6541A read the rising edge of SCL after eight clock. When the master execute stop condition after eighth clock(before ACK), eighth data is valid. However, when the master execute stop condition under eight clock, data is invalid.



S: Start condition
A: Acknowledge
P: Stop condition
Sr: Repeat start condition

Fig4



S: Start condition
A: Acknowledge
P: Stop condition
Sr: Repeat start condition

Fig5

Instruction

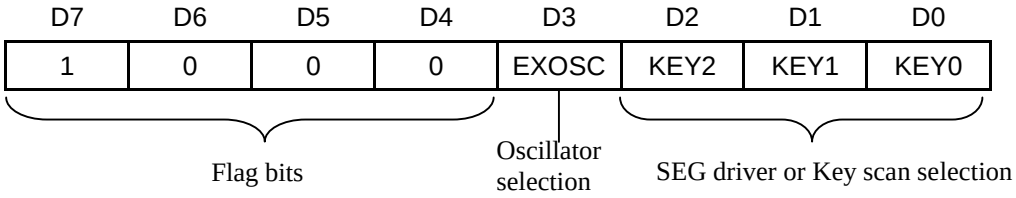
Instruction	Code								Content
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Command Register1	1	0	0	0	EXOSC	KEY2	KEY1	KEY0	・FOSC select ・Segment/ Key scan select
Command Register2	1	0	0	1	WSEL	TSEL2	TSEL1	TSEL0	・Operating wave form ・Segment/ general output select
Command Register3	1	0	1	0	BS	E2	E1	E0	・Bias select ・E.V.R select
Command Register4	1	0	1	1	SK1	SK0	DS1	DS0	・Display control ・Key scan ON/OFF ・Duty select
Address counter	0	1	C1	C0	S3	S2	S1	S0	・Output address register

Command Register1

Command Register1 is used to set the duty ratio, the bias ratio, and the SEG driver/Key scan. When the D7 ~ D4 bits of the 1st word are (1,0,0,0), the D3 ~ D0 bits are recognized as command data1.
The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- SEG driver/Key scan : SEG drivers(SEG117,SEG118, SEG119, SEG120)



- Oscillator selection

EXOSC	Oscillator circuit
0	External resistor and capacitor
1	External oscillation signal input

- SEG driver or Key scan

KEY2	KEY1	KEY0	SEG117/K1	SEG118/K2	SEG119/K3	SEG120/K4
0	0	0	SEG117	SEG118	SEG119	SEG120
0	0	1	SEG117	SEG118	SEG119	K4
0	1	0	SEG117	SEG118	K3	K4
0	1	1	SEG117	K2	K3	K4
1	0	0	K1	K2	K3	K4

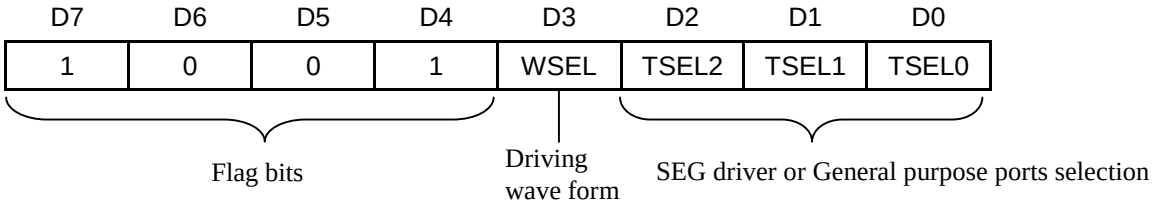
*) If KEY2 ~ KEY0 is set to (1, 0, 1), (1, 1, 0), (1, 1, 1) all outputs are used as segment drivers.

(5) Command Register2

Command Register2 is used to set the duty ratio, the bias ratio, and the SEG driver/general purpose ports. When the D7 ~ D4 bits of the 1st word are (1,0,0,1), the D3 ~ D0 bits are recognized as command data2. The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- SEG driver/General purpose ports : SEG drivers(SEG1,SEG2, SEG3, SEG4)



- Driving waveform

Driving waveform is chosen according to the characteristic of a panel.

WSEL	Driving waveform
0	A(Time sharing system frequency) waveform
1	B(Flame reversal) waveform

*) Do not change the driving waveform during display ON.

- SEG driver or General purpose ports

TSEL2	TSEL1	TSEL0	SEG1/P1	SEG2/P2	SEG3/P3	SEG4/P4
0	0	0	SEG1	SEG2	SEG3	SEG4
0	0	1	SEG1	SEG2	SEG3	P4
0	1	0	SEG1	SEG2	P3	P4
0	1	1	SEG1	P2	P3	P4
1	0	0	P1	P2	P3	P4

*) If TSEL2 ~ TSEL0 is set to (1, 0, 1), (1, 1, 0), (1, 1, 1) all outputs are used as segment drivers.

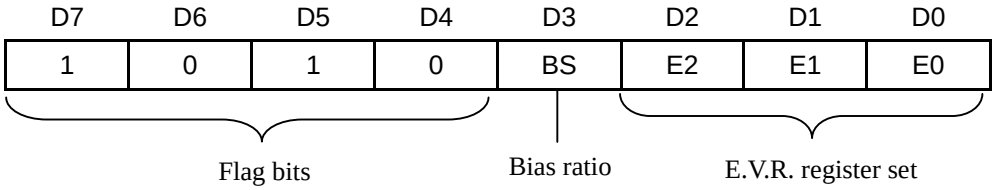
(6) Command Register3

- Command Register3 is used to set the Bias ratio and E.V.R. resister set. When the D7 to D4 bits of the 1st
- word are (1,0,1,0), the D3 ~ D0 bits are recognized as command data3.

The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- Oscillator selection : External resistor and capacitor
- Bias ratio selection : 1/3
- E.V.R. Register Set : V0(0,0,0)



- Bias ratio

BS	Bias ratio
0	1/3
1	1/2

*) Do not change the Bias ratio during display ON.
**)If Bias is set to 1/2, short V_2-V_3.
**)If 1/1 Duty is select, Bias is set to 1/1 Bias regardless of Bias ration selection.

- E.V.R. resister set

E.V.R. resistor set instruction adjusts the contrast of the LCD, by 3-bits selects(E2,E1,E0).
One LCD driving voltage VLCD out of 8 voltage-stages by setting E.V.R. register.
Set the binary code “000” when contrast adjustment is unused.

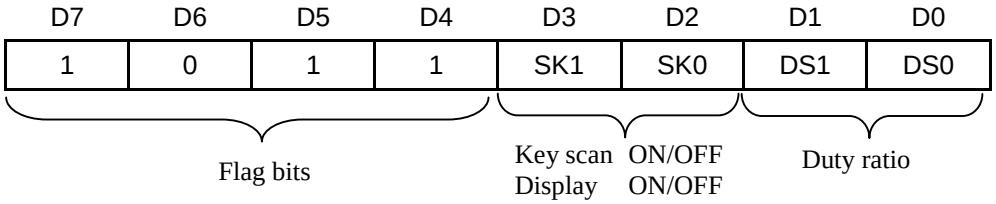
E2	E1	E0	V1		V_0 (V_0~V_{SS})
			1/2bias	1/3bias	
0	0	0	V_0	V_0	High
0	0	1	$0.933V_0$	$0.955V_0$	:
0	1	0	$0.875V_0$	$0.913V_0$	:
0	1	1	$0.824V_0$	$0.875V_0$	:
1	0	0	$0.778V_0$	$0.840V_0$	:
1	0	1	$0.737V_0$	$0.808V_0$	:
1	1	0	$0.700V_0$	$0.778V_0$	:
1	1	1	$0.667V_0$	$0.750V_0$	Low

(7) Command Register4

- Command Register4 is used to set the Key scan ON/OFF, Display ON/OFF, Duty ratio. When the D7 to D4 bits of the 1st word are (1,0,1,1), the D3 ~ D0 bits are recognized as command data4.
  The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- Display control : Display ON
- Key scan ON/OFF selection : Key scan OFF
- Duty ratio selection : 1/4 Duty



- Display control and Key scan ON/OFF

  It is used to set the Key scan ON/OFF, Display control.
  The Oscillator circuit stop(OFF) only when the Display and Key scan are OFF((SK1,SK0)=(0,0)).
  The Key-input is not accepted at all when Key scan is OFF.
  Even during Display OFF, interface can be accessed, and data can be written into the command register, address counter and data register

SK1	SK0	Display	Key scan	Oscillator
0	0	OFF	OFF	OFF
0	1	OFF	ON	ON
1	0	ON	OFF	ON
1	1	ON	ON	ON

*) When Display OFF

- All segment and common terminal output are V_{SS}
  (When general purpose output ports are selected, even Display OFF, these ports can output data)
- V_1 , V_2 and V_3 become V_0 (no current pass through the bleeder resistors)

- Duty ratio
  - It is used to set the Duty selection. When duty select 1/1, Bias is 1/1, breeder resostance is open between from V1 to Vss.
  -

DS1	DS0	Duty ratio
0	0	1/4
0	1	1/3
1	0	1/2
1	1	1/1

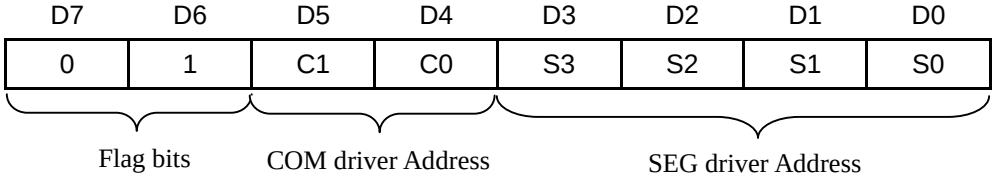
*) Do not change the duty ratio during display ON.

(8) Output Address Counter

Output Address Counter will specify the addresses of the SEG and COM drivers for the display data.
When the MSB (D7 to D6) of the 1st data is “01”, the LSB 6 bits (D5 to D0) specify the addresses of COM and SEG drivers, and the 2nd data is the display data which will be sent to the 1st-data-specified drivers. At the same time, SEG and COM driver addresses will be increased automatically shown in **Table 1**. In other words, as of the SEG and COM driver addresses specified by the first data in the Output Address Counter, display data can be transferred to the SEG and COM drivers without further address setting.
The address setting range is from "00_0000" to "11_1110. if the data transferred additionally , then it will be reset to “00_0000” and renew the auto-increment operation. If it set the data without range by Duty select, the data can not show the display.

Output Address counter default setting
Output Address counter (C1, C0, S3, S2, S1, S0)=(0, 0, 0, 0, 0, 0)

- Address Data



Address range depend on Duty

DUTY	Address range
1/1	00 0000～00 1110
1/2	00 0000～01 1110
1/3	00 0000～10 1110
1/4	00 0000～11 1110

Address range＝[C1][C0]_[S3][S2][S1][S0]

Table 1. The Relationship Between Output Address and SEG/COM Drivers

C1	C0	S3	S2	S1	S0	COM Driver	SEG Driver							
							D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	COM1	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
0	1	0	0	0	0	COM2	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
1	0	0	0	0	0	COM3	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
1	1	0	0	0	0	COM4	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120

Increment Direction

- ✧ If general purpose ports are selected by Command Register, under (C1, C0, S3, S2, S1, S0)=(0, 0, 0, 0, 0, 0), D4 ~ D7 bits are the addresses of (P1, P2, P3, P4) ports which corresponds to (SEG1,SEG2, SEG3, SEG4).
- ✧ When SEG1~SEG4 are set as general purpose output ports, data for SEG1~SEG4 during COM2~COM4 scanning will be ignored.
- ✧ When SEG117~SEG120 are set as Key ports, data for SEG117~SEG120 will be ignored.

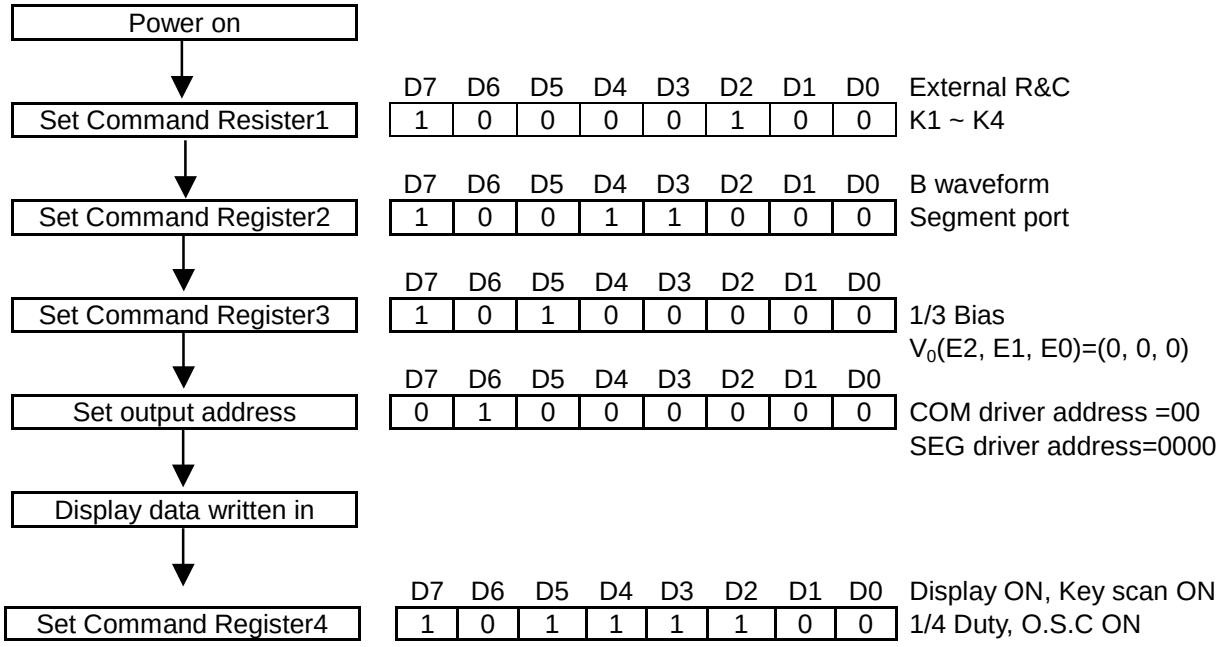
(9) Power ON Reset

After power ON, **NJU6541A** is initialized to the following values:

- Address counter (C1, C0, S3, S2, S1, S0)=(0, 0, 0, 0, 0, 0)
- Display data register all "0"
- Duty ratio 1/4 duty
- Bias ratio 1/3 bias
- Oscillator selection External resistor and capacitor
- Driving waveform A waveform
- E.V.R. resister V_0(E2, E1, E0)=(0, 0, 0)
- Segment/General purpose port Segment output(SEG1,SEG2, SEG3, SEG4)
- Segment/Key scan Segment output(SEG117,SEG118, SEG119, SEG120)
- Display OFF
- Key scan OFF

(10) Sequence of Initialization

1/4 duty,1/3 bias,SEG1 ~ SEG4 used as SEG drivers, SEG117 ~ SEG120, external resister and capacitor, B waveform, E.V.R. V_0(E2, E1, E0)=(0, 0, 0) data written in from COM1.



(10) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates LCD driving bias voltages V_1 , V_2 and V_3. It adjusts the voltage by 8 steps electrical volume from V_0 and allots the voltage to V_0, V_1 , V_2 and V_3 by resistor-voltage-dividing as shown in below.
V_0, V_1, V_2 and V_3 terminals requires external capacitors for bias voltage stabilization for display quality. These values of capacitors should be fixed in accordance with evaluation in the application.

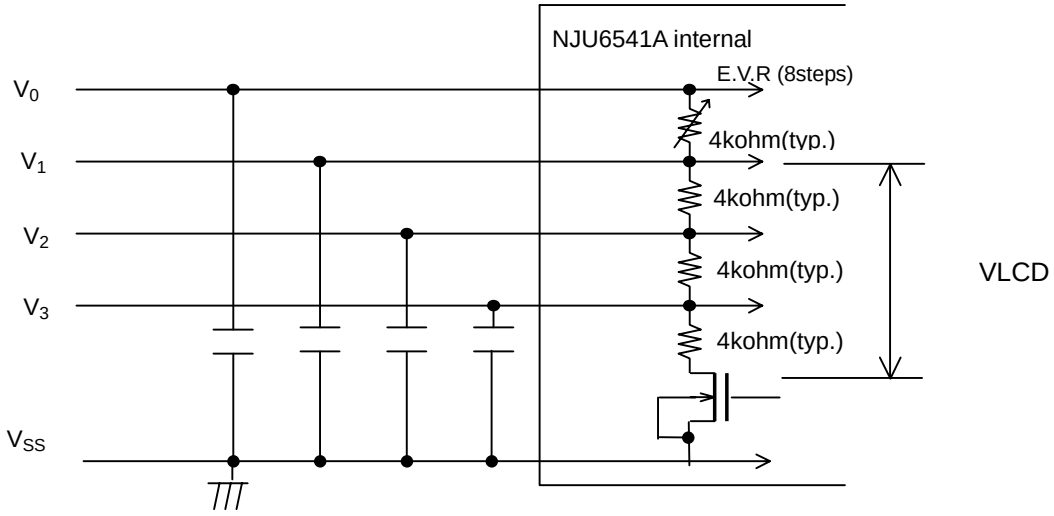
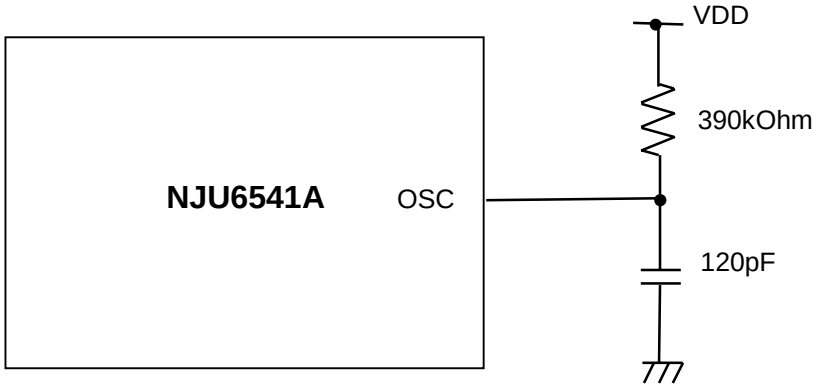


Fig6

When the E.V.R. is not used, V1 terminal should connect to V0.
When the **NJU6541A** operates as 1/2 bias operation, V2 terminal should connect to V3.
When it select 1/1 duty, between V1 and Vss do not pass current by COS switch open.

(11) Oscillator circuit

The oscillator includes an external capacitor and an resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC.



(f_{OSC}=15.4kHz TYP)

Fig7

(12) Keyscan circuit

The Key scan circuit consists of a detector block of key pressing and a fetching block of key status. It scans 5x6 key matrix and fetches conditions of 30 keys. Furthermore, it operates correctly against the key roll over input.

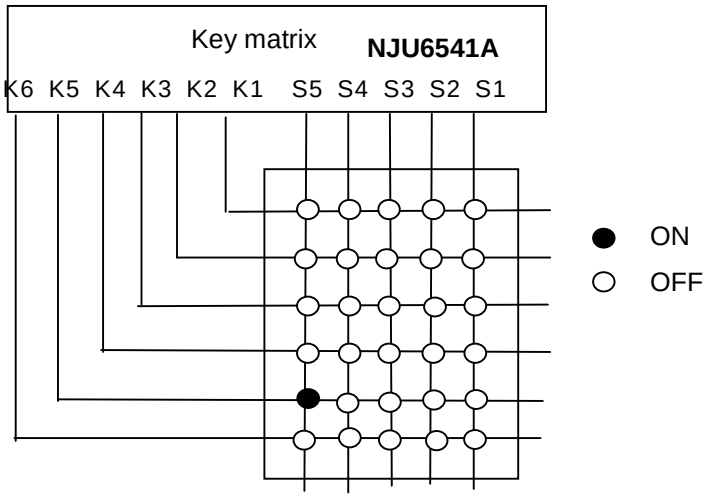


Fig8

(12-1) Timing of Key scan

Key scan cycle is 160 x T[S](T=1/fosc). The data of key scan is a result of comparison with a couple of Key scan for correct judge whether Key On or Off. When the result of comparison is correct (accord), the NJU6541A recognizes Key On and outputs “L” level from REQ terminal after 416 x T[S] from start of Key scan for a request to read key data out to external CPU. When the REQ terminals outputs “L” signal, the key scan does not operate until end of key data reading by CPU, and scanned key data is kept. When the result of comparison is incorrect (not accord), Key scan operates again if any key is On. It read Key scan data without regard to REQ “H” or “L”.

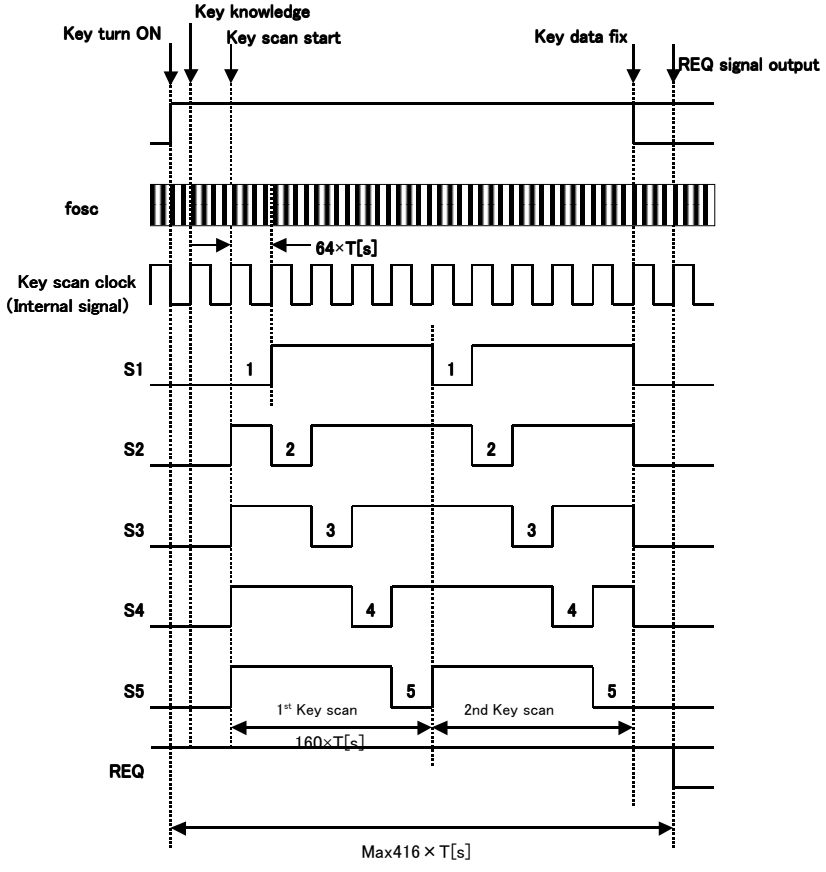


Fig9

12-2) Request signal output

When the **NJU6541A** detect the key-in to scan start by the key scan circuit, it outputs “L” signal as the request signal from the “REQ” terminal to notice the key pressing information to an application system. The request signal resets to “H” level after key scan data read.

12-3) Contents of key register renewal

Contents of key register are no fixed in case of no key operation.

Contents of key register are not changed in busy of key data reading operation.

It stops when a couple of data by continuously twice key scan operations are accorded and fixed as a correct key status. The correct key status data is stored and newly key scan operation does not start until external CPU reads data out after key status is fixed.

When a key on the key matrix is pressed, the bit corresponding to terminals (S1 to S5, K1 to K6) connected the switch goes to “1” and another bits go to “0”.

In case of Example 1, when the switch connecting to K5 and S5 is pressed, bit (KD29) corresponding to S5 and K5 go to “1” but another bits go to “0”.

Example 1. One key is pressed

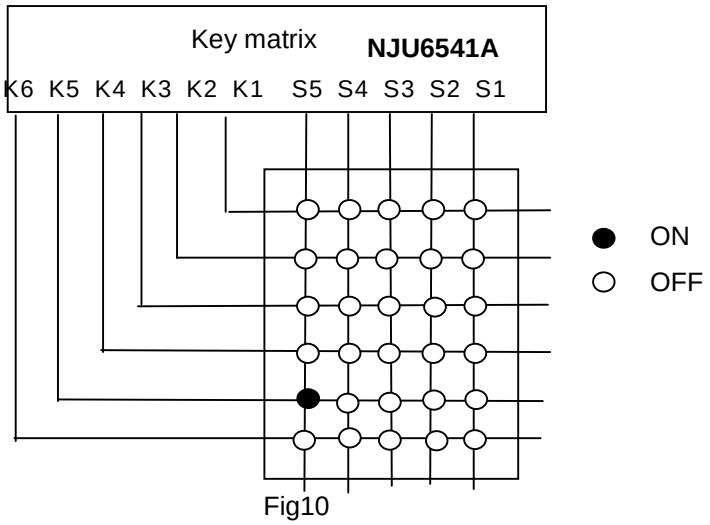


Fig10

Key register

	K1	K2	K3	K4	K5	K6
S1	KD1	KD2	KD3	KD4	KD5	KD6
S2	KD7	KD8	KD9	KD10	KD11	KD12
S3	KD13	KD14	KD15	KD16	KD17	KD18
S4	KD19	KD20	KD21	KD22	KD23	KD24
S5	KD25	KD26	KD27	KD28	KD29	KD30

12-4) Format of Key scan data

Key register data was outputted by I2C bus. Key register reading is two method, one is REQ signal method, another is a method of always requesting reading.

12-4-1) REQ signal method

When there is "Read" mastering request when REQ is "L", after the slave address is specified, the method of outputting data outputs the key register data to KD30-KD1 separately for five of every eight bits (upper 2bits is dummy data =”H”) data. NJU6541A doesn't reset the data of the Key register until all the Key register data of KD30-KD1 is sent to the master, and the stop condition is executed. The key input is not accepted. The ACK data is not sent from the master, and data in the key register is maintained when ending on the way of the data transfer. The key data is output from KD30 when the master reads NJU6541A the key data again.

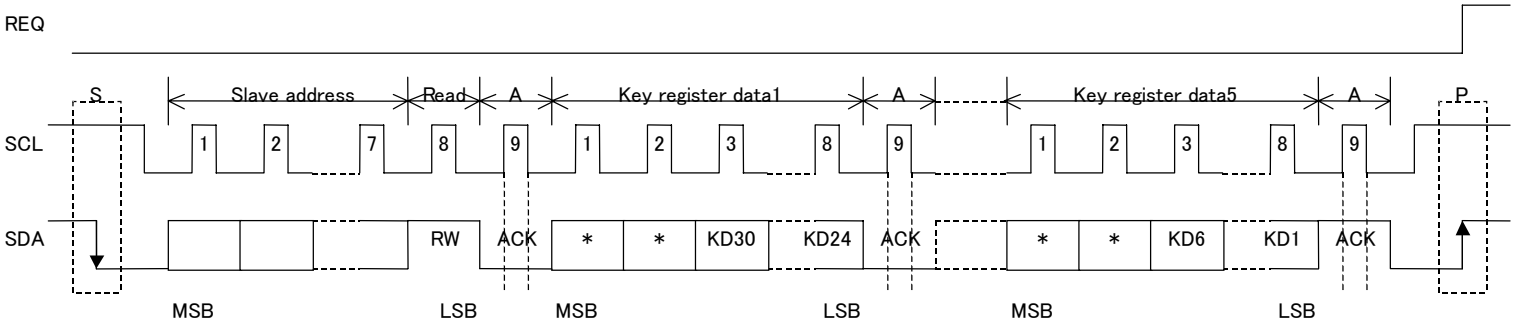
12-4-2) REQ signal is not used.

NJU6541A can transmit the data of the key register If reading is requested by the master when the REQ signal is "H".

When the key is pushed : The key register is maintained until reading the key data is completed.
When the key is not pushed : "L" is output.(NJU6541A doesn't output the data of the key register, and "L" is output. All the time, "L" is output to the master though the key data is maintained in the key register when the key is pushed. When the key data is read again after reading ends, the data of the key register is output.)

12-5) Example of Key scan output

After the slave address is fixed, the data of the key register is output from KD30. The first two bits are the dummy data("H") at the key register data transfer. Six bits are three bit key data from now on.
This is forwarded five times, and the data of 30 keys is transmitted. The terminal REQ is fixed to "H" when the STOP condition is executed after key register 1-5 is transmitted, and all data in the key register is fixed to "L".

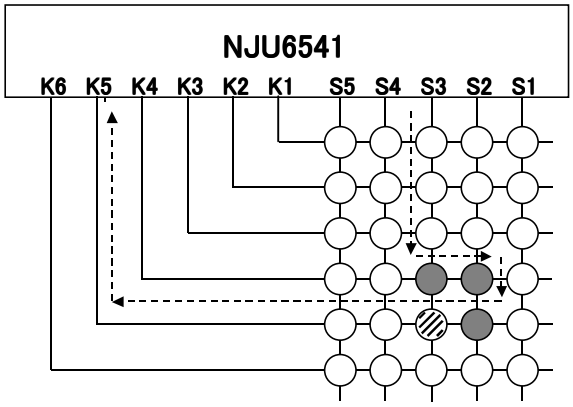


S: Start condition
A: Acknowledge
P: Stop condition
Sr: Repeat start condition

Fig11

12-6) Key More Input

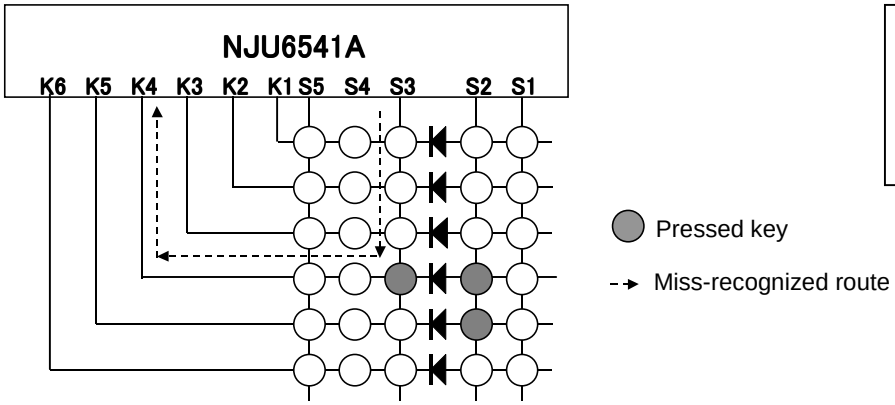
non-pressed key data may change pressed key data in triple or more key Input as shown in Fig. 1 and incorrect key data may be output to external CPU. For prevention of miss-recognition by incorrect key data, diodes should be inserted or control program of CPU should ignore the combination of key data miss-recognition. For example, 4 keys and more ON data should be ignored.



In case of 3 keys operation in left picture, if S4 terminal outputs "L" signal, this signal goes around on the dotted line and non-pressed key is miss-recognized as pressed key.

Pressed key
Miss-recognized key
Miss-recognized route

Fig12



For prevention of miss-recognition by incorrect key data, diodes should be inserted. An precision key can be recognized.

Fig13

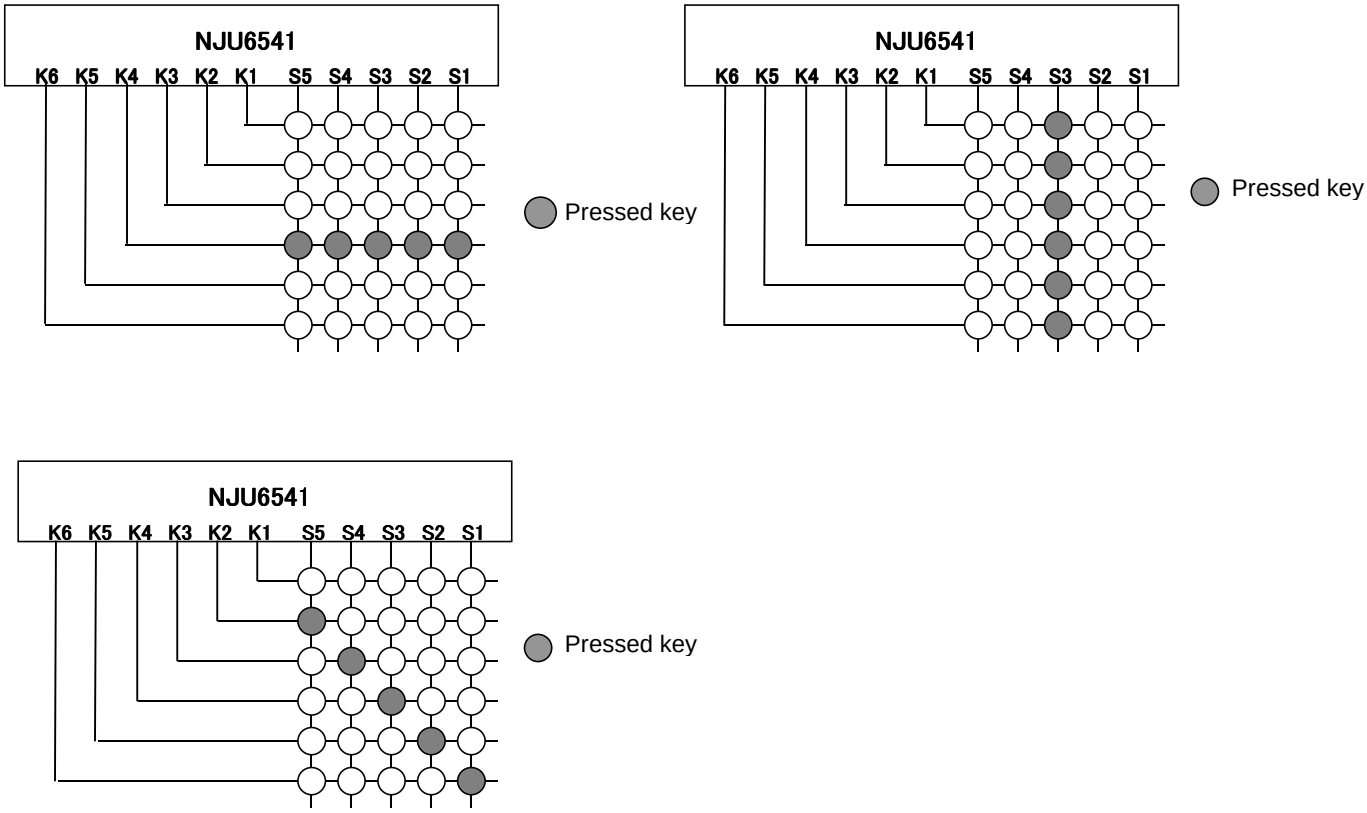


Fig14

12-7) Key scan OFF mode

Key scan operation is turned ON or OFF by the instruction. After the scanning ends, the key scanning is turned off. The request signal is output until reading out data even if the turn off command enters while scanning the key. The REQ signal outputs "L" if it reads out data. The REQ signal doesn't change into "H" until reading out data though the key scan stops when the REQ signal inputs the key scan on instruction by "L" after scan the key. The key register data can be reading in case of either case.

12-8) Key scan operates shown as follows

1, Key scan signal output terminals S1 – S5 output “L” signals when key scan does not operate, and output key scan signals after start of key scan operation. The conditions of key scan signal input terminals K1 – K6 are “H” state with internal pull-up resistances, though “L” signal comes in to K1 – K6 corresponding to the turned on keys.

2, The function of key scan starts twice operations when any key is turned on. It stops when a couple of data by continuously twice key scan operations are accorded and fixed as a correct key status. It operates more 2 times when the key status is not fixed and any keys are still turning on. It repeats again and again until key status is fixed. The correct key status data is stored and newly key scan operation does not start until external CPU reads data out after key status is fixed.

3, When the key status is fixed, REQ terminal outputs “L” signal as Key data read out request to the Master. should read key data out at detection of this “L” signal. The Key data read out request signal is released and REQ terminal outputs “H” signal after finish of the Master key data read out for newly key scan operation.

Key scan example

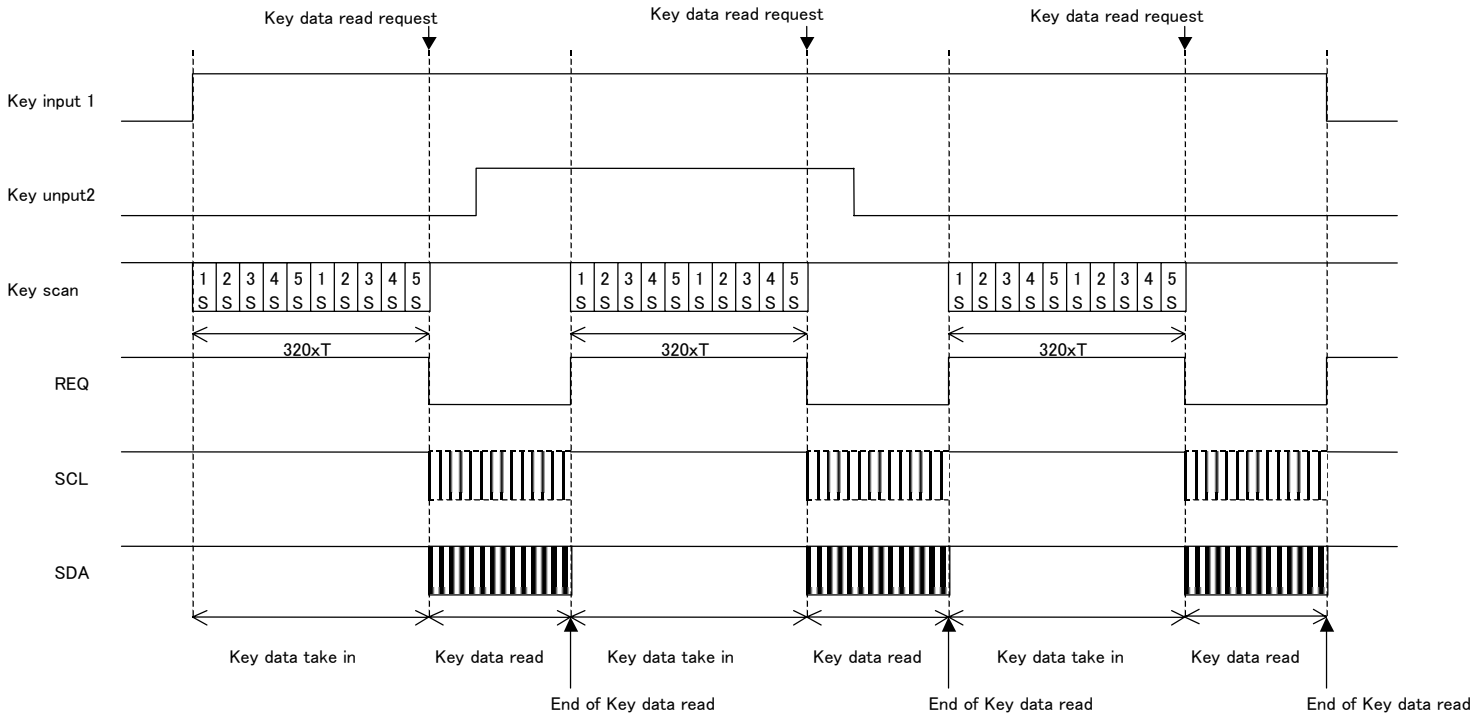


Fig15

13) General port output

The terminal SEG specified by command register 2 can be used as a general-purpose port. And, SEG1 ~ SEG4 terminals can be selected as segment driver output or general-purpose ports by instruction. The output setting of a general-purpose port sets the data of SEG1-SEG4 of COM1.Data is “1”=Output “H”, Data is “0”=Output “L”.

■ ABSOLUTE MAXIMAM RATINGS

(V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply Voltage 1	V_{DD}	-0.3 ~ +7.0	V	
Supply Voltage 2	V_0	-0.3 ~ +7.0	V	
Supply Voltage 3	V_1, V_2, V_3	-0.3 ~ V_0+0.3	V	
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V	INHb, CSb, SCL, SDA, RSTb, OSC applicable.
Operating Temp.	Topr	-40 ~ +105	°C	
Storage Temp.	Tstg	-55 ~ +125	°C	
Dissipation Power	P_D	1000	mW	The power dissipation is value mounted on glass epoxy board in size 76.2mm x 114.3mm x 1.6tmm

Note-1) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used within the range specified in the DC electrical characteristics, or the electrical stress may cause mulfunctions and impact on the reliability.

Note-2) All voltages are relative to V_{SS} = 0V reference.

Note-3) The following relationship shall be maintained.
$V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$, $V_0 \geq V_{DD}$, and V_0 shall be input after V_{DD}.

Note-4) To stabilize the LSI operation, place decoupling capacitors between V_{DD}-V_{SS} and between V_0-V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• DC characteristics 1

(V_{DD}=2.4 to 3.6V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply	V_{DD}		2.4	-	3.6	V	
LCD Driving Voltage	V_0	$V_0 \geq V_{DD}$	2.4	-	5.5	V	
LCD Bias Voltage	V_2	Ta=25°C Testing via COM/SEG terminals COM/SEG without load	2/3 V_1-0.2	2/3 V_1	2/3 V_1+0.2	V	
	V_3		1/3 V_1-0.2	1/3 V_1	1/3 V_1+0.2	V	
"H" Level Input Voltage1	V_{IH1}	CSb, RESb, OSC	0.8 V_{DD}	-	V_{DD}	V	
"L" Level Input Voltage1	V_{IL1}	CSb, RESb, OSC	0	-	0.2 V_{DD}	V	
"H" Level Input Voltage2	V_{IH2}	K1-K6	0.8 V_{DD}	-	V_{DD}	V	
"L" Level Input Voltage2	V_{IL2}	K1-K6	0	-	0.2 V_{DD}	V	
"H" Level Input Voltage3	V_{IH3}	SCL, SDA	0.7 V_{DD}	-	3.6	V	
"L" Level Input Voltage3	V_{IL3}	SCL, SDA	0(-0.5)	-	0.3 V_{DD}	V	
Hysteresis Voltage1	V_{H1}	CSb, RESb	-	0.2V_{DD}	-	V	
Hysteresis Voltage2	V_{H2}	SCL, SDA	0.05V_{DD}	-	-	V	
"H" Level Input Current	I_{IH}	V_{IN}= V_{DD} CSb, SCL, SDA, RESb	-	-	1.0	µA	
"L" Level Input Current	I_{IL}	V_{IN}= V_{SS} CSb, SCL, SDA, RESb	-	-	1.0	µA	
"H" Level Output Voltage1	V_{OH1}	V_{DD} =3V, I_O=5mA, P1 to P4	V_{DD}-0.6	-	-	V	
"L" Level Output Voltage1	V_{OL1}	V_{DD} =3V, I_O=5mA, P1 to P4	-	-	0.6	V	
"H" Level Output Voltage2	V_{OH2}	V_{DD} =3V, I_{OH}=-10uA, S1 to S5	0.8V_{DD}	-	V_{DD}	V	
"L" Level Output Voltage2	V_{OL2}	V_{DD} =3V, I_{OL2}=250uA, S1 to S5	V_{SS}	-	0.2 V_{DD}	V	
"L" Level Output Voltage3	V_{OL3}	V_{DD}=3V, REQ I_O=+3mA (open drain)	0	-	0.4	V	
"L" Level Output Voltage4	V_{OL4}	V_{DD}=3V, SDA I_O=+3mA (open drain)	0	-	0.4	V	
Driver-on Resistance (COM)	R_{COM}	±Id=1µA, V_{LCD}=3V/5.5V	-	-	10	kOhm	5
Driver-on Resistance (SEG)	R_{SEG}	±Id=1µA, V_{LCD}=3V/5.5V	-	-	10	kOhm	5
Pull up MOS current	I_P	V_{DD}=3V, V_{IN}=V_{ss}, K1-K6	-5	-15	-25	µA	
Oscillating Frequency	f_{OSC}	V_{DD} =3V, R_{OSC}=390kOhm, Cosc=120pF, Ta=25°C	12.6	15.4	18.2	kHz	
External Clock Frequency	f_{CP}	Input into OSC	12.6	15.4	18.2	kHz	6
External Clock Duty	duty	Input into OSC	40	50	60	%	
Bleeder Resistor	R_B	V_1-V_{SS} Ta=25°C	9	12	15	kOhm	
E.V.R	R_{EVR}	V0-V1 Ta=25°C E.V.R.=V0(1,1,1)	3	4	5	kOhm	
Operating Current	I_{DD1}	V_{DD} =3V, Display OFF, Key scan OFF, Ta=25°C	-	3	10	µA	
	I_{DD2}	V_{DD} =3V, Ta=25°C, Display ON Checker flag display, 1/3 bias Using external R & C, output open	-	15	30	µA	
	I_{LCD1}	V_{DD}=3V, V_0=5V, Display OFF Ta=25°C	-	-	1	µA	
	I_{LCD2}	V_{DD} =3V, V_0=5V, Ta=25°C, Display ON, Key scan ON Checker flag display, 1/3 bias output open, E.V.R.=(1,1,1)	-	320	450	µA	

Note-5) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_0, V_{SS}, V_1 , V_2 or V_3 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.

Note-6) The range of the oscillatory frequency is recommended. Please decide it noting flicker and the display quality when changing.

DC characteristics 2

(V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply	V_{DD}		4.5	-	5.5	V	
LCD Driving Voltage	V_0	$V_0 \geq V_{DD}$	4.5	-	5.5	V	
LCD Bias Voltage	V_2	Ta=25°C Testing via COM/SEG terminals COM/SEG without load	2/3 V_1-0.2	2/3 V_1	2/3 V_1+0.2	V	
	V_3		1/3 V_1-0.2	1/3 V_1	1/3 V_1+0.2	V	
"H" Level Input Voltage1	V_{IH1}	RESb, OSC	0.8 V_{DD}	-	V_{DD}	V	
"L" Level Input Voltage1	V_{IL1}	RESb, OSC	0	-	0.2 V_{DD}	V	
"H" Level Input Voltage3	V_{IH3}	SCL, SDA (Open drain)	0.7 V_{DD}	-	5.5	V	
"L" Level Input Voltage3	V_{IL3}	SCL, SDA (Open drain)	0(-0.5)	-	0.3 V_{DD}	V	
Hysteresis Voltage1	V_{H1}	RESb	-	0.2V_{DD}	-	V	
Hysteresis Voltage2	V_{H2}	SCL, SDA	0.05V_{DD}	-	-	V	
"H" Level Input Current	I_{IH}	V_{IN}= V_{DD} CSb, SCL, SDA, RESb	-	-	1.0	μA	
"L" Level Input Current	I_{IL}	V_{IN}= V_{SS} CSb, SCL, SDA, RESb	-	-	1.0	μA	
"H" Level Output Voltage1	V_{OH1}	V_{DD} =5V, I_O=-10mA, P1 to P4	V_{DD}-1.0	-	-	V	
"L" Level Output Voltage1	V_{OL1}	V_{DD} =5V, I_O=+10mA, P1 to P4	-	-	1.0	V	
"H" Level Output Voltage2	V_{OH2}	V_{DD} =5V, I_{OH}=-20uA, S1 to S5	0.8V_{DD}		V_{DD}	V	
"L" Level Output Voltage2	V_{OL2}	V_{DD} =5V, I_O=+500uA, P1 to P4	V_{SS}		0.2 V_{DD}	V	
"L" Level Output Voltage3	V_{OL3}	V_{DD} =5V , REQ I_O=+3mA (open drain)	0		0.4	V	
"L" Level Output Voltage4	V_{OL4}	V_{DD} =5V , SDA I_O=-3mA (open drain)	0		0.4	V	
Driver-on Resistance (COM)	R_{COM}	±Id=1μA, V_{LCD}=4.5V/5.5V	-	-	10	kOhm	7
Driver-on Resistance (SEG)	R_{SEG}	±Id=1μA, V_{LCD}=4.5V/5.5V	-	-	10	kOhm	7
Pull up MOS Current	I_P	V_{DD} =5V, V_{IN}=V_{SS}, K1-K6	-10	-25	-65	μA	
Oscillating Frequency	f_{OSC}	V_{DD} =5V, R_{OSC}=390kOhm, Cosc=120pF, Ta=25°C	12.6	15.4	18.2	kHz	
External Clock Frequency	f_{CP}	Input into OSC	12.6	15.4	18.2	kHz	8
External Clock Duty	duty	Input into OSC	40	50	60	%	
Bleeder Resistor	R_B	V_1-V_{SS} Ta=25°C	9	12	15	kOhm	
E.V.R	R_{EVR}	V0-V1 Ta=25°C E.V.R.=V0(1,1,1)	3	4	5	kOhm	
Operating Current	I_{DD1}	V_{DD} =5V, Display off Ta=25°C, Key scan off	-	5	12.5	μA	
	I_{DD2}	V_{DD} =5V, Ta=25°C, Display ON Checker flag display, 1/3 bias Using external R & C, Output open	-	30	60	μA	
	I_{LCD1}	V_{DD}=5V, V_0=5V, Display off Ta=25°C	-	-	1	μA	
	I_{LCD2}	V_{DD} =5V, V_0=5V, Ta=25°C, Checker flag display, 1/3 bias Output open, E.V.R.=(1,1,1)	-	320	450	μA	

Note-7) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_0, V_{SS}, V_1 , V_2 or V_3 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.

Note-8) The range of the oscillatory frequency is recommended. Please decide it noting flicker and the display quality when changing.

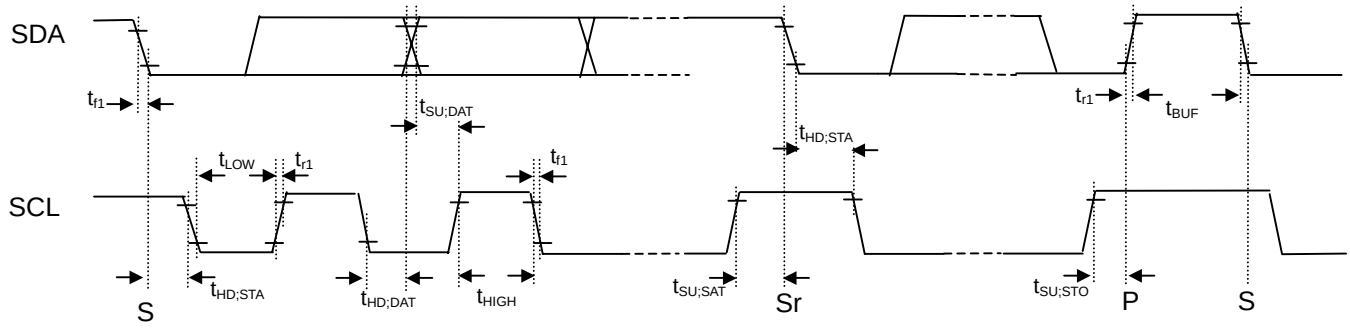
AC characteristics

V_{DD}=2.4V to 5.5V, Ta=-40 to 105°C

Item	記号	条 件	MIN	TYP	MAX	UNIT
SCL Click frequency	f_{SCL}	SCL	-	-	400	kHz
Hold Time (repetition) [Start] condition	$t_{HD;STA}$	SCL, SDA	0.6	-	-	us
SCL Clock “L” time	t_{LOW}	SCL	1.3	-	-	us
SCL Clock “H” time	t_{HIGH}	SCL	0.6	-	-	us
Repetition[Start] condition Set up time	$t_{SU;STA}$	SCL, SDA	0.6	-	-	us
Data hold time	$t_{HD;DAT}$	SCL, SDA	0	-	0.9	us
Data set up time	$t_{SU;DAT}$	SCL, SDA	100	-	-	ns
Rising time1	t_{r1}	SCL, SDA	-	-	300	ns
Rising time2	t_{r2}	EN, RSTb, OSC	-	-	300	ns
Falling time1	t_{f1}	SCL, SDA	-	-	300	ns
Falling time2	t_{f2}	EN, RSTb, OSC	-	-	300	ns
[Stop] condition Set up time	$t_{SU;STO}$	SCL, SDA	0.6	-	-	us
[Stop] [Start] Bus free time	t_{BUF}	SDA	1.3	-	-	us

The I^2C-bus timing of NJU6541A conforms to a F/S mode.

I^2C bus timing

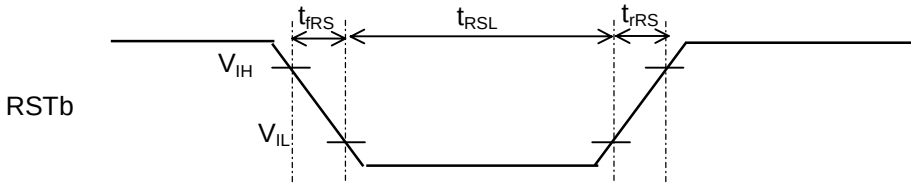


S: Start condotion
Sr: Repeat start condition
P: Stop condition

- Input condition when hardware reset circuit is used

(Ta=25°C)

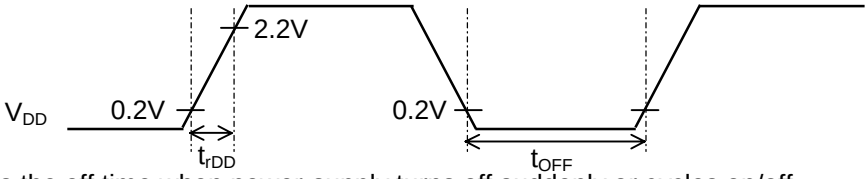
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reset Input “L” Level Width	t_{RSL}	f_{OSC}= 15.4kHz	1.5			ms
Reset Rising Time	t_{rRS}				100	ns
Reset Falling Time	t_{fRS}				100	ns



- Power supply condition when hardware reset circuit is used

(Ta=-40 to 105°C(T.B.D))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power-on Rising Time	t_{rDD}		0.1		5	ms
Power-off Time	t_{OFF}		1			ms

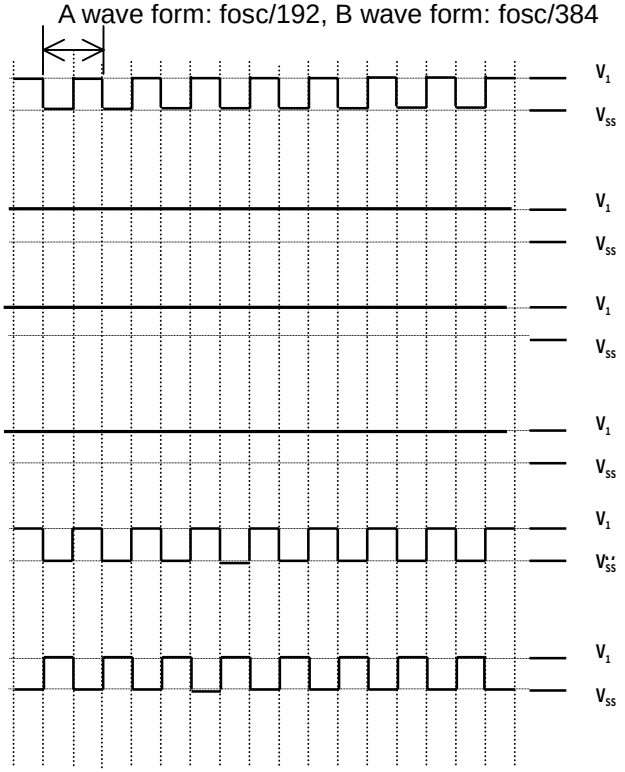


Note 10) t_{OFF} is the off time when power-supply turns off suddenly or cycles on/off.

■ LCD DRIVING WAVEFORM

1/1duty, 1/1bias, (A/B wave form)

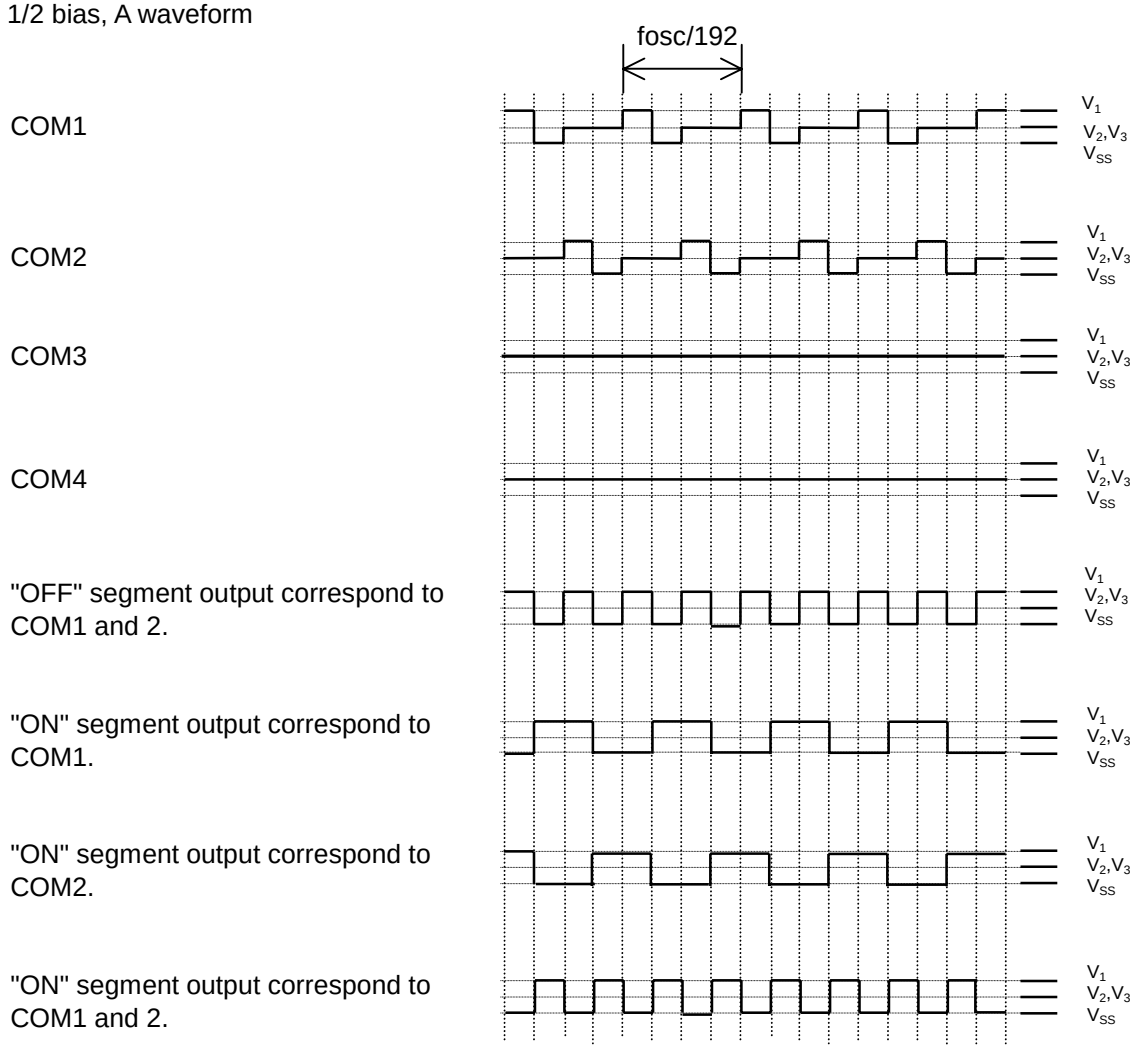
A wave form: fosc/192, B wave form: fosc/384



Note) COM2-COM4 must open when 1/1duty is selected.

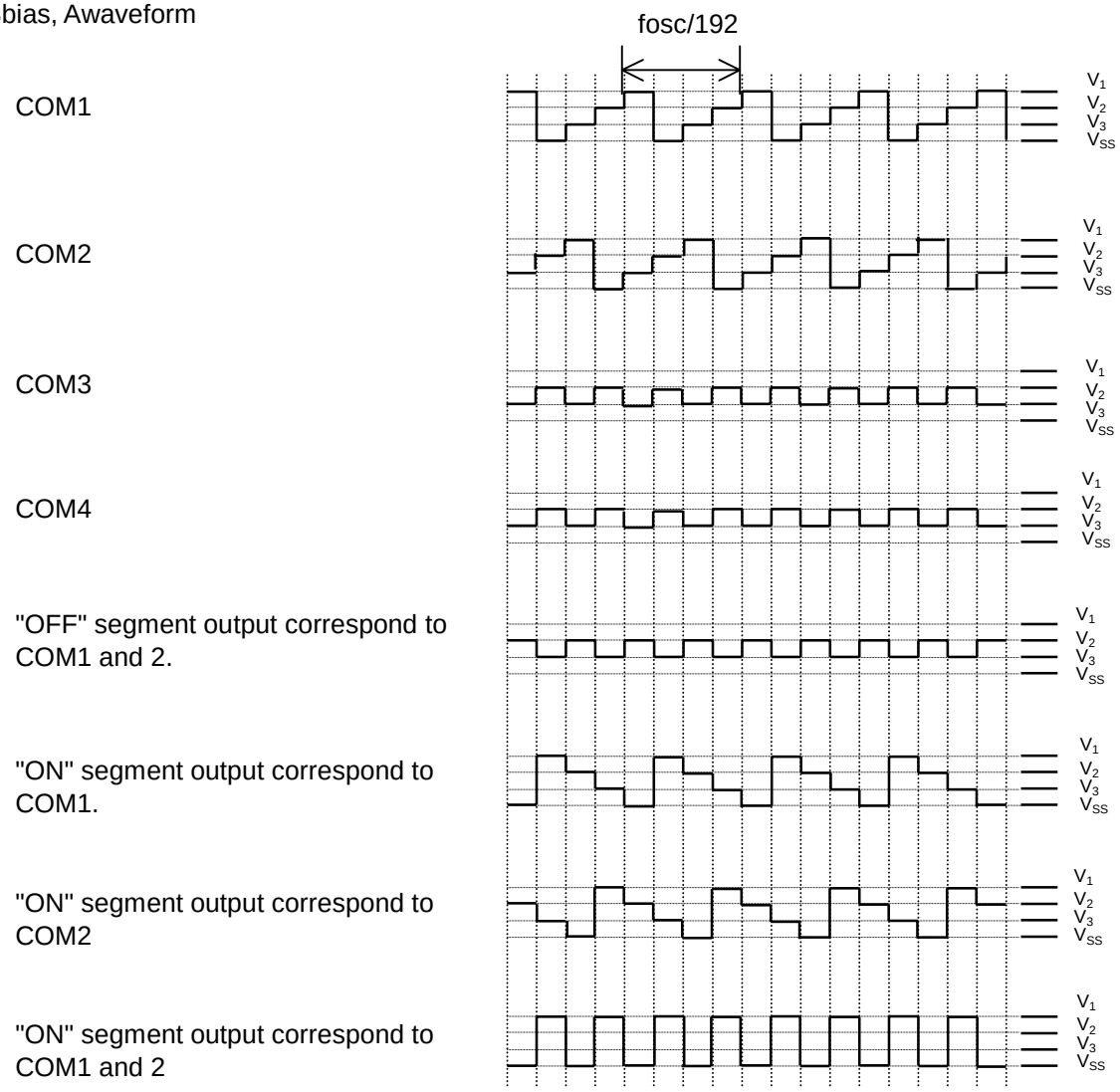
1/1duty, 1/1bias

1/2 duty, 1/2 bias, A waveform



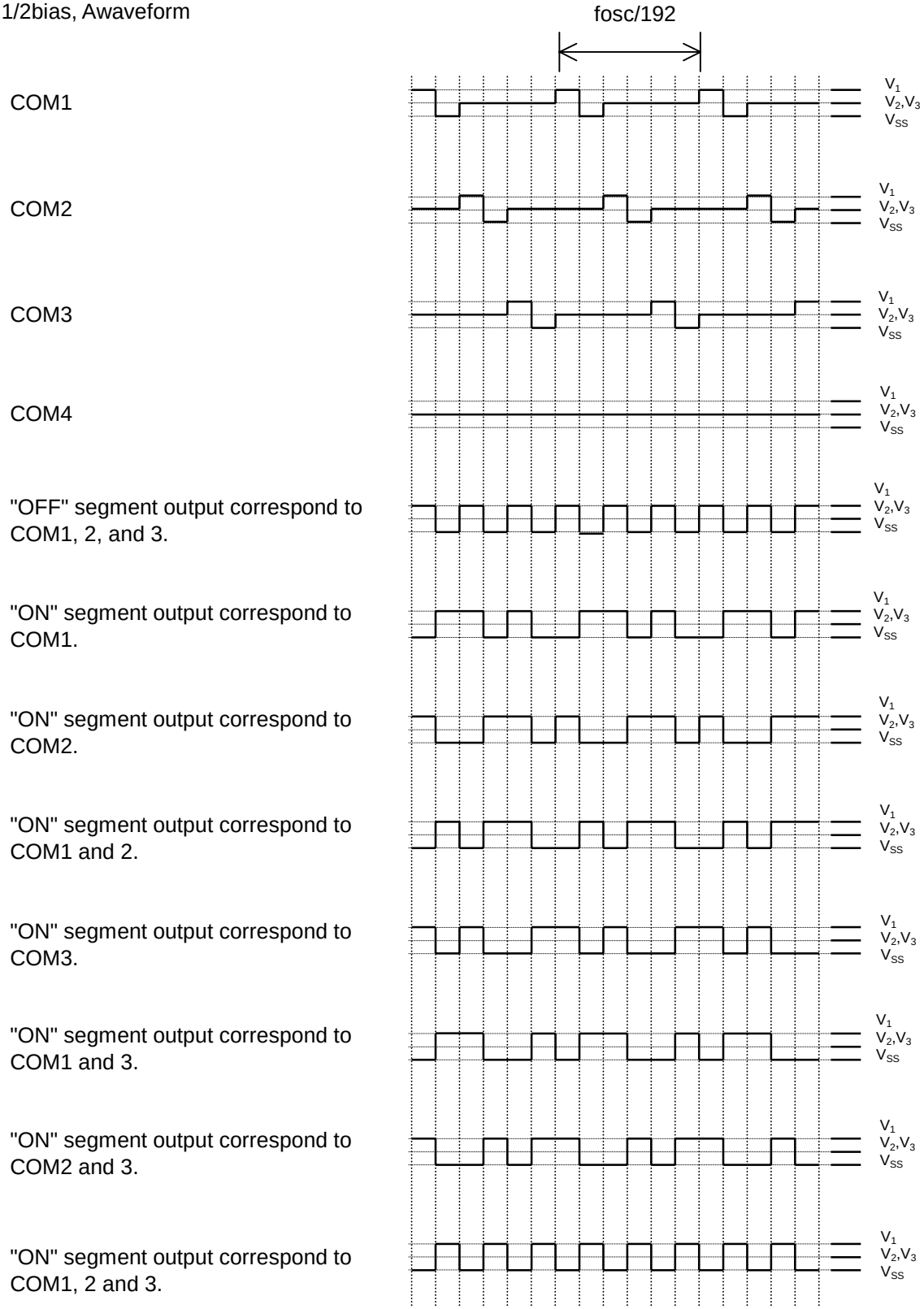
1/2duty, 1/2bias

1/2duty, 1/3bias, Awaveform



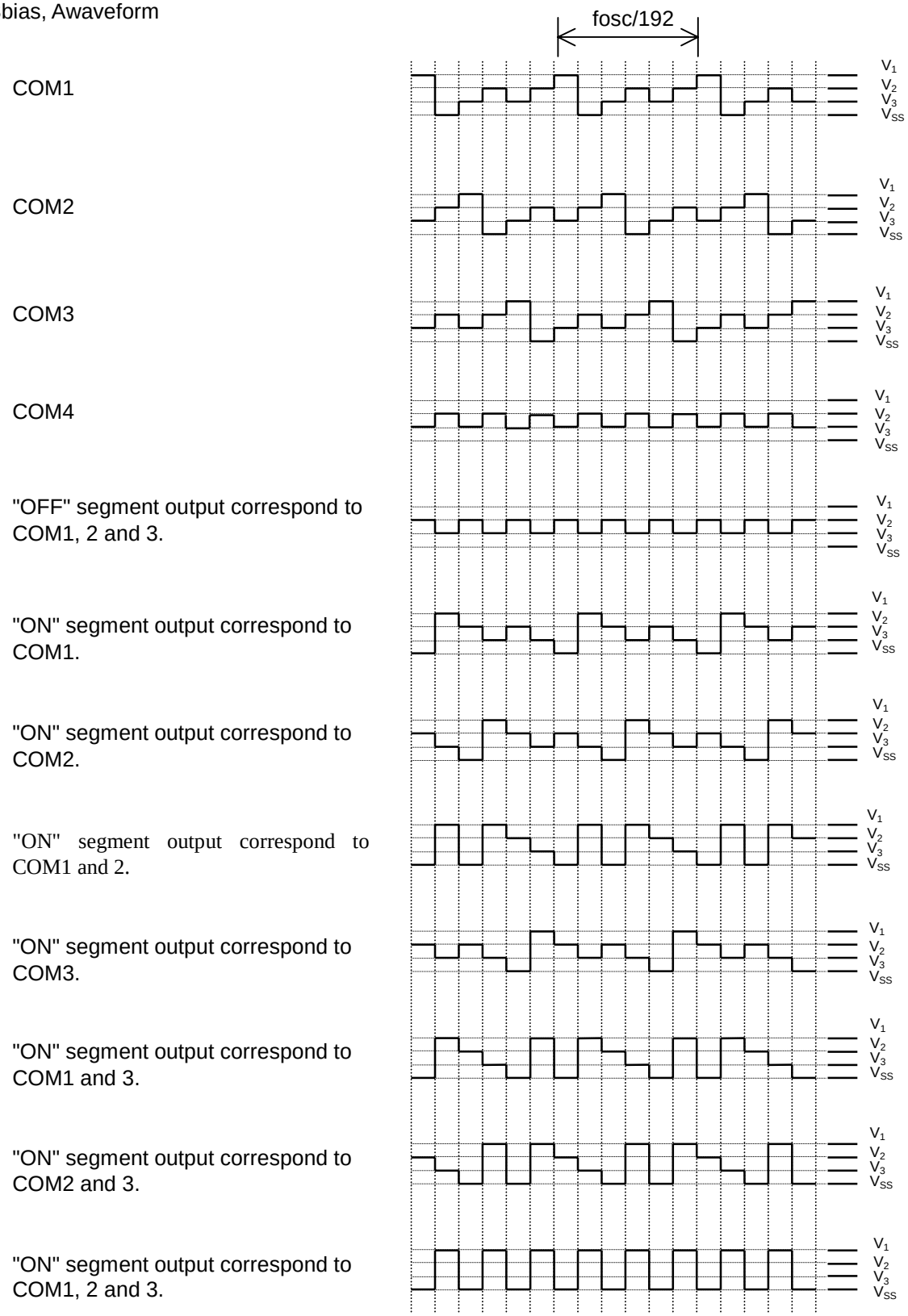
1/2duty, 1/3bias

1/3duty, 1/2bias, Awaveform



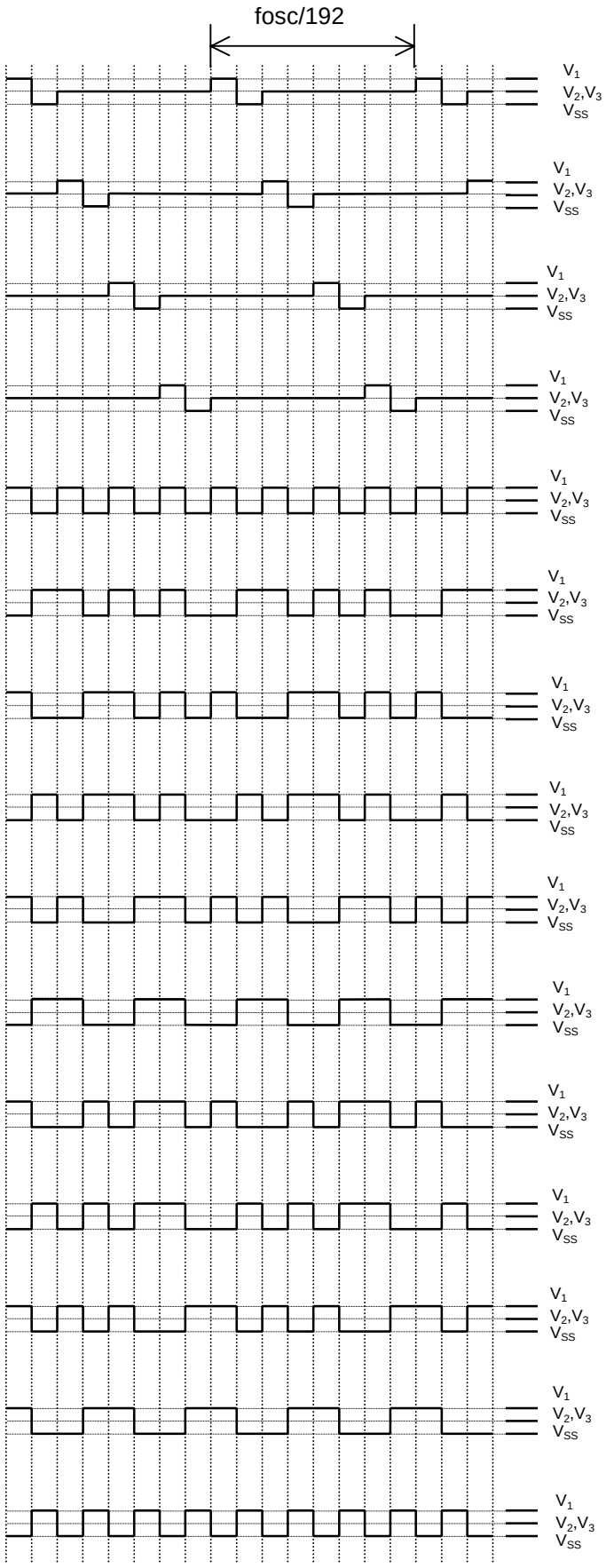
1/3duty, 1/2bias

1/3duty, 1/3bias, Awaveform



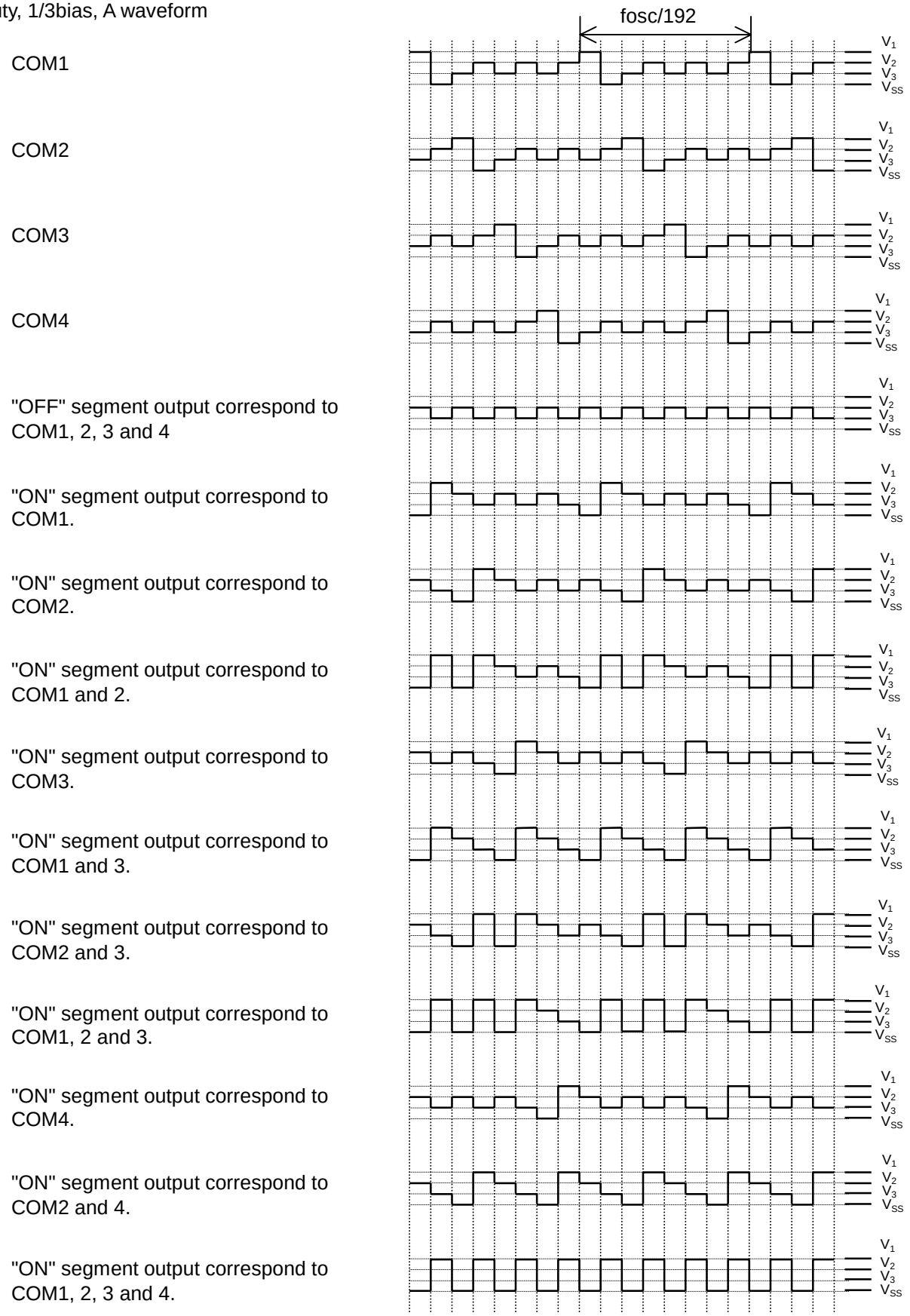
1/3duty, 1/3bias

1/4duty, 1/2bias, A waveform



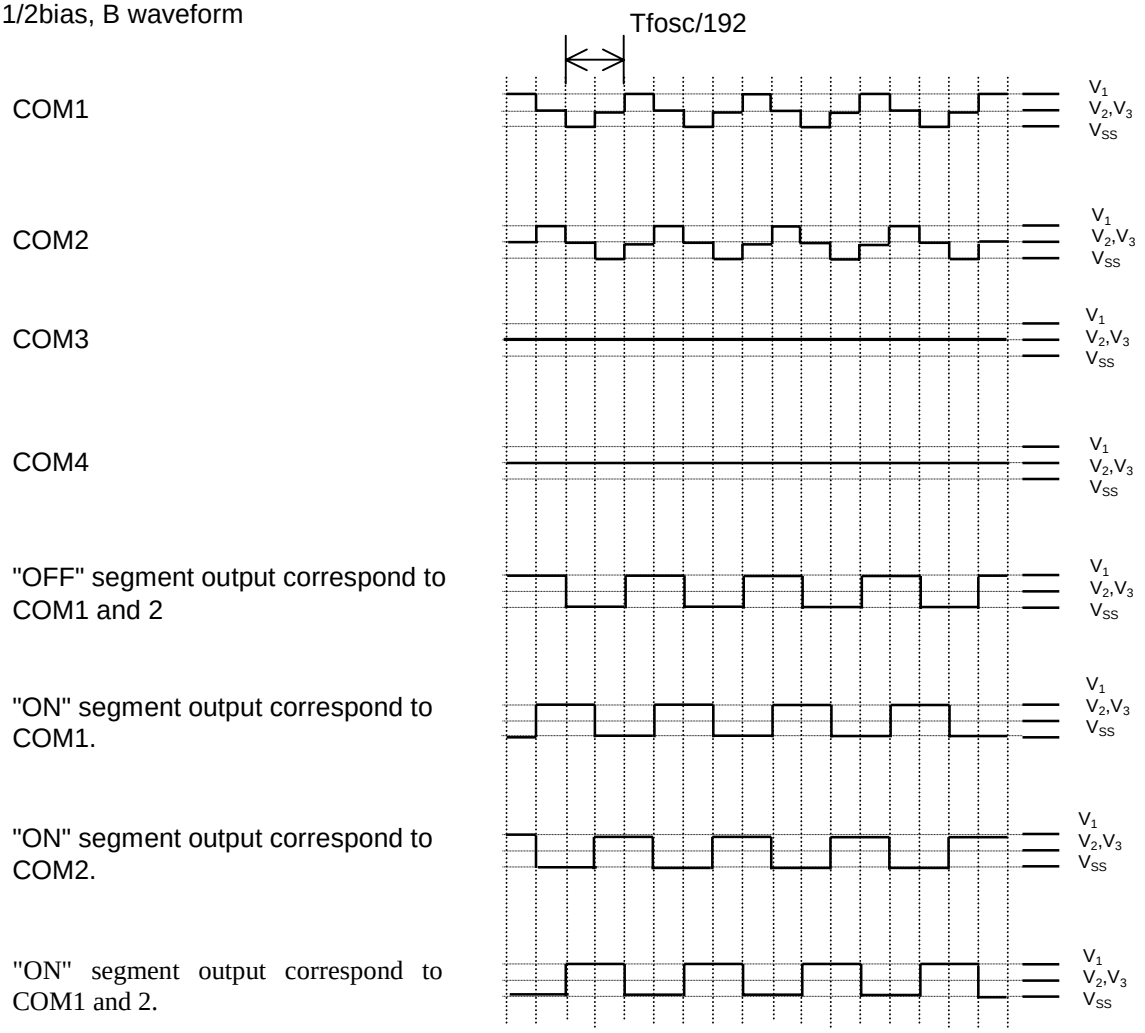
1/4duty, 1/2bias

1/4duty, 1/3bias, A waveform



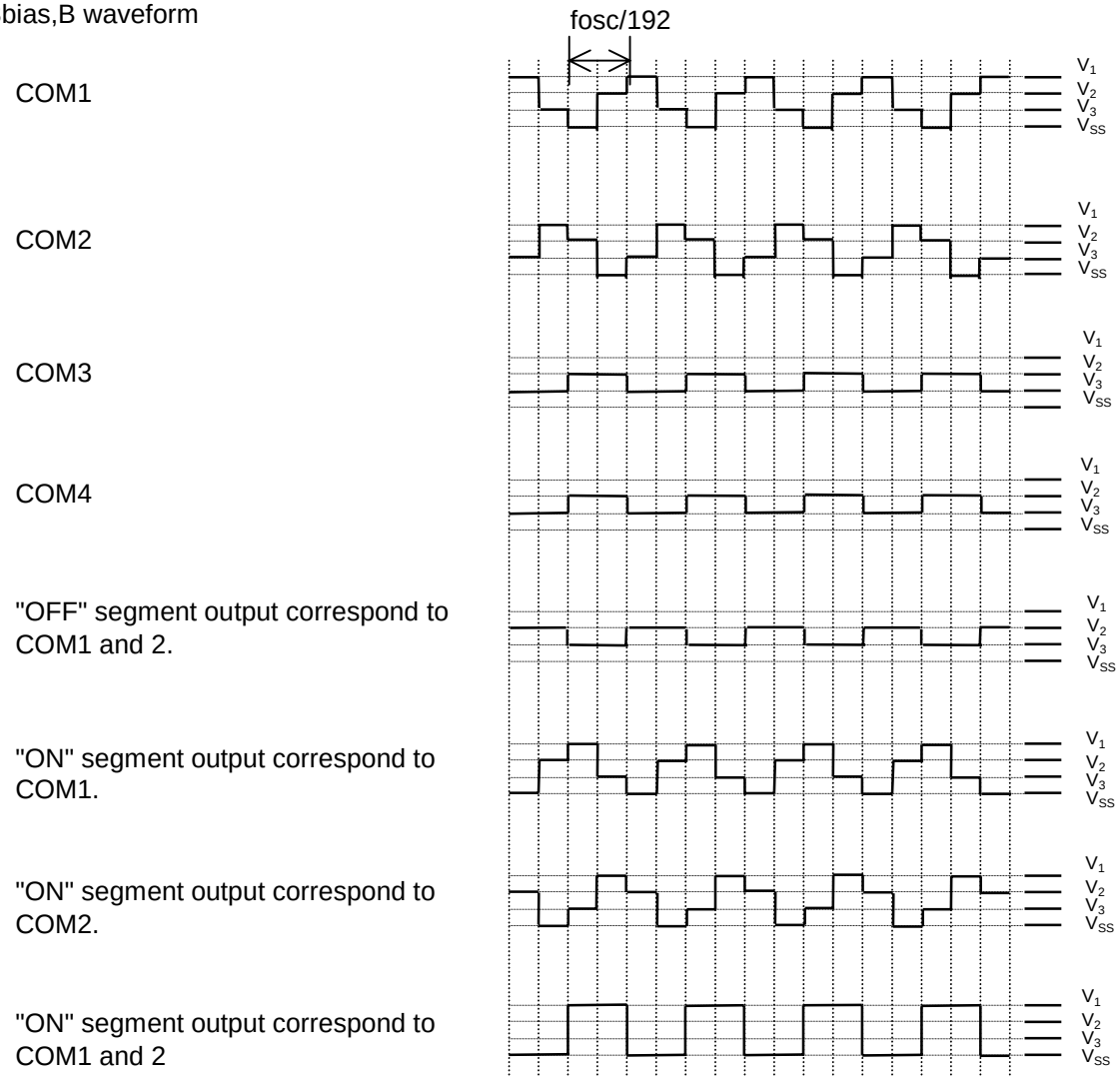
1/4duty, 1/3bias

1/2duty, 1/2bias, B waveform



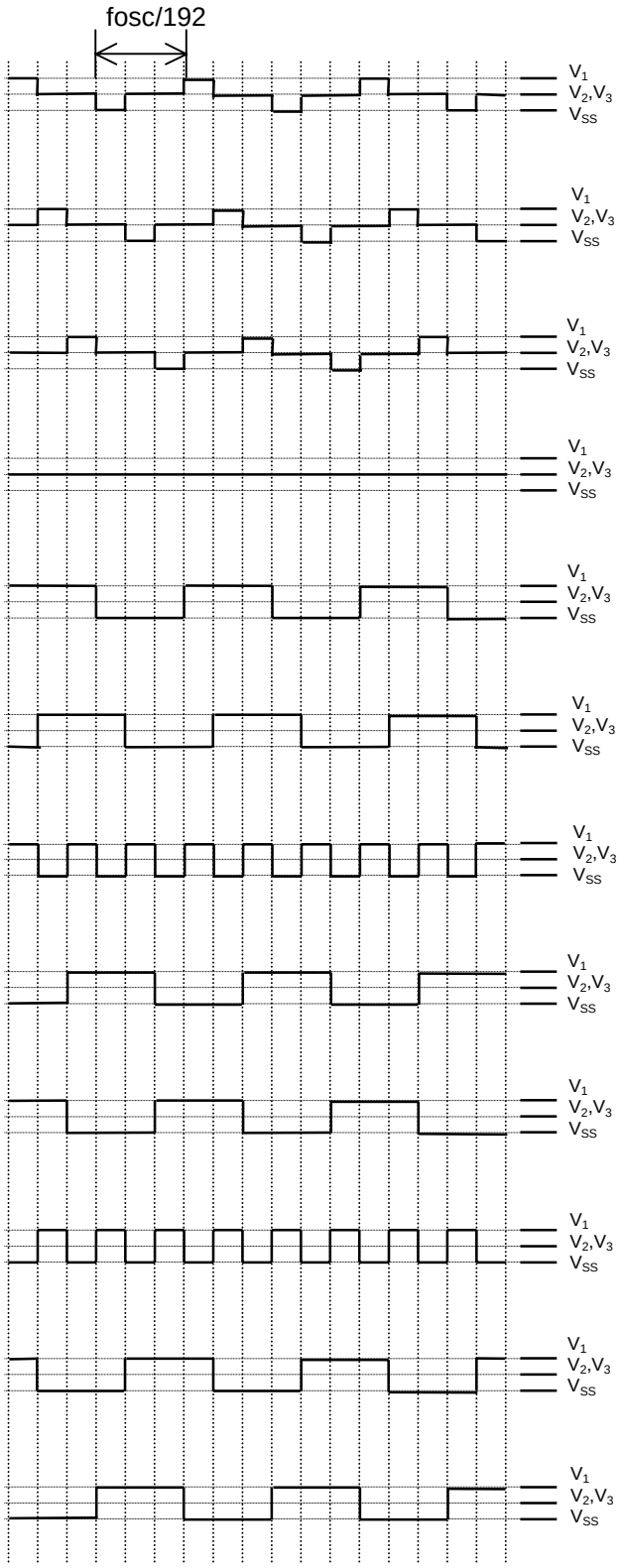
1/2duty, 1/2bias

1/2duty, 1/3bias,B waveform



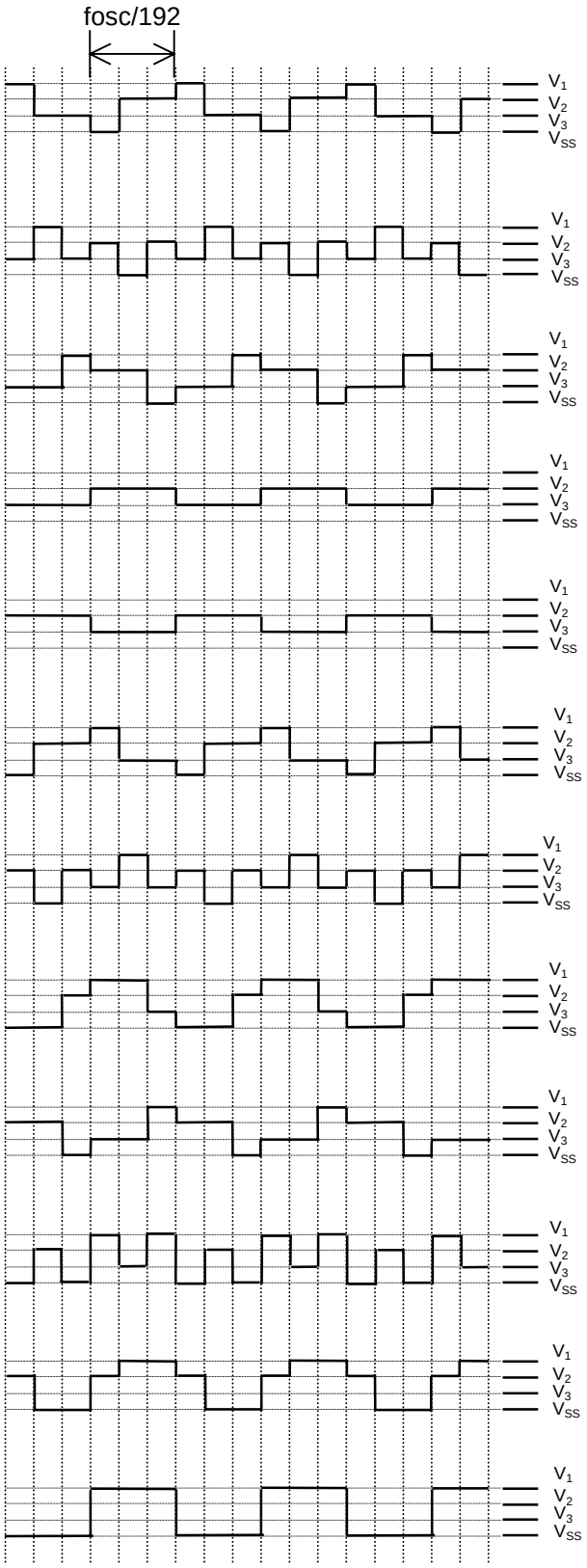
1/2duty, 1/3bias

1/3duty, 1/2bias, B waveform



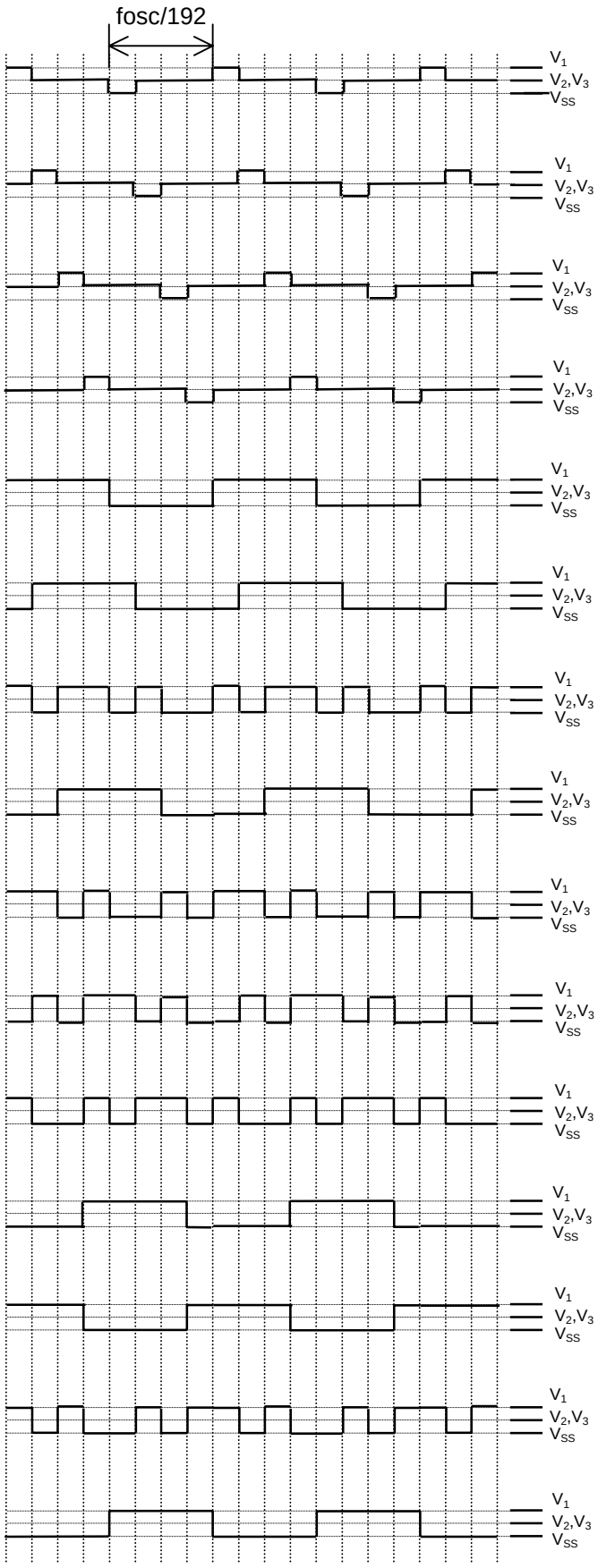
1/3duty, 1/2bias

1/3duty, 1/3bias, B waveform



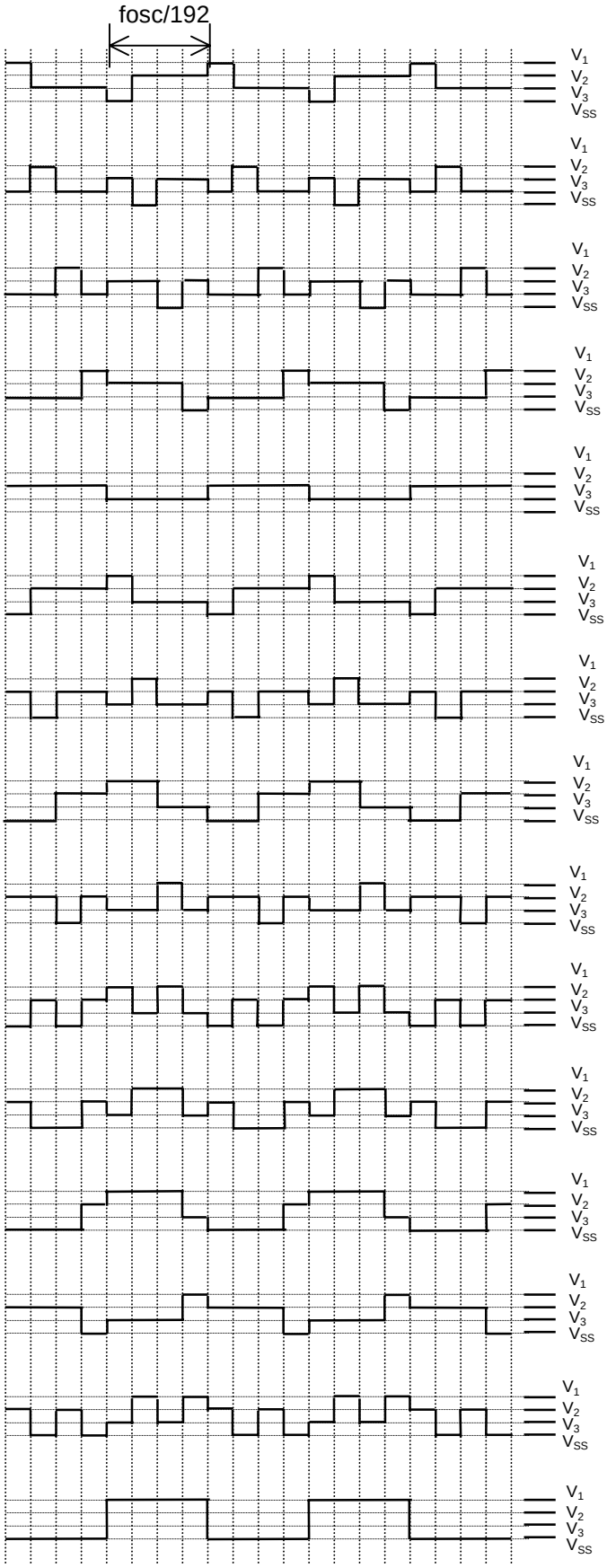
1/3duty, 1/3bias

1/4duty, 1/2bias, B waveform



1/4duty, 1/2bias

1/4duty, 1/3bias, B waveform



"OFF" segment output correspond to COM1, 2, 3 and 4.

"ON" segment output correspond to COM1.

"ON" segment output correspond to COM2.

"ON" segment output correspond to COM1 and 2.

"ON" segment output correspond to COM3.

"ON" segment output correspond to COM1 and 3.

"ON" segment output correspond to COM2 and 3.

"ON" segment output correspond to COM1, 2 and 3.

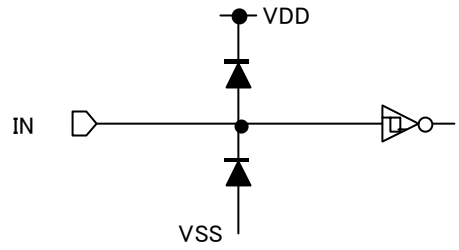
"ON" segment output correspond to COM4.

"ON" segment output correspond to COM2 and 4.

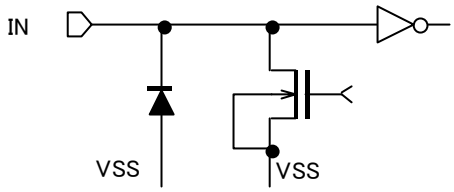
"ON" segment output correspond to COM1, 2, 3 and 4.

1/4duty, 1/3bias

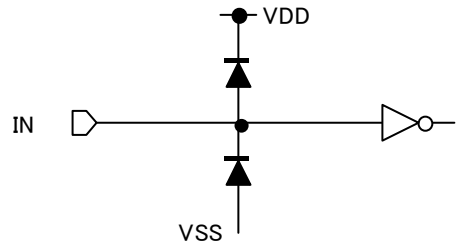
INPUT and OUTPUT Curcuit



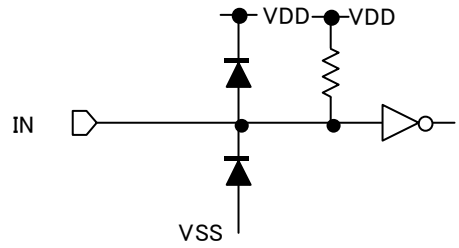
RSTb, TEST, CSb,



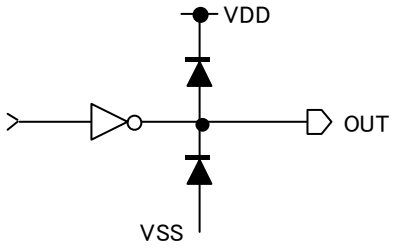
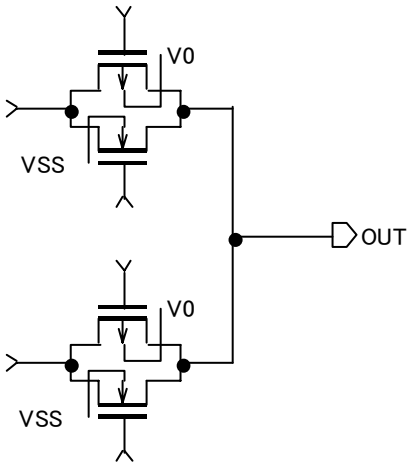
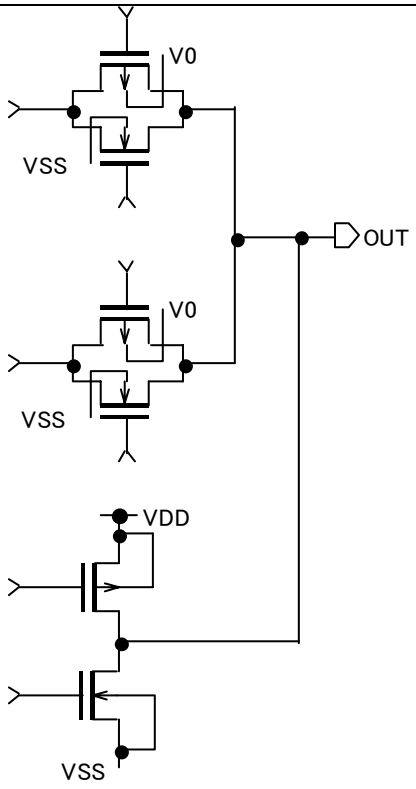
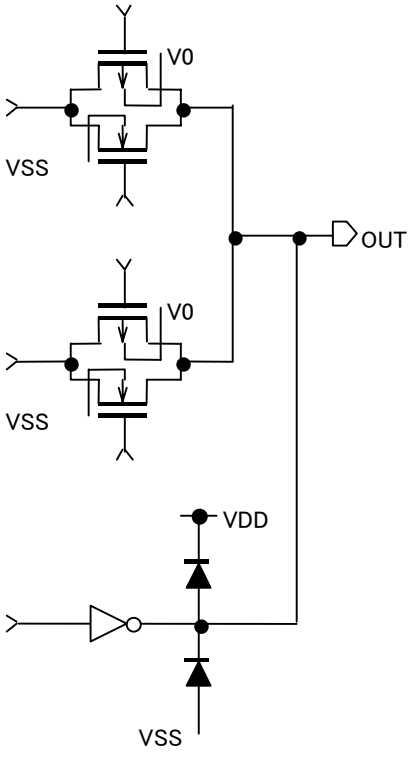
SDA、SCL、REQ



OSC

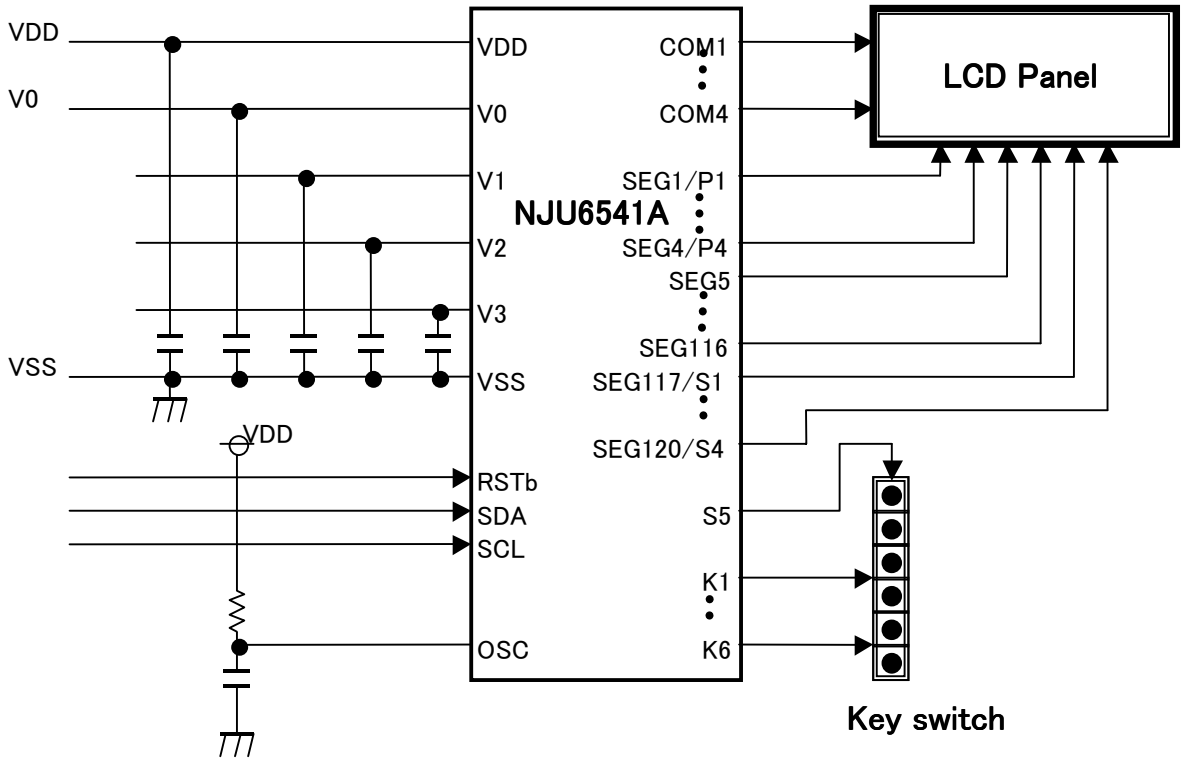


K1~K6

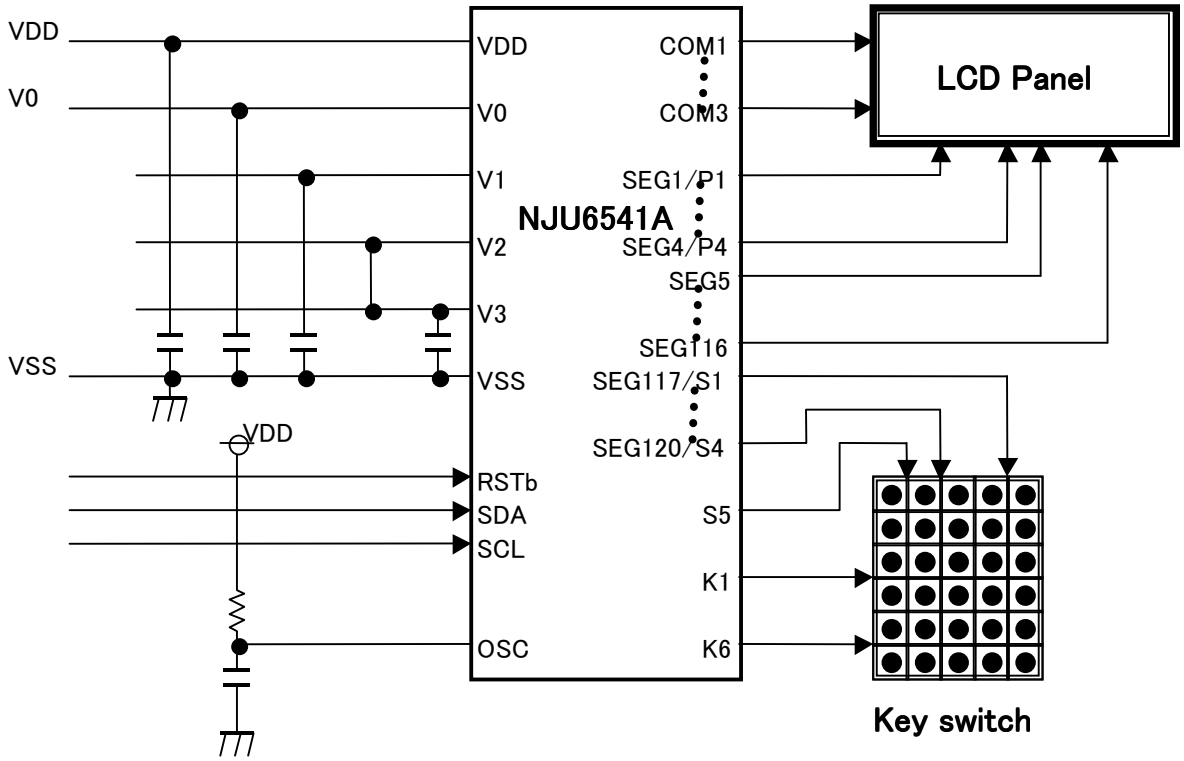
	
S5	SEG5~SEG116, COM1~COM4
	
SEG1/P1~SEG4/P4	SEG117/S1~SEG120/S4

■ APPLICATION CIRCUIT

• 1/4duty, 1/3bias SEG1~SEG120



• 1/3duty, 1/2bias 30Key



1/1duty, 1/1bias, 30Key, P1~P4port

(a)