



STP5NK52ZD - STB5NK52ZD-1 STD5NK52ZD - STD5NK52ZD-1

N-channel 520V - 1.22Ω - 4.4A - TO-220 - DPAK - I²PAK - IPAK
Zener-protected SuperMESH™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STB5NK52ZD-1	520V	<1.5Ω	4.4A	70W
STD5NK52ZD	520V	<1.5Ω	4.4A	70W
STD5NK52ZD-1	520V	<1.5Ω	4.4A	70W
STP5NK52ZD	520V	<1.5Ω	4.4A	70W

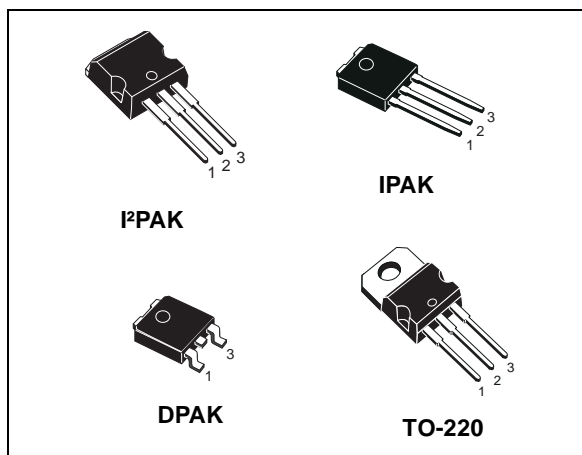
- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Improved ESD capability

Description

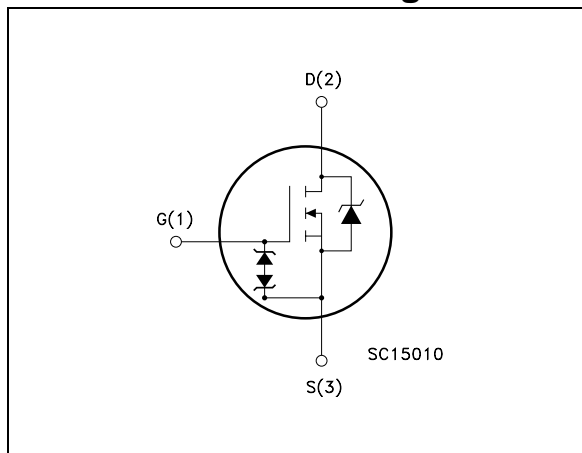
The SuperFREDMesh™ series associates all advantages of reduced on-resistance, zener gate protection and very high dv/dt capability with a Fast body-drain recovery diode. Such series complements the “FDmesh™” advanced technology.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB5NK52ZD-1	B5NK52ZD	I ² PAK	Tube
STD5NK52ZD	D5NK52ZD	DPAK	Tape & reel
STD5NK52ZD-1	D5NK52ZD	IPAK	Tube
STP5NK52ZD	P5NK52ZD	TO-220	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	9
4	Package mechanical data	10
5	Package mechanical data	15
6	Revision history	16

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	520	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	520	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4.4	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	17.6	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	70	W
	Derating factor	0.56	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	2800	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 4.4\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal data

		TO-220/I ² PAK	DPAK/IPAK	
Rthj-case	Thermal resistance junction-case Max	1.78		$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-ambient Max	62.5	100	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^\circ\text{C}$

Table 3. Avalanche Characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4.4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	170	mJ

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1mA, V _{GS} = 0	520			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C =125°C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20V			± 10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50μA	2.5	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 2.2A		1.22	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward transconductance	V _{DS} = 15V, I _D = 2.2A		3.1		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		529 71 13.4		pF pF pF
C _{OSS eq} (1)	Equivalent output capacitance	V _{GS} = 0V, V _{DS} = 0 to 416V		11		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 416V, I _D = 4.4A, V _{GS} = 10V (see Figure 16)		16.9 4.2 8.4		nC nC nC

1. C_{OSS eq} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260V, I_D = 2.2A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 15)		11.4		ns
t_r	Rise time			13.6		ns
$t_{d(off)}$	Turn-off-delay time				23.1	ns
t_f	Fall time				15	ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				4.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				17.6	A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 4.4A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4.4A, di/dt = 100A/\mu s$ $V_{DD} = 60V, T_j = 25^\circ C$ (see Figure 20)		97.7		ns
Q_{rr}	Reverse Recovery Charge			300		nC
I_{RRM}	Reverse Recovery Current			5.9		A
t_{rr}	Reverse Recovery Time	$I_{SD} = 4.4A, di/dt = 100A/\mu s$ $V_{DD} = 60V, T_j = 150^\circ C$ (see Figure 20)		139		ns
Q_{rr}	Reverse Recovery Charge			500		nC
I_{RRM}	Reverse Recovery Current			7.2		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 1mA$ (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220 / I²PAK / D²PAK

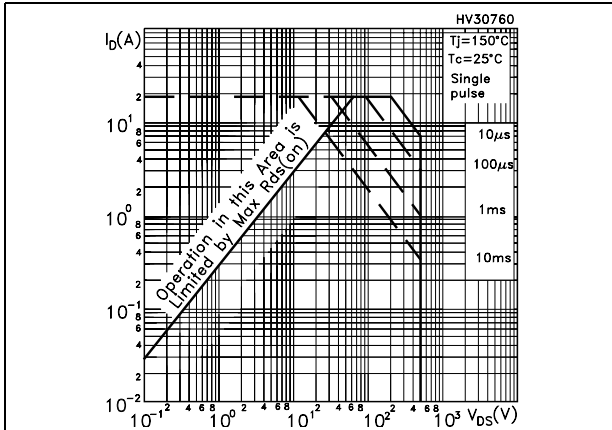


Figure 2. Thermal impedance for TO-220 / I²PAK / D²PAK

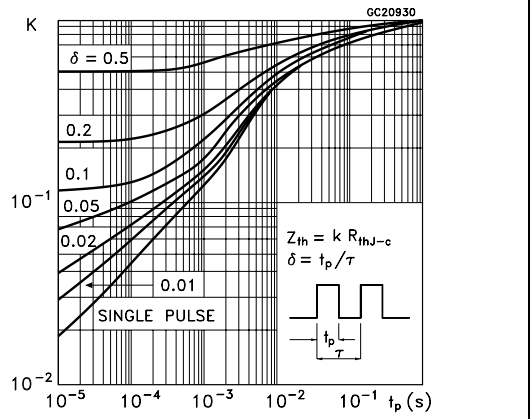


Figure 3. Safe operating area for DPAK / IPAK

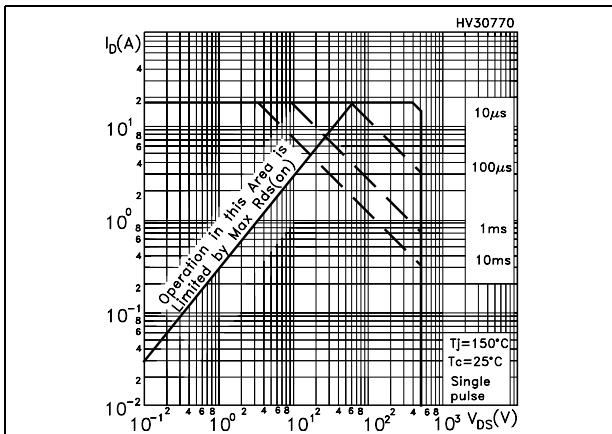


Figure 4. Thermal impedance for DPAK / IPAK

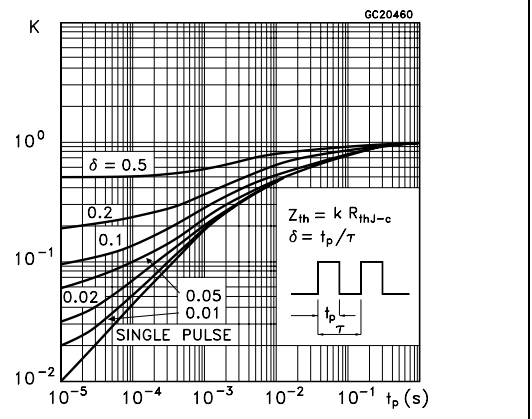


Figure 5. Output characteristics

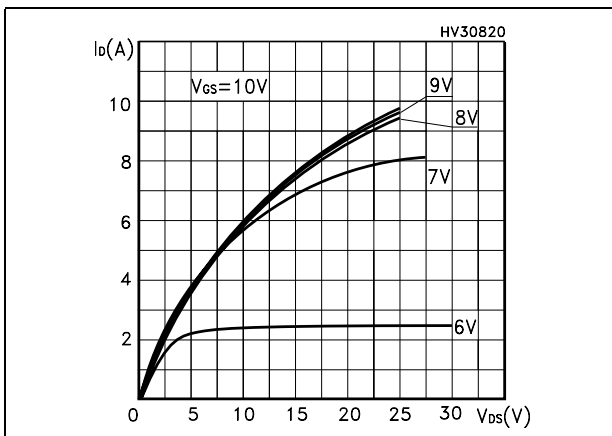


Figure 6. Transfer characteristics

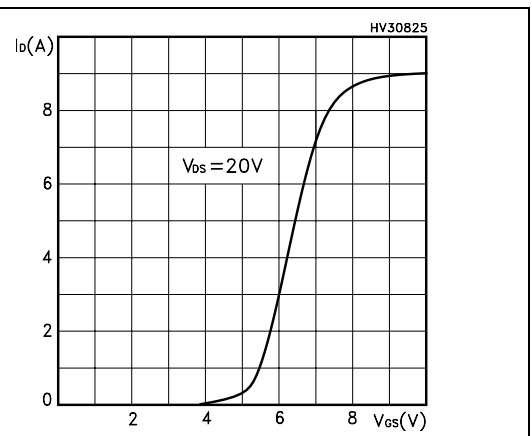


Figure 7. Normalized $B_{V_{DS}}$ vs temperature

Figure 8. Static drain-source on resistance

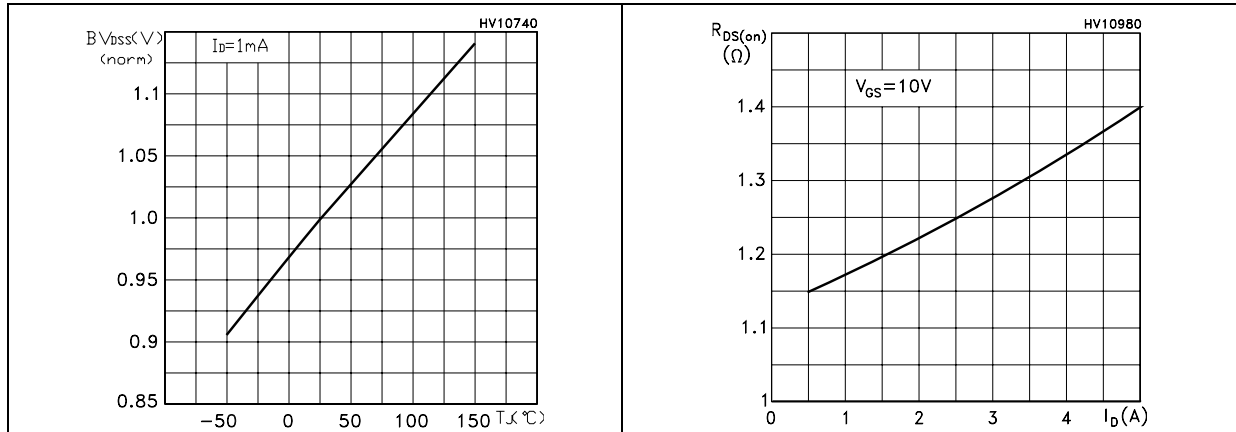


Figure 9. Gate charge vs gate-source voltage

Figure 10. Capacitance variations

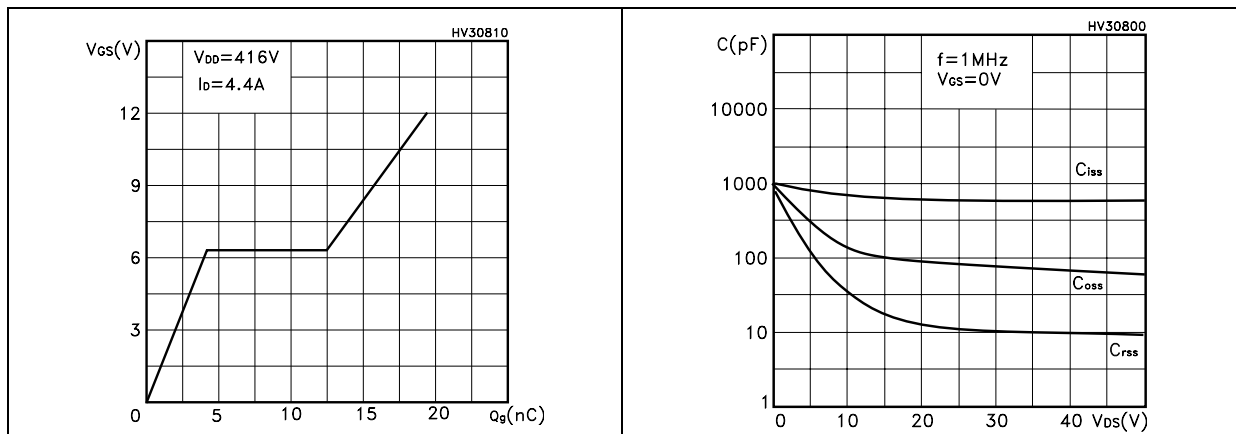


Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on resistance vs temperature

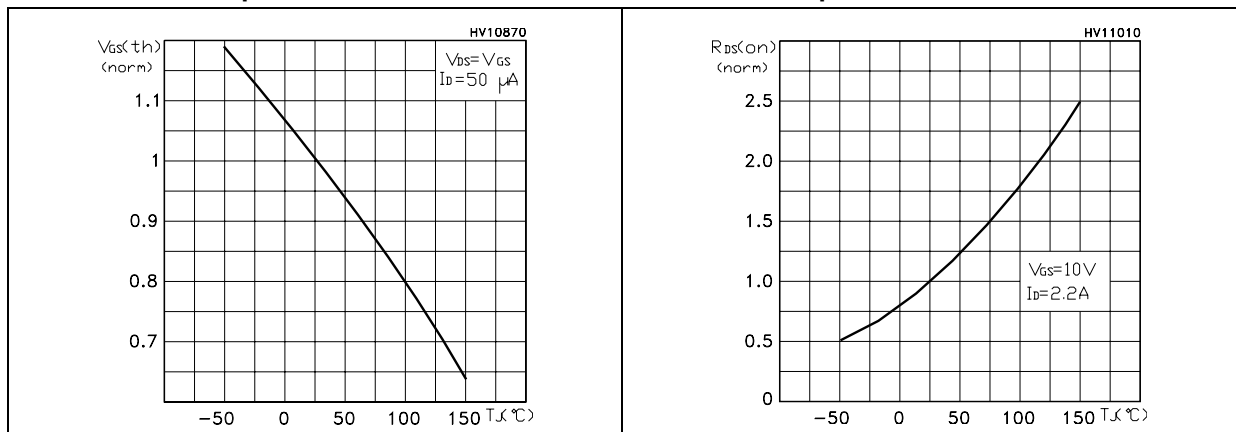


Figure 13. Source-drain diode forward characteristics

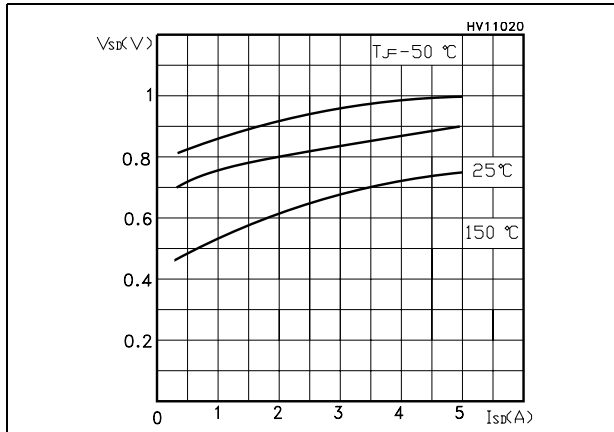
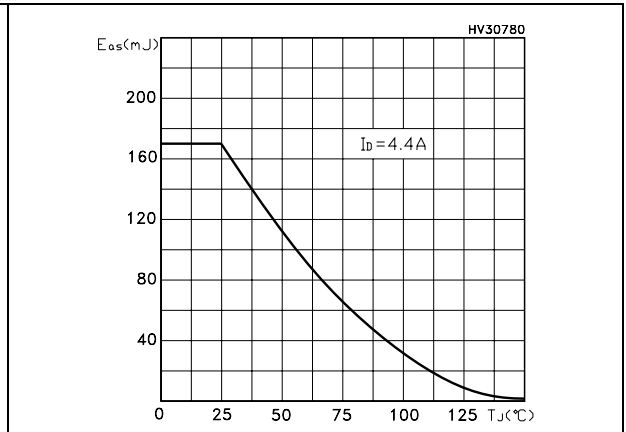


Figure 14. Maximum avalanche energy vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load

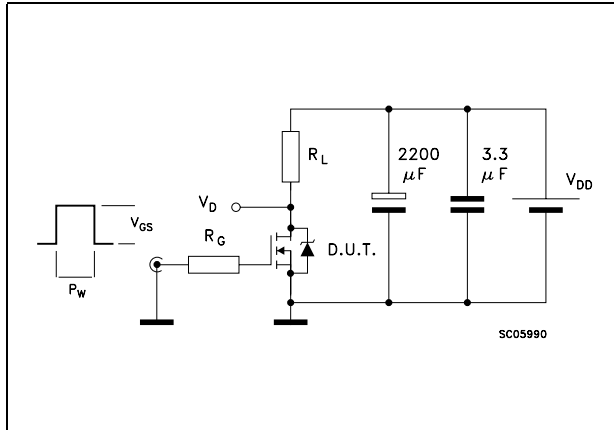


Figure 16. Gate charge test circuit

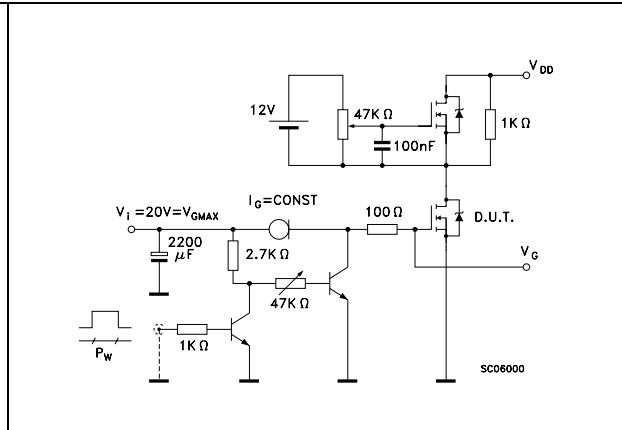


Figure 17. Test circuit for inductive load switching and diode recovery times

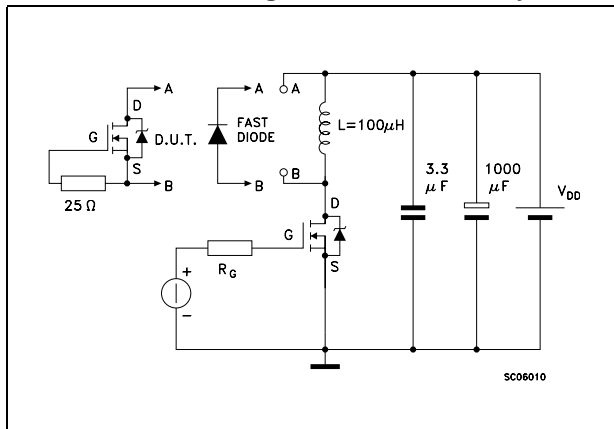


Figure 18. Unclamped Inductive load test circuit

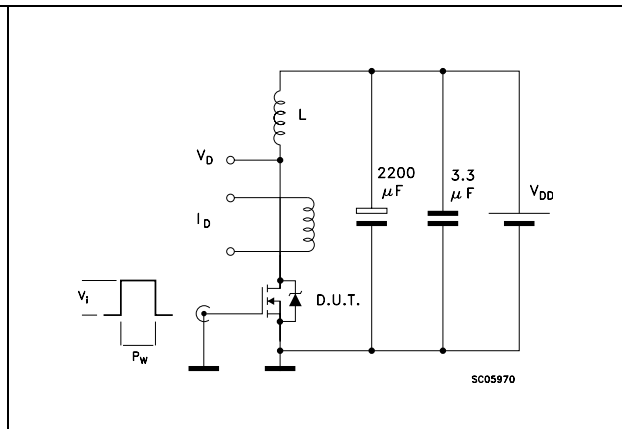


Figure 19. Unclamped inductive waveform

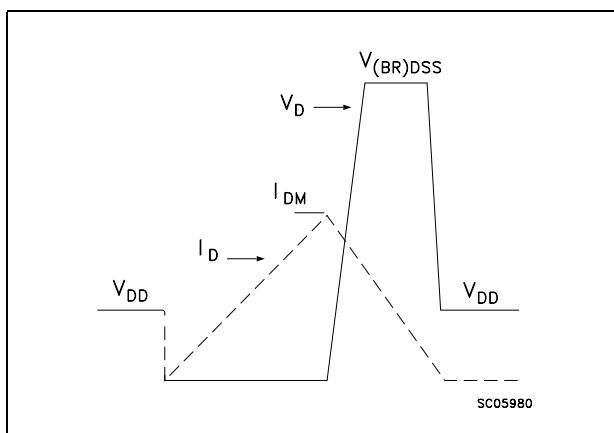
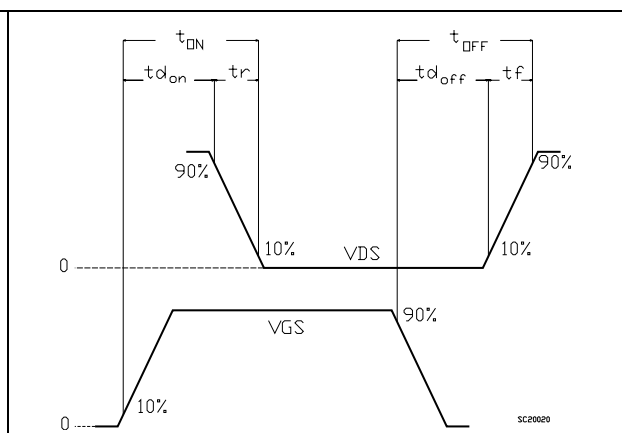


Figure 20. Switching time waveform

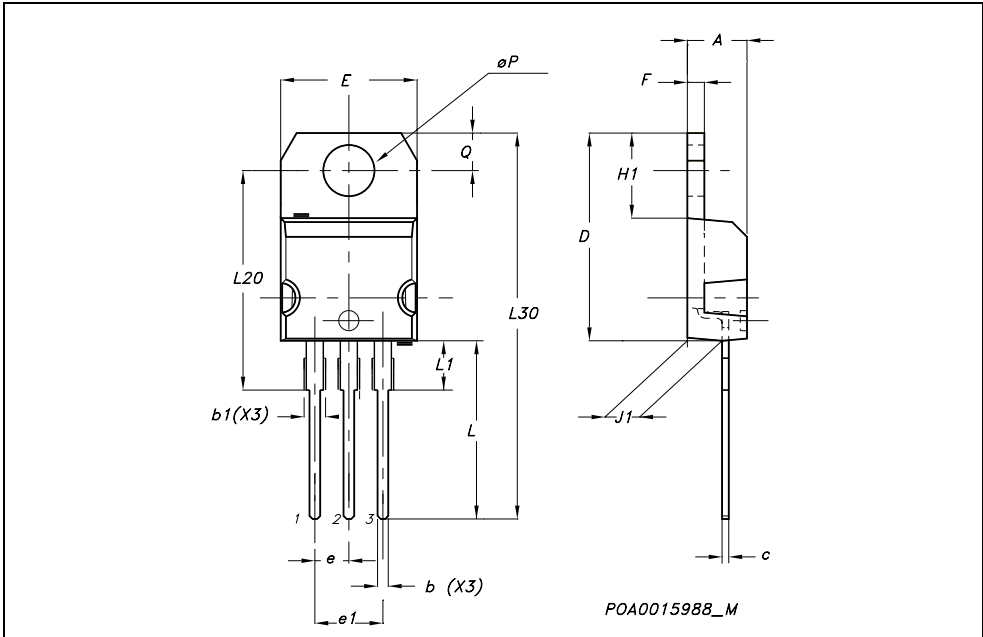


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

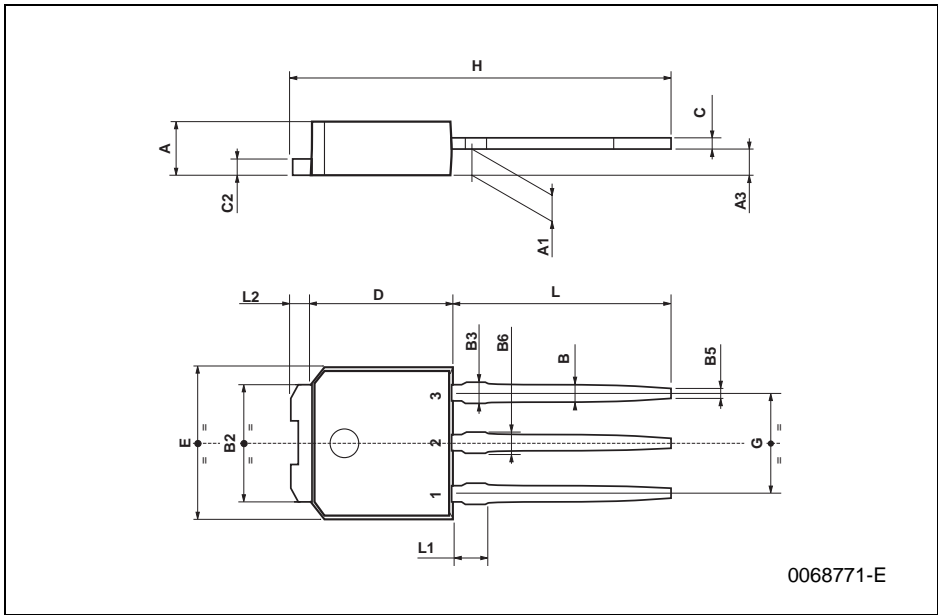
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



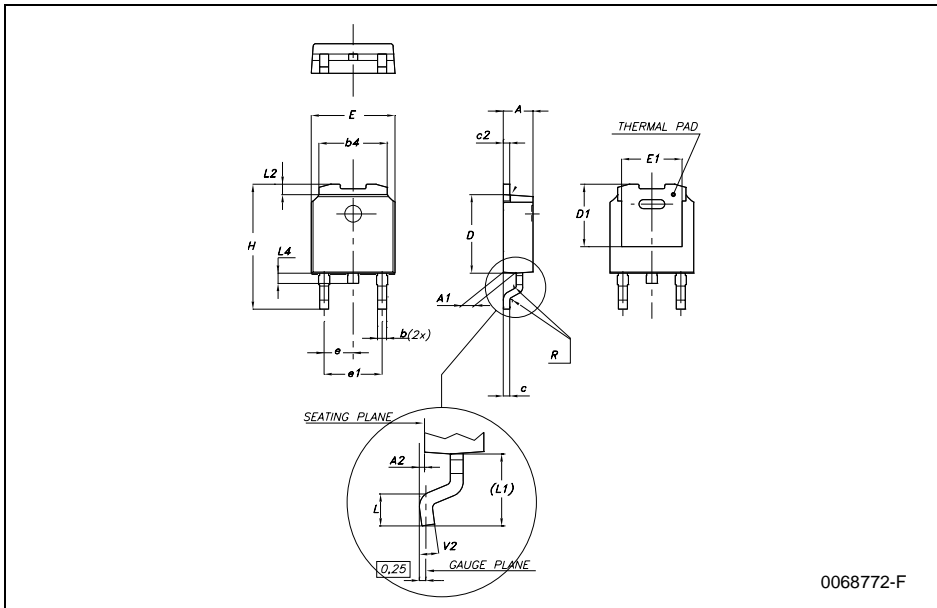
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



DPAK MECHANICAL DATA

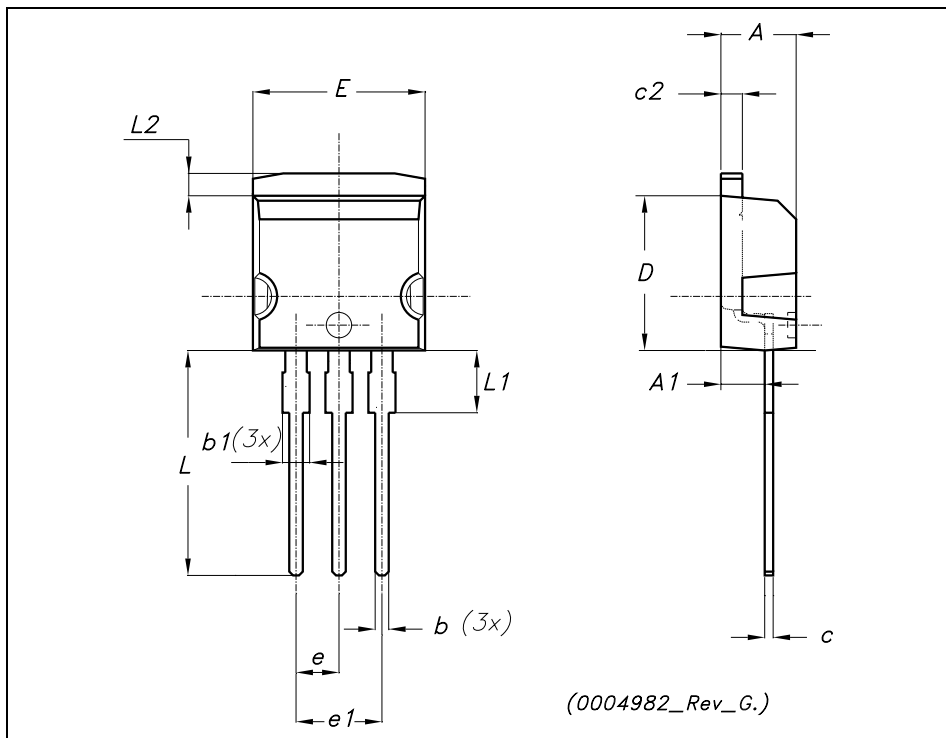
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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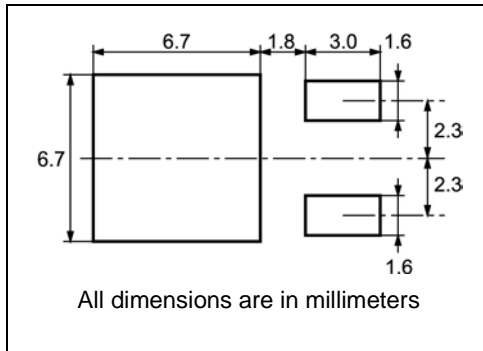
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



5 Package mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY		BULK QTY	
2500		2500	

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

6 Revision history

Table 9.

Date	Revision	Changes
16-Jun-2005	1	First release
06-Sep-2005	2	Inserted ecopack indication
03-Oct-2005	3	Corrected value on Table 1
23-Mar-2006	4	Complete version. New template

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