PANJIT SEMI CONDUCTOR

DATA SHEET

2N7002

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

VOLTAGE 60 Volts **CURRENT** 200 mAmp

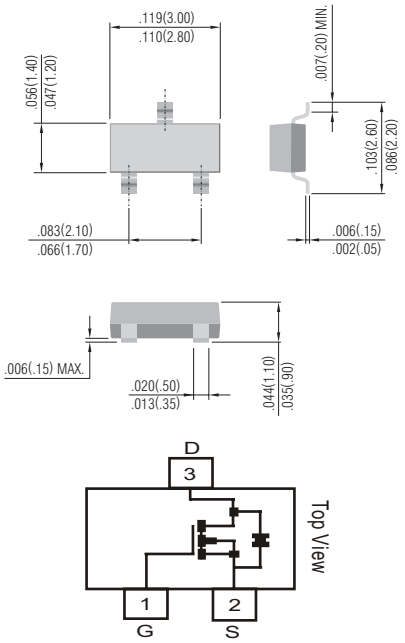
FEATURE

N-channel enhancement mode field effect transistor,designed for high speed pulse amplifier and drive application,which is manufactured by the N-channel DMOS process.

Both normal and Pb free product are available :
Normal : 80~95% Sn, 5~20% Pb
Pb free: 98.5% Sn above

SOT-23

Unit: inch (mm)



MECHANICS DATA

High density cell design for low $R_{DS(ON)}$

Voltage controlled small signal switching.

Rugged and reliabale.

High saturation current capability.

High-speed switching.CMOS logic compatible.

CMOS logic compatible input.

Not thermal runaway.

No secondary breakdown.

Marking Code: S72

ABSOLUTE MAXIMUM RATING

TA=25℃Unless otherwise noted

PARAMETER	SYMBOL	Value	UNIT
Drain-Source Voltage	V_{DSS}	60	V
Drain-gate Voltage	V_{DRG}	60	V
Gate-Source Voltage	V_{GSS}	20	V
Maximum Drain Current-Continue -Pulse (Note1)	I_D	200 800	mA
Maximum power Dissipation Derating Above 25℃	P_D	350	mW
Operating and Storage Temperature Range	T_J,T_{STG}	-55 to +150	℃
Thermal Risistance,Junction-to-Ambient	$R_{\theta JA}$	357	℃/W

Note:
1.Pulse Test: Pulse Width <300 us, Duty Cycle <2.0%.

ELECTRICAL CHRACTERISTICS

TA=25℃ Unless otherwise noted

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, ID=10 μA	60	105	—	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V, T_J=25℃ V_{DS}=60V, V_{GS}=0V, T_J=125℃	—	—	1.0 0.5	μA mA
Gate-Body Leakage, Forward	I_{GSSF}	V_{DS}=0, V_{GS}=20V	—	—	100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{DS}=0, V_{GS}=-20V	—	—	-100	nA
ON CHARACTERISTIC(note1)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 μA	1	2.1	2.5	V
Static Drain-Source On-Resisitance	$R_{DS(ON)}$	V_{GS}=10V, I_D=500mA, T_J=25℃	—	3.7	7.5	Ω
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS}=10V, I_D=500mA V_{GS}=5.0V, I_D=50mA	—	—	3.75 1.5	V
On-State Drain Current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}≧2$V_{DS(ON)}$	500	—	—	mA
Forward Transconductance	G_{FS}	V_{DS}≧2$V_{DS(ON)}$, I_D=200mA	80	—	—	mS
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, F=1.0MHz	—	—	50	pF
Output Capacitance	C_{OSS}		—	—	25	pF
Reverse Transfer Capacitance	C_{RSS}		—	—	5	pF
Turn-On Time	T_{ON}	V_{DD}=30V,R_L=25Ω, I_D=500mA V_{GS}=10V, R_{GEN}=25Ω	—	—	20	ns
Turn-Off Time	T_{OFF}		—	—	20	ns

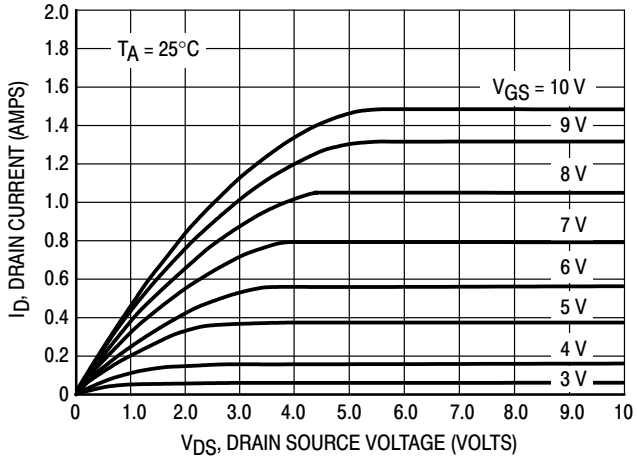


Figure 1. Ohmic Region

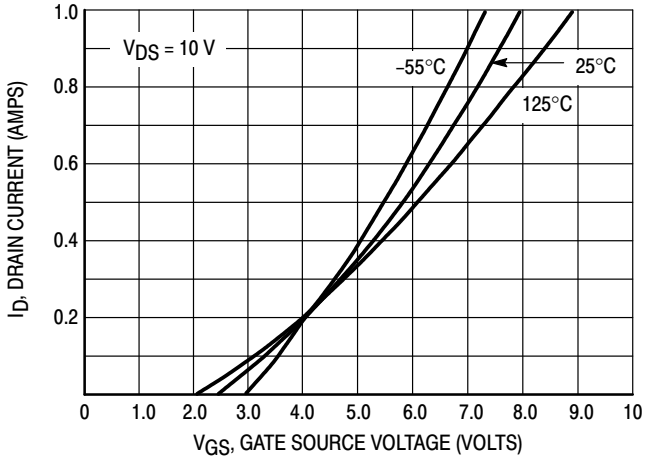


Figure 2. Transfer Characteristics

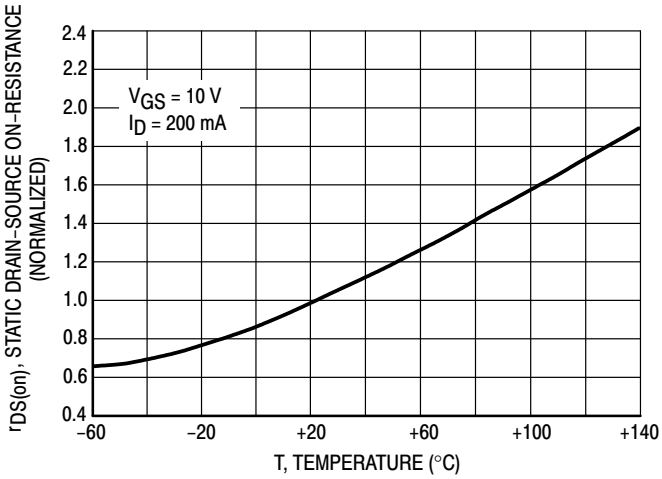


Figure 3. Temperature versus Static Drain–Source On–Resistance

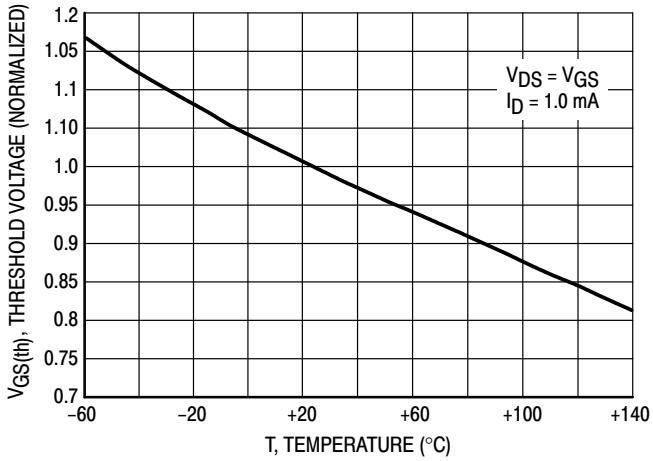


Figure 4. Temperature versus Gate Threshold Voltage