

AS1367

150mA, Adaptive Low Drop-Out Linear Regulator

1 General Description

The AS1367 is a precise, low noise, high speed, low dropout regulator with adaptive operation. Features included are high ripple rejection and low dropout voltage, a reference voltage source, an error amplifier and a current limiter.

The AS1367 provides high speed operation, low power consumption and high efficiency by automatically switching between a light load and a heavy load mode depending upon the output current level.

The EN function enables the output to be turned off, while the electric charge at the output capacitor is discharged via the internal auto-discharge resistance, and as a result the V_{OUT} pin quickly returns to the GND level.

Furthermore a Bypass Pin is included to reduce noise. The device features integrate short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying. Thermal Protection shuts down the device when die temperature reaches 160°C. This is a useful protection when the device is under sustained short circuit conditions.

The device is available in a 8-pin TDFN 2x2 package.

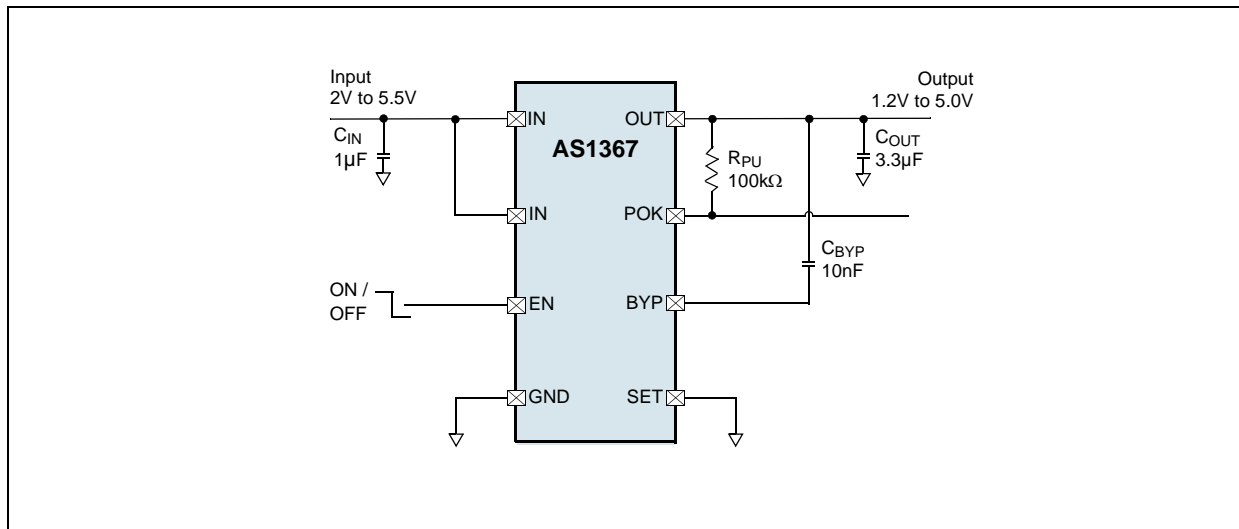
2 Key Features

- Low Dropout Voltage: 110mV @ 150mA load
- Operating Input Voltage Range: 2.0V to 5.5V
- Output Voltage Range: 1.2V to 5.0V (50mV steps)
- Max. Output Current: 150mA
- Low Shutdown Current: 100nA
- High PSRR: 60dB @ 10kHz
- Integrated Overtemperature/Overcurrent Protection
- Under-Voltage Lockout Feature
- Chip Enable Input
- Power-OK
- Low Quiescent Current: 10µA
- Low Output Noise: 15µV @ 100kHz Bandwidth
- Operating Temperature Range: -40°C to +85°C
- 8-pin TDFN 2x2 Package

3 Applications

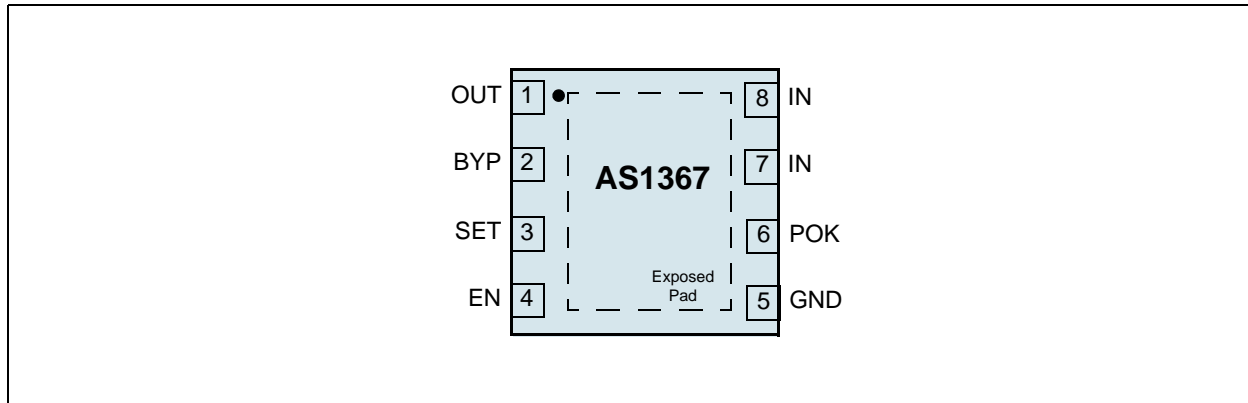
The AS1367 is ideal for cellular phones, cordless phones, wireless communication equipment, portable games, cameras, video recorders, portable audio-video equipment and personal digital assistants.

Figure 1. AS1367 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
OUT	1	Regulated Output Voltage. The current flowing out of this pin is equivalent to a DC load current. Fixed 1.2, 1.5, 1.8, 3.0, 3.3 and 4.5V output, as well as versions from 1.2V up to 5.0V can be ordered. Bypass this pin with 3.3 μ F to GND.
BYP	2	Bypass. This pin should be connected via a 10nF capacitor to pin OUT.
SET	3	Set Input. Connect to GND for preset output. Connect to a resistive voltage-divider between OUT and GND to set the output voltage between 1.2V and 5.0V.
EN	4	Active-High Enable Input. A logic low reduces the supply current to < 1 μ A. Connect this pin to pin IN for normal operation.
GND	5	Ground. This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.
POK	6	Power-OK Output. Active-low, open-drain output indicates an out-of-regulation condition. Connect a 100k Ω pull-up resistor to pin OUT for logic levels. Leave this pin unconnected if the Power-OK feature is not used.
IN	7, 8	Input Voltage. These pins should be connected to the positive terminal of the input capacitor. Bypass this pin with 1 μ F to GND. Input voltage can range from 2.0V to 5.5V.
GND	Exposed Pad	Exposed Pad. This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation. Internally it is connected GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Section 6 Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Typ	Units	Comments
IN, POK to GND	-0.3	+7		V	
OUT to GND	-0.3	V _{IN} + 0.3		V	
BYP to GND	-0.3	V _{OUT} + 0.3		V	
Output Short-Circuit Duration	Indefinite			V	
Continuous Power Dissipation		300		mW	Derate 7.1mW/°C above +70°C
Operating Temperature Range	-40	+85		°C	
Junction Temperature T _J		+150		°C	Internally limited
Thermal Resistance Θ_{JA}		+140		°C/W	
Storage Temperature Range	-65	+150		°C	
Package Body Temperature		+260		°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"</i>

6 Electrical Characteristics

$V_{IN} = V_{OUT(NOM)} + 0.5V$ or $V_{IN} = 2V$ (whichever is greater), $EN = IN$, $C_{IN} = 1\mu F$, $C_{OUT} = 3.3\mu F$, $C_{BYP} = 10nF$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$ (unless otherwise specified). Typical values are at $T_{AMB} = +25^{\circ}C$.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.0		5.5	V
V_{OUT}	Output Voltage	Trimmable in 50mV steps	1.2		5.0	V
ΔV_{OUT}	Output Voltage Accuracy	$T_{AMB} = +25^{\circ}C$, $I_{OUT} = 1mA$, $V_{OUT} > 2V$	-1		1	%
		$I_{OUT} = 100\mu A$ to $150mA$, $V_{OUT} > 2V$	-2.5		2.5	
		$T_{AMB} = +25^{\circ}C$, $I_{OUT} = 1mA$, $V_{OUT} \leq 2V$	-20		20	mV
		$I_{OUT} = 100\mu A$ to $150mA$, $V_{OUT} \leq 2V$	-50		50	
I_{OUT}	Maximum Output Current		150			mA
I_{LIM}	Current Limit	V_{OUT} forced to GND		180		mA
V_{SET}	SET Threshold	V_{OUT} up to V_{IN} , $I_{OUT} = 1mA$	50	100	150	mV
I_{SET}	SET Input Bias Current	SET = 0V	-100		100	nA
I_Q	Quiescent Current	$I_{OUT} = 0mA$		10	16	μA
		$I_{OUT} = 100\mu A$		10	20	
		$I_{OUT} = 150mA$		15	30	
$V_{IN-V_{OUT}}$	Dropout Voltage ¹	$3.0V < V_{OUT}$, $I_{OUT} = 150mA$		110	200	mV
ΔV_{LNR}	Line Regulation	$V_{IN} = (V_{OUT(NOM)} + 0.5V)$ to $5.5V$, $I_{OUT} = 1mA$		0.02	0.06^2	% / V
ΔV_{LDR}	Load Regulation	$I_{OUT} = 100\mu A$ to $150mA$		0.001	0.01	% / mA
	Dynamic Line Transient	$V_{IN} = (V_{OUT(NOM)} + 0.5V)$ to $5.5V$ within $10\mu s$, $I_{OUT} = 1mA$		17		mV
	Dynamic Load Transient	$I_{OUT} = 1mA$ to $150mA$ within $10\mu s$		12	50	mV
	Output Noise Voltage	$I_{OUT} = 10mA$, $f = 100Hz$ to $100kHz$		15		μV_{RMS}
PSRR	Output Voltage Power-Supply Rejection Ratio	$I_{OUT} = 10mA$, $f = 1kHz$		75		dB
		$I_{OUT} = 10mA$, $f = 10kHz$		60		
		$I_{OUT} = 10mA$, $f = 100kHz$		52		
Shutdown ³						
t_{ON}	EN Exit Delay ⁴	$I_{OUT} = 0mA$			500	μs
I_{OFF}	Shutdown Supply Current	EN = 0V		0.1	1	μA
V_{IH}	Enable Input Threshold		1.4		0.4	V
V_{IL}						
R_{SHDN}	Autodischarge Resistance	EN = 0V, $I_{OUT} = 0mA$		740		Ω
Power-OK Output						
V_{POK}	Power-OK Voltage Threshold	$I_{OUT} = 0mA$, $V_{OUTRISING}$	90	94	97.5	% V_{OUT}
		$I_{OUT} = 0mA$, $V_{OUTFALLING}$		3		
V_{OL}	POK Output Low Voltage	POK sinking $1mA$, EN = 0V			0.3	V
I_{POK}	POK Leakage Current	V_{OUT} in regulation		1	100	nA
SET						
V_{SET}	SET Threshold Voltage	V_{OUT} to V_{IN}	50	100	150	mV
I_{SET}	Set Input Bias Current	SET = 0V	-100		100	nA

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Thermal Protection						
T _{SHDN}	Thermal Shutdown Temperature			160		°C
ΔT _{SHDN}	Thermal Shutdown Hysteresis			20		°C

1. Dropout voltage = $V_{IN} - V_{OUT}$ when V_{OUT} is $100\text{mV} < V_{OUT}$ for $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$ (applies only to nominal output voltages $\geq 2.5\text{V}$).
2. Guaranteed by design.
3. The rise and fall time of the shutdown signal must not exceed 1ms.
4. The delay time is defined as time required to set V_{OUT} to 95% of its final nominal value.

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics

$V_{OUT} = 3.3V$, $I_{OUT} = 10mA$, $T_{AMB} = +25^{\circ}C$ (unless otherwise specified);

Figure 3. Output Voltage vs. Output Current

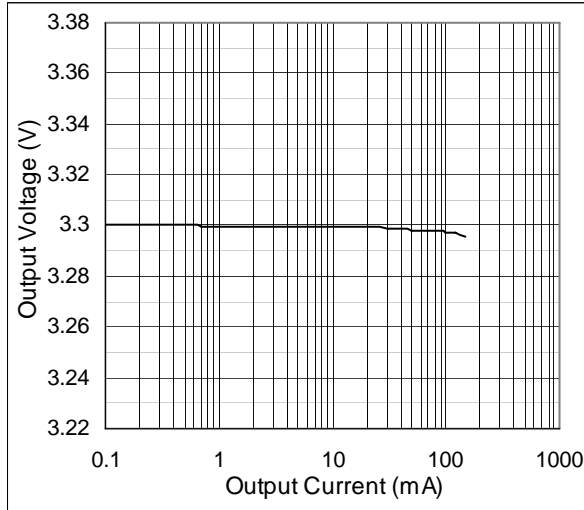


Figure 4. Output Voltage vs. Input Voltage

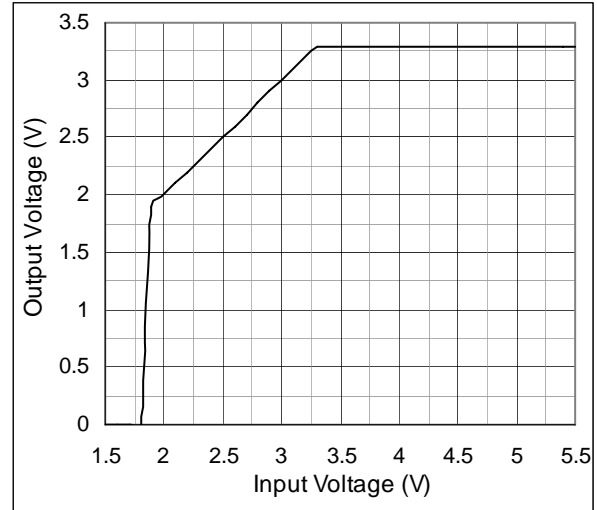


Figure 5. Output Voltage vs. Temperature

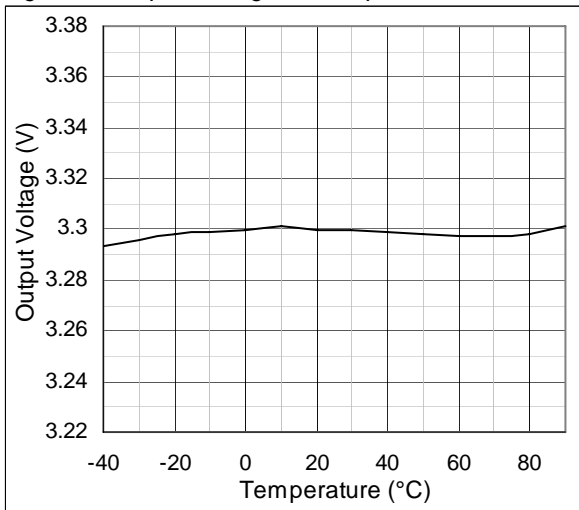


Figure 6. No Load Battery Current vs. Input Voltage

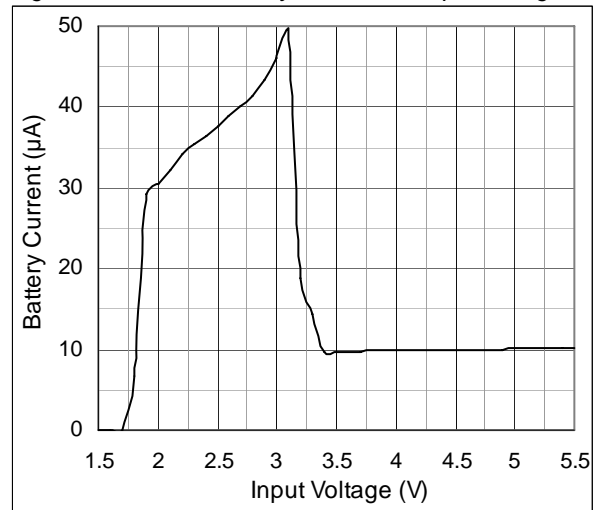


Figure 7. Quiescent Current vs. Output Current

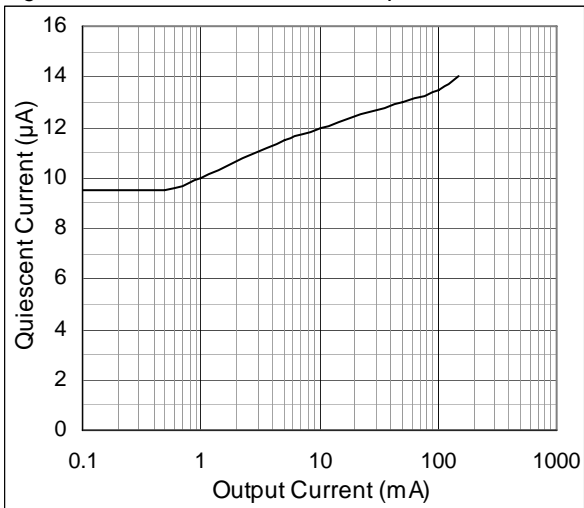


Figure 8. Quiescent Current vs. Input Voltage

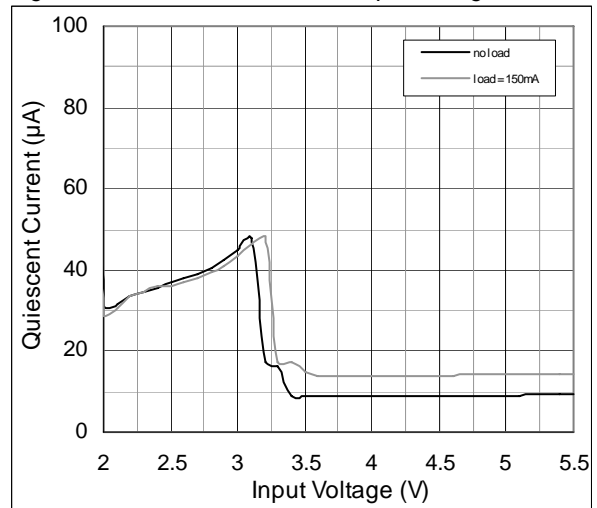


Figure 9. PSRR vs. Frequency

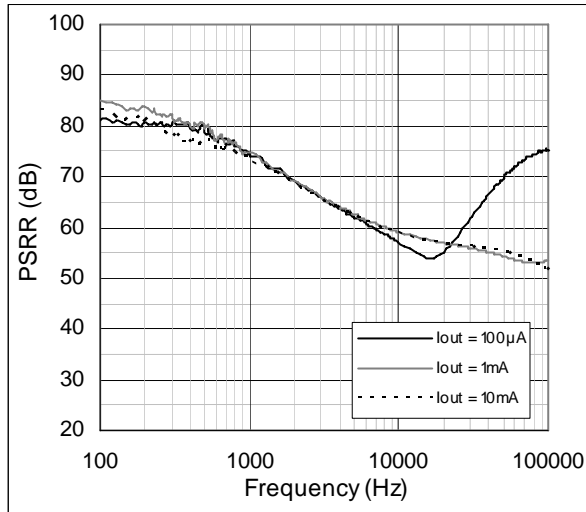


Figure 10. Startup; $V_{IN} = 3.8V$, $I_{OUT} = 100mA$

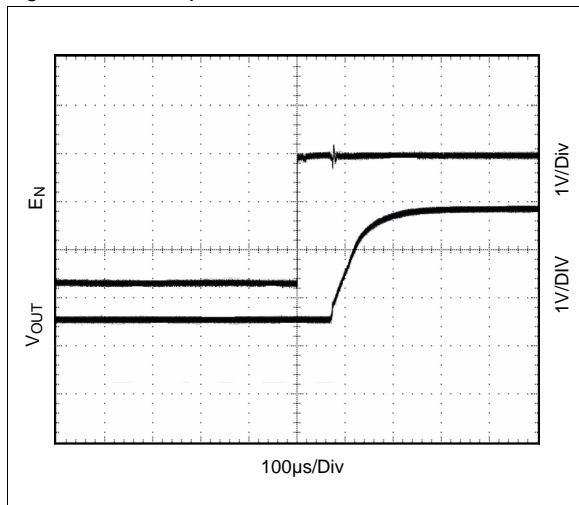


Figure 11. Startup; $V_{IN} = 3.8V$, $I_{OUT} = 100mA$

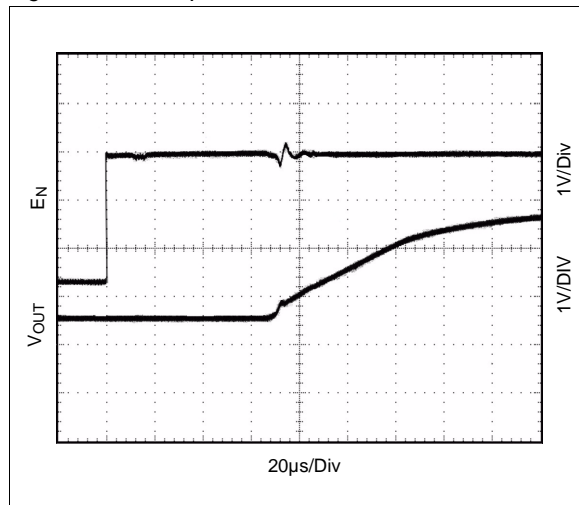


Figure 12. Line Transient Response; $V_{IN} = 3.8V$ to $4.1V$, $I_{OUT} = 100mA$

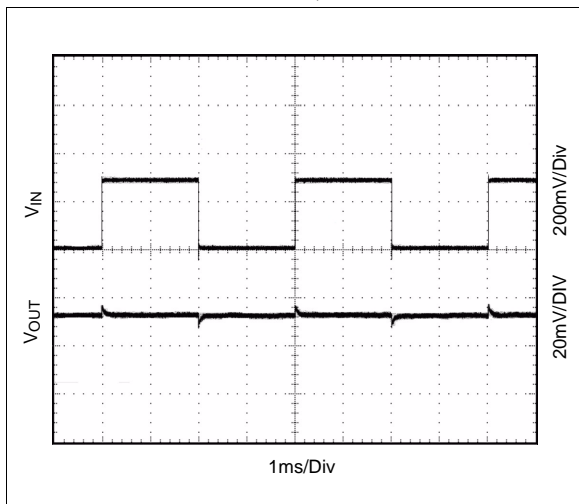


Figure 13. Line Transient Response; $V_{IN} = 3.8V$ to $4.1V$, $I_{OUT} = 100mA$

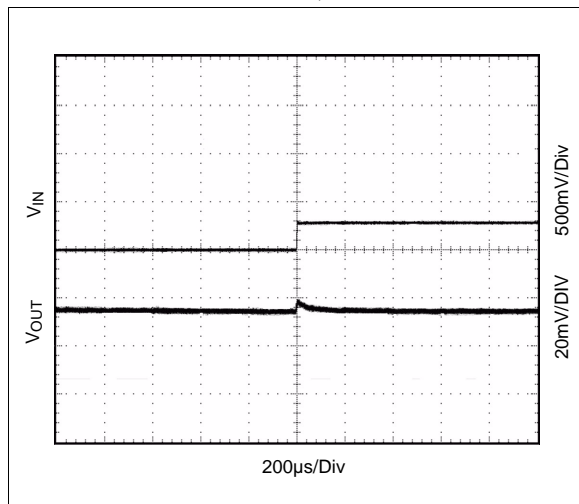


Figure 14. Load Transient Response;
 $V_{IN} = 3.8V$, $I_{OUT} = 1mA$ to $100mA$

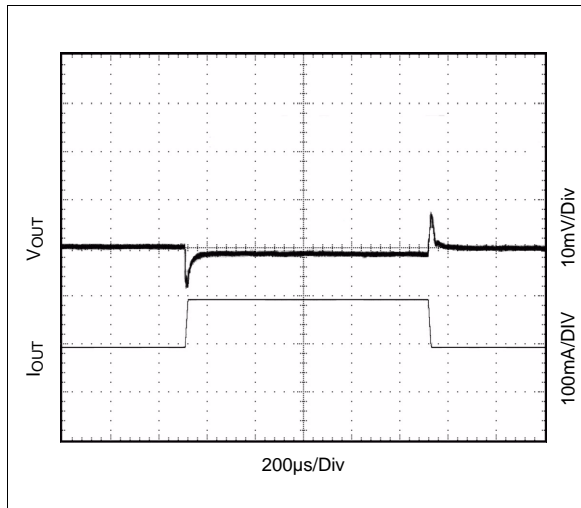
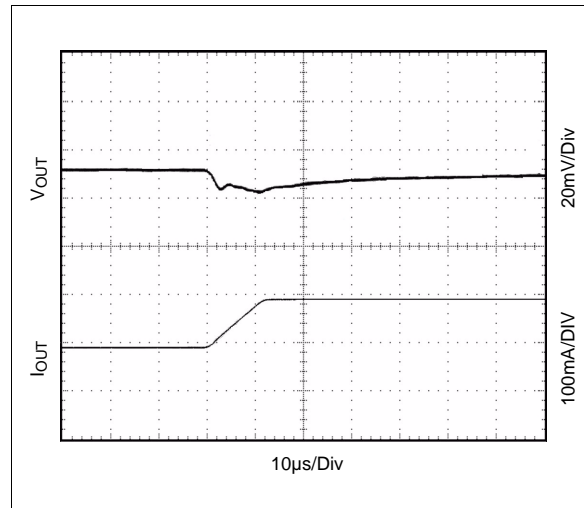


Figure 15. Load Transient Response;
 $V_{IN} = 3.8V$, $I_{OUT} = 1mA$ to $100mA$



8 Detailed Description

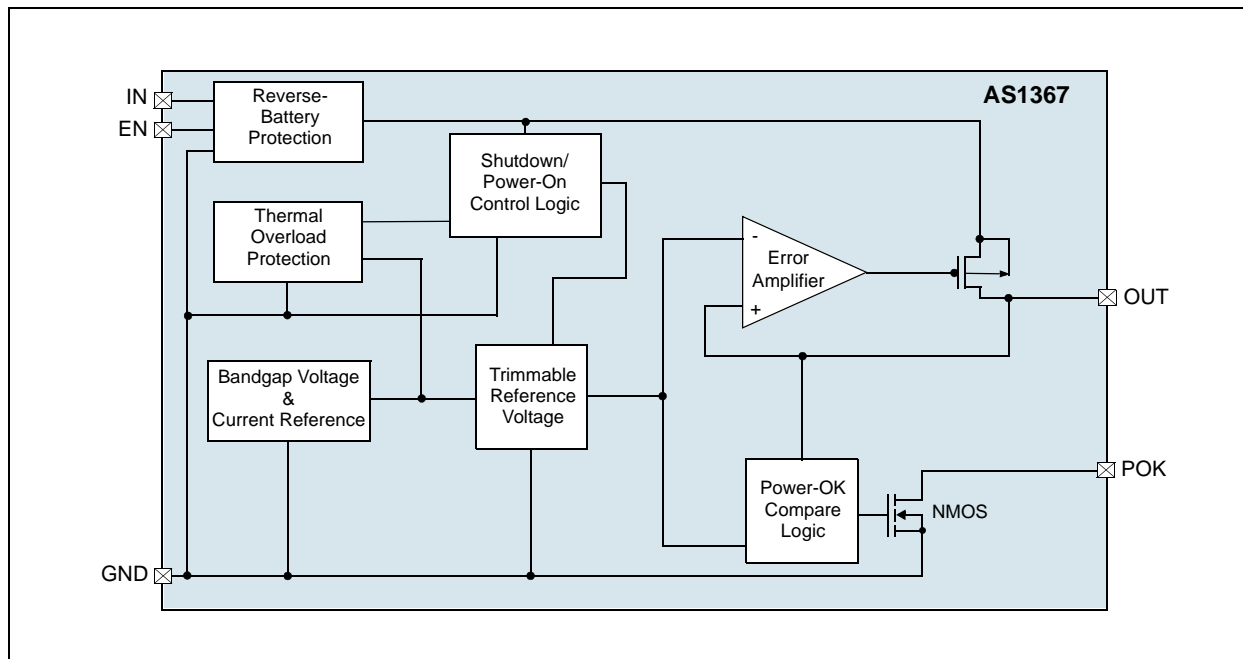
The AS1367 is low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 150mA. All devices come standard with adjustable output voltages of 1.2V to 5.0V and fixed output voltages (see [Ordering Information on page 13](#)).

The AS1367 also features a Power-OK output to indicate when the output is within 6% of final value, and also an Enable pin. Shutdown current for the whole regulator is typically 10nA. The device features integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 160°C. This is a useful protection when the device is under sustained short circuit conditions.

As illustrated in [Figure 16](#), the devices comprise a reference, error amplifier, P-channel MOSFET pass transistor, Power-OK detect logic, internal voltage divider, current limiter, reverse-battery protection, thermal sensor and shutdown logic.

The bandgap reference is connected to the inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the P-channel MOSFET gate is pulled lower, allowing more current to pass to the output, and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. The output voltage feeds back through an internal resistor voltage divider connected to pin OUT.

Figure 16. AS1367 - Block Diagram



Output Voltages

Standard products are factory-set with output voltages from 1.2V to 5.0V. A two-digit suffix of the part number identifies the nominal output (see [Ordering Information on page 13](#)). Non-standard devices are available. For more information contact: <http://www.austriamicrosystems.com/contact-us>

Power-OK

The AS1367's power-ok is built around an N-channel MOSFET. The circuitry monitors the voltage on pin SET and if the voltage goes out of regulation (e.g. during dropout, current limit, or thermal shutdown) the pin POK goes low. If the pin SET is connected to GND an internal resistive-divider is activated and connected to the output. Therefore, the Power-OK functionality can be realised with no additional external components.

The Power-OK feature is not active during shutdown and provides a power-on-reset function that can operate down to $V_{IN} = 2.0V$. A capacitor to GND may be added to generate a power-on-reset delay. To obtain a logic-level output, connect a pull-up resistor from pin POK to pin OUT. Larger values for this resistor will help to minimize current consumption; a 100k Ω resistor is perfect for most applications (see Figure 1 on page 1).

Current Limiting

The AS1367 include current limiting circuitry to protect against short-circuit conditions. The circuitry monitors and controls the gate voltage of the P-channel MOSFET, typically limiting the output current to 180mA. The P-channel MOSFET output can be shorted to ground for an indefinite period of time without damaging the device.

Thermal-Overload Protection

The devices are protected against thermal runaway conditions by the integrated thermal sensor circuitry. Thermal shutdown is an effective tool to prevent die overheating since the power transistor is the principle heat source in the device.

If the junction temperature exceeds 160°C with 20°C hysteresis, the thermal sensor starts the shutdown logic, at which point the P-channel MOSFET is switched off. After the device temperature has dropped by approximately 20°C, the thermal sensor will turn the P-channel MOSFET on again. Note that this will be exhibited as a pulsed output under continuous thermal-overload conditions.

Note: The absolute maximum junction-temperature of +150°C should not be exceeding during continual operation.

Operating Region and Power Dissipation

Maximum power dissipation is determined by the thermal resistance of the package and circuit board, the temperature difference between the die junction and the ambient air and the rate of the air flow. The power dissipation of the device is calculated by:

$$P = I_{OUT} \times (V_{IN} - V_{OUT}) \quad (EQ 1)$$

Maximum power dissipation is calculated by:

$$P_{MAX} = \frac{T_J - T_{AMB}}{\theta_{JA}} \quad (EQ 2)$$

Where:

$T_J - T_{AMB}$ is the temperature difference between the device die junction and the surrounding air.

θ_{JA} is the thermal resistance through the circuit board, copper traces, and other materials to the surrounding.

Note: Pin GND is a multi-function pin providing a connection to the system ground and acting as a heat sink. This pin should be connected to the system ground using a large pad or a ground plane.

9 Application Information

Capacitor Selection and Regulator Stability

Ceramic capacitors are highly recommended as they offer distinct advantages over their tantalum and aluminum electrolytic components. For stable operation with load currents up to the maximum over the entire device temperature range, use a 3.3µF (min) ceramic output capacitor with an ESR <math><0.2\Omega</math>. Use large output capacitor values (10µF max) to reduce noise and improve load transient-response, stability and power-supply rejection.

Note: Some ceramic capacitors exhibit large capacitance and ESR variations with variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below $T_{AMB} = -10^{\circ}\text{C}$. With X7R or X5R capacitors, a 3.3µF capacitor should be sufficient at all operating temperatures.

Power Supply Rejection Ratio

The AS1367 are designed to deliver low dropout voltages and low quiescent currents. Power-supply rejection is typically 60dB at 10kHz. To improve power supply-noise rejection and transient response, increase the values of the input and output bypass capacitors.

The [Electrical Characteristics on page 4](#) show also the device line- and load-transient responses. For further details see the Power-Supply Rejection Ratio vs. Frequency graph in the [Figure 9 on page 7](#).

Dropout Voltage

For standard products with output voltage greater than the minimum V_{IN} (1.2V), the minimum input-output voltage differential (dropout voltage) determines the lowest usable supply voltage. This determines the useful end-of-life battery voltage in battery-powered systems. The dropout voltage is a function of the P-MOSFET drain-to-source on-resistance multiplied by the load current, and it is calculated by:

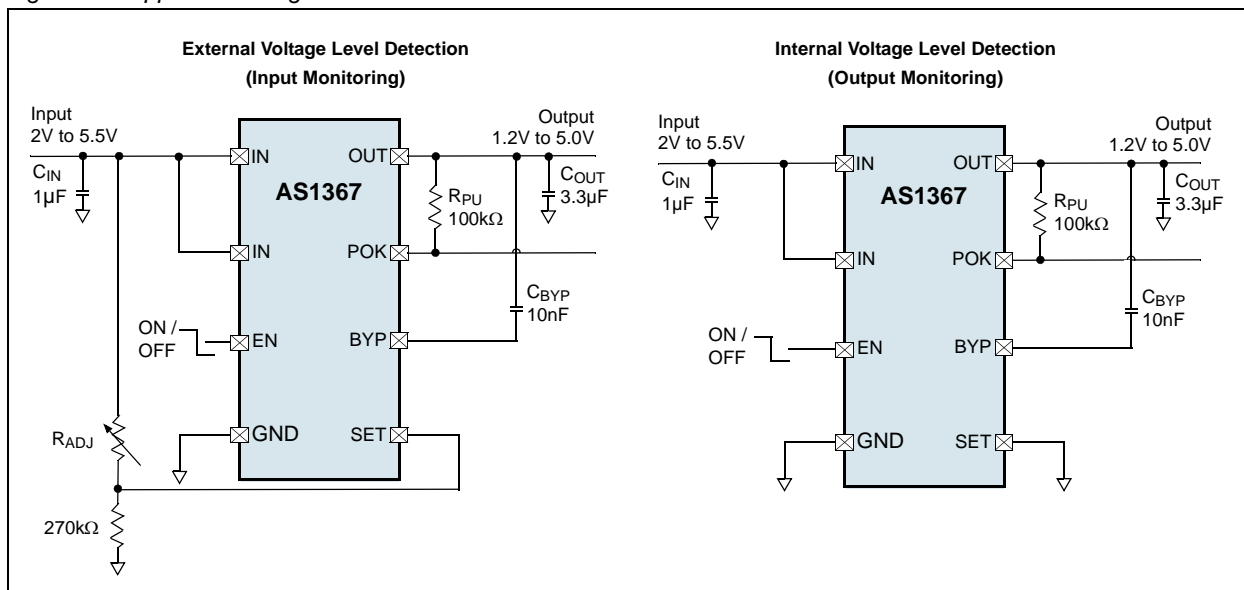
$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT} \quad (\text{EQ 3})$$

Where:

$R_{DS(ON)}$ is the drain-to-source on-resistance.

I_{OUT} is the output current.

Figure 17. Application Diagrams



10 Package Drawings and Markings

The device is available in a 8-pin TDFN package.

Figure 18. 8-pin TDFN 2x2 Package Diagram

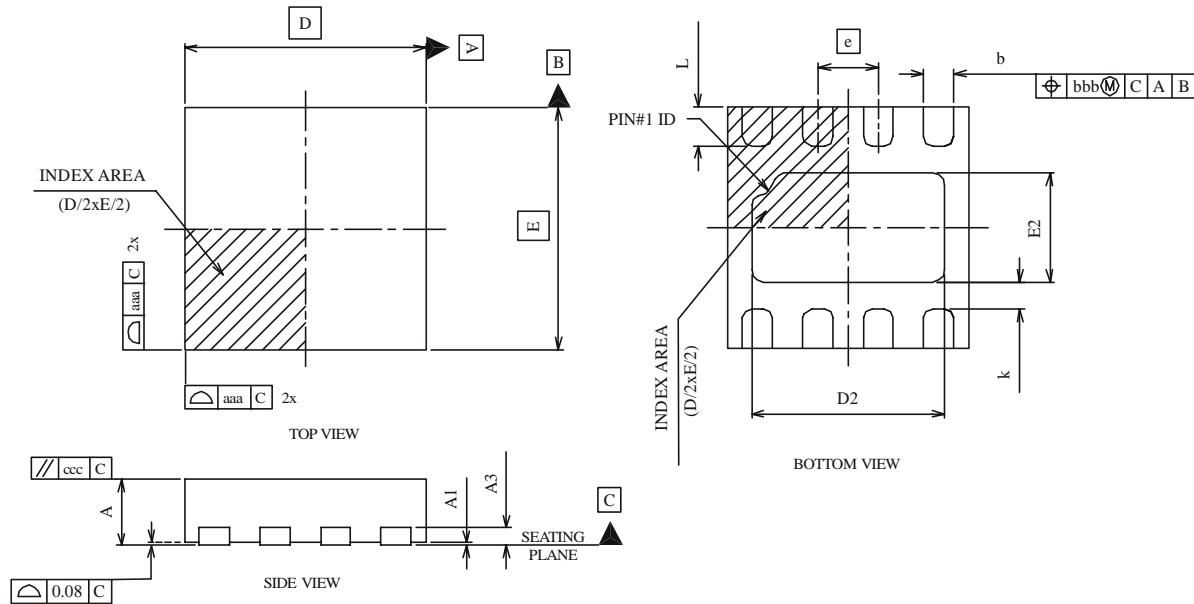


Table 4. 8-pin TDFN 2x2 package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.51	0.55	0.60	D BSC		2.00	
A1	0.00	0.02	0.05	E BSC		2.00	
A3		0.15 REF		D2	1.45	1.60	1.70
b	0.18	0.25	0.30	E2	0.75	0.90	1.00
e		0.50		L	0.225	0.325	0.425
aaa		0.15		k	0.20		
bbb		0.10		ND		4	
ccc		0.10		N		8	

Note:

- Figure 18 is shown for illustration only.
- Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- All dimensions are in millimeters, angle is in degrees (°).
- N is the total number of terminals.
- The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
- ND and NE refer to the number of terminals on each D and E side respectively.
- Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension B should not be measured in that radius area.
- Coplanarity applies to the terminals and all other bottom surface metallization.

11 Ordering Information

The device is available as the standard products listed in [Table 5](#).

Table 5. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1367-BTDT-12	AB	1.2V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-18	AC	1.8V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-30	AD	3.0V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-33	AE	3.3V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2
AS1367-BTDT-45	AF	4.5V	150mA, Adaptive LDO	Tape and Reel	8-pin TDFN 2x2

Non-standard devices from 1.2V to 5.0V are available in 50mV steps. For more information and inquiries contact <http://www.austriamicrosystems.com/contact>

Note: All products are RoHS compliant and Pb-free.

Buy our products or get free samples online at ICdirect: <http://www.austriamicrosystems.com/ICdirect>

For further information and requests, please contact us <mailto:sales@austriamicrosystems.com> or find your local distributor at <http://www.austriamicrosystems.com/distributor>

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