Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 54 Powerful Instructions – Most Single Clock Cycle Execution
  - 16 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 12 MIPS Throughput at 12 MHz
- Non-volatile Program and Data Memories
  - 512/1024 Bytes of In-System Programmable Flash Program Memory
  - 32 Bytes Internal SRAM
  - Flash Write/Erase Cycles: 10,000
  - Data Retention: 20 Years at 85°C / 100 Years at 25°C
- Peripheral Features
  - One 16-bit Timer/Counter with Prescaler and Two PWM Channels
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - 4-channel, 8-bit Analog to Digital Converter (1)
  - On-chip Analog Comparator
- Special Microcontroller Features
  - In-System Programmable (2)
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Supply Voltage Level Monitor with Interrupt and Reset
  - Internal Calibrated Oscillator
- I/O and Packages
  - 6-pin SOT: Four Programmable I/O Lines
- Operating Voltage:
  - 1.8 – 5.5V
- Programming Voltage:
  - 5V
- Speed Grade
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 8 MHz @ 2.7 – 5.5V
  - 0 – 12 MHz @ 4.5 – 5.5V
- Industrial Temperature Range
- Low Power Consumption
  - Active Mode:
    - 200µA at 1MHz and 1.8V
  - Idle Mode:
    - 25µA at 1MHz and 1.8V
  - Power-down Mode:
    - < 0.1µA at 1.8V

Note: 1. The Analog to Digital Converter (ADC) is available in ATtiny5/10, only
2. At 5V, only

8-bit AVR® Microcontroller with 512/1024 Bytes In-System Programmable Flash

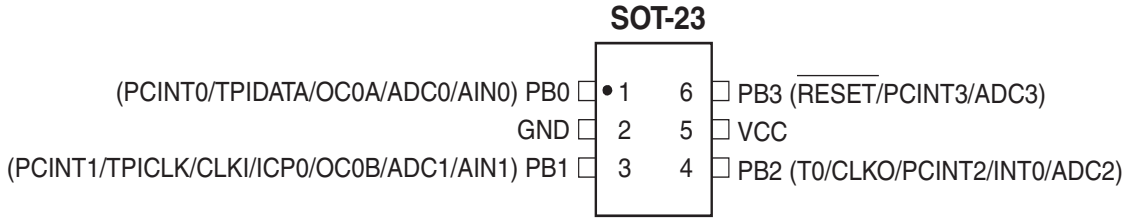
ATtiny4/5/9/10

Preliminary

8127CS–AVR–10/09

1. Pin Configurations

Figure 1-1. Pinout of ATtiny4/5/9/10



1.1 Pin Description

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB3..PB0)

This is a 4-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The port also serves the functions of various special features of the ATtiny4/5/9/10, as listed on page 36.

1.1.4 $\overline{\text{RESET}}$

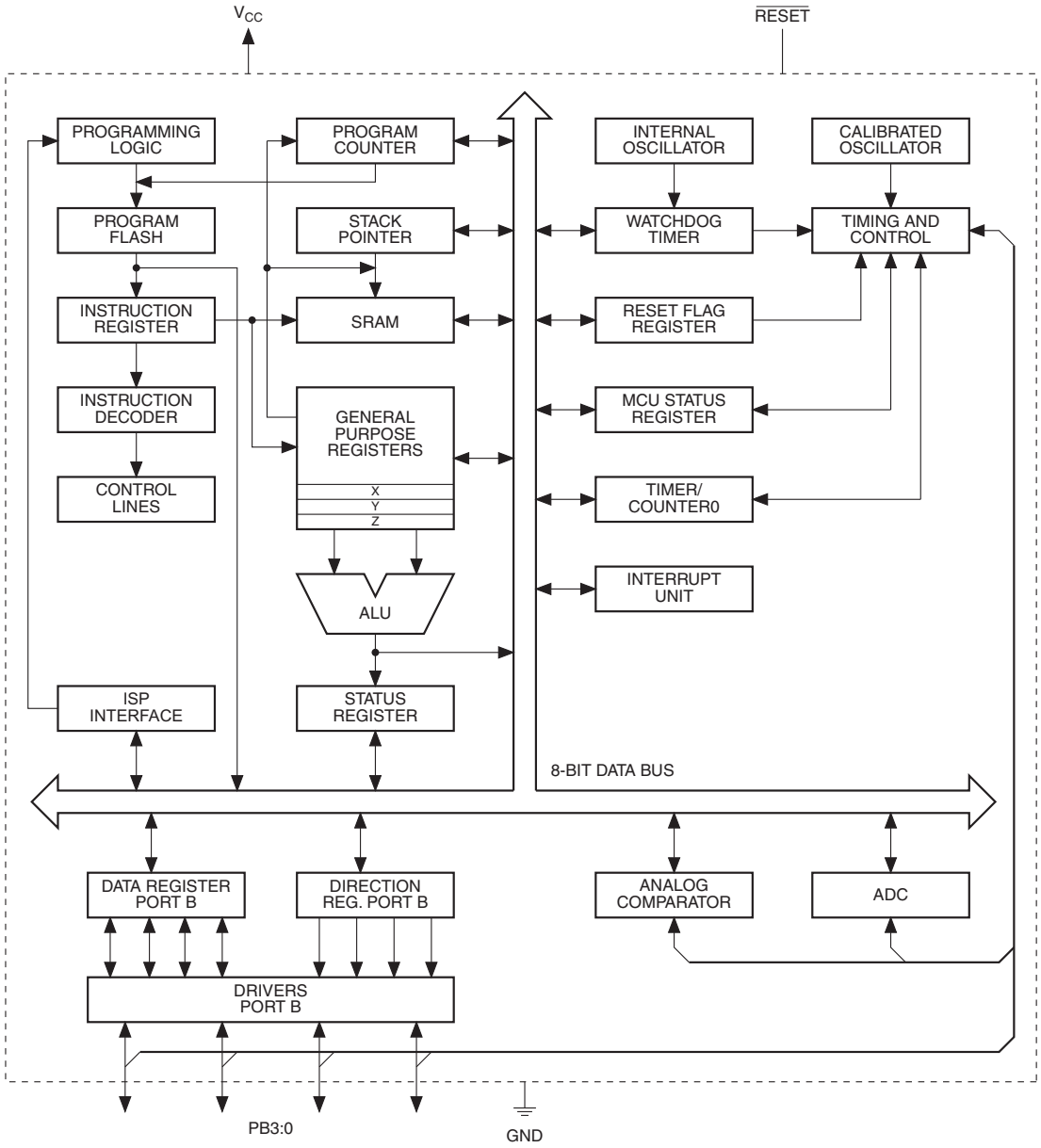
Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 16-4 on page 119. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

2. Overview

ATtiny4/5/9/10 are low-power CMOS 8-bit microcontrollers based on the compact AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny4/5/9/10 achieve throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 16 general purpose working registers and system registers. All registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is compact and code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny4/5/9/10 provide the following features: 512/1024 byte of In-System Programmable Flash, 32 bytes of SRAM, four general purpose I/O lines, 16 general purpose working registers, a 16-bit timer/counter with two PWM channels, internal and external interrupts, a programmable watchdog timer with internal oscillator, an internal calibrated oscillator, and four software selectable power saving modes. ATtiny5/10 are also equipped with a four-channel, 8-bit Analog to Digital Converter (ADC).

Idle mode stops the CPU while allowing the SRAM, timer/counter, ADC (ATtiny5/10, only), analog comparator, and interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disabled until the next interrupt or hardware reset. In Standby mode, the oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip, in-system programmable Flash allows program memory to be re-programmed in-system by a conventional, non-volatile memory programmer.

The ATtiny4/5/9/10 AVR are supported by a suite of program and system development tools, including macro assemblers and evaluation kits.

2.1 Comparison of ATtiny4, ATtiny5, ATtiny9 and ATtiny10

A comparison of the devices is shown in Table 2-1.

Table 2-1. Differences between ATtiny4, ATtiny5, ATtiny9 and ATtiny10

Device	Flash	ADC	Signature
ATtiny4	512 bytes	No	0x1E 0x8F 0x0A
ATtiny5	512 bytes	Yes	0x1E 0x8F 0x09
ATtiny9	1024 bytes	No	0x1E 0x90 0x08
ATtiny10	1024 bytes	Yes	0x1E 0x90 0x03

3. General Information

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at http://www.atmel.com/avr.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device has been characterized.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F	SREG	I	T	H	S	V	N	Z	C	Page 12
0x3E	SPH	Stack Pointer High Byte								Page 12
0x3D	SPL	Stack Pointer Low Byte								Page 12
0x3C	CCP	CPU Change Protection Byte								Page 12
0x3B	RSTFLR	–	–	–	–	WDRF	–	EXTRF	PORF	Page 34
0x3A	SMCR	–	–	–	–	SM2	SM1	SM0	SE	Page 25
0x39	OSCCAL	Oscillator Calibration Byte								Page 21
0x38	Reserved	–	–	–	–	–	–	–	–	
0x37	CLKMSR	–	–	–	–	–	–	CLKMS1	CLKMS0	Page 21
0x36	CLKPSR	–	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	Page 22
0x35	PRR	–	–	–	–	–	–	PRADC	PRTIM0	Page 26
0x34	VLMCSR	VLMF	VLMIE	–	–	–	VLM2	VLM1	VLM0	Page 33
0x33	NVMCMD	–	–	NVM Comman						Page 115
0x32	NVMCSR	NVMBSY	–	–	–	–	–	–	–	Page 115
0x31	WDTCSR	WDIF	WDIE	WDP3	–	WDE	WDP2	WDP1	WDP0	Page 32
0x30	Reserved	–	–	–	–	–	–	–	–	
0x2F	GTCCR	TSM	–	–	–	–	–	–	PSR	Page 79
0x2E	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	Page 73
0x2D	TCCR0B	ICNC0	ICES0	–	WGM03	WGM02	CS02	CS01	CS00	Page 75
0x2C	TCCR0C	FOC0A	FOC0B	–	–	–	–	–	–	Page 76
0x2B	TIMSK0	–	–	ICIE0	–	–	OCIE0B	OCIE0A	TOIE0	Page 78
0x2A	TIFR0	–	–	ICF0	–	–	OCF0B	OCF0A	TOV0	Page 79
0x29	TCNT0H	Timer/Counter0 – Counter Register High Byte								Page 77
0x28	TCNT0L	Timer/Counter0 – Counter Register Low Byte								Page 77
0x27	OCR0AH	Timer/Counter0 – Compare Register A High Byte								Page 77
0x26	OCR0AL	Timer/Counter0 – Compare Register A Low Byte								Page 77
0x25	OCR0BH	Timer/Counter0 – Compare Register B High Byte								Page 77
0x24	OCR0BL	Timer/Counter0 – Compare Register B Low Byte								Page 77
0x23	ICR0H	Timer/Counter0 - Input Capture Register High Byte								Page 78
0x22	ICR0L	Timer/Counter0 - Input Capture Register Low Byte								Page 78
0x21	Reserved	–	–	–	–	–	–	–	–	
0x20	Reserved	–	–	–	–	–	–	–	–	
0x1F	ACSR	ACD	–	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	Page 81
0x1E	Reserved	–	–	–	–	–	–	–	–	
0x1D	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	Page 93
0x1C	ADCSRB	–	–	–	–	–	ADTS2	ADTS1	ADTS0	Page 94
0x1B	ADMUX	–	–	–	–	–	–	MUX1	MUX0	Page 93
0x1A	Reserved	–	–	–	–	–	–	–	–	
0x19	ADCL	ADC Conversion Result								Page 95
0x18	Reserved	–	–	–	–	–	–	–	–	
0x17	DIDR0	–	–	–	–	ADC3D	ADC2D	ADC1D	ADC0D	Page 82, Page 95
0x16	Reserved	–	–	–	–	–	–	–	–	
0x15	EICRA	–	–	–	–	–	–	ISC01	ISC00	Page 37
0x14	EIFR	–	–	–	–	–	–	–	INTF0	Page 38
0x13	EIMSK	–	–	–	–	–	–	–	INT0	Page 38
0x12	PCICR	–	–	–	–	–	–	–	PCIE0	Page 39
0x11	PCIFR	–	–	–	–	–	–	–	PCIF0	Page 39
0x10	PCMSK	–	–	–	–	PCINT3	PCINT2	PCINT1	PCINT0	Page 39
0x0F	Reserved	–	–	–	–	–	–	–	–	
0x0E	Reserved	–	–	–	–	–	–	–	–	
0x0D	Reserved	–	–	–	–	–	–	–	–	
0x0C	PORTCR	–	–	–	–	–	–	BBMB	–	Page 50
0x0B	Reserved	–	–	–	–	–	–	–	–	
0x0A	Reserved	–	–	–	–	–	–	–	–	
0x09	Reserved	–	–	–	–	–	–	–	–	
0x08	Reserved	–	–	–	–	–	–	–	–	
0x07	Reserved	–	–	–	–	–	–	–	–	
0x06	Reserved	–	–	–	–	–	–	–	–	
0x05	Reserved	–	–	–	–	–	–	–	–	
0x04	Reserved	–	–	–	–	–	–	–	–	
0x03	PUEB	–	–	–	–	PUEB3	PUEB2	PUEB1	PUEB0	Page 50
0x02	PORTB	–	–	–	–	PORTB3	PORTB2	PORTB1	PORTB0	Page 51
0x01	DDRB	–	–	–	–	DDRB3	DDRB2	DDRB1	DDRB0	Page 51
0x00	PINB	–	–	–	–	PINB3	PINB2	PINB1	PINB0	Page 51

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. The ADC is available in ATtiny5/10, only.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3/4
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	3/4
RET		Subroutine Return	PC ← STACK	None	4/5
RETI		Interrupt Return	PC ← STACK	I	4/5
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd – K	Z, C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	A, b	Skip if Bit in I/O Register is Set	if (I/O(A,b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow.	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	1/2
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Decrement	X ← X - 1, Rd ← (X)	None	2/3
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	1/2
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Decrement	Y ← Y - 1, Rd ← (Y)	None	2/3
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1/2
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2/3
LDS	Rd, k	Store Direct from SRAM	Rd ← (k)	None	1
ST	X, Rr	Store Indirect	(X) ← Rr	None	1
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1
ST	- X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1
ST	- Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1
ST	Z+, Rr	Store Indirect and Post-Increment.	(Z) ← Rr, Z ← Z + 1	None	1
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1, (Z) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	1
IN	Rd, A	In from I/O Location	Rd ← I/O (A)	None	1
OUT	A, Rr	Out to I/O Location	I/O (A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
BREAK		Break	(see specific descr. for Break)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

6. Ordering Information

6.1 ATtiny4

Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
12	1.8 - 5.5V	ATtiny4-TSHR[3][4]	6ST1	Industrial (-40°C to 85°C)[4]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Topside marking for ATtiny4: T4**x** (**x** stands for “die revision”).
4. Bottomside marking for ATtiny4: z**H**zzz [**H** stands for (-40°C to 85°C)].

Package Type	
6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)

6.2 ATtiny5

Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
12	1.8 - 5.5V	ATtiny5-TSHR[3][4]	6ST1	Industrial (-40°C to 85°C)[4]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Topside marking for ATtiny5: T5**x** (**x** stands for “die revision”).
4. Bottomside marking for ATtiny5: z**H**zzz [**H** stands for (-40°C to 85°C)].

Package Type	
6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)

6.3 ATtiny9

Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
12	1.8 - 5.5V	ATtiny9-TSHR[3][4]	6ST1	Industrial (-40°C to 85°C)[4]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Topside marking for ATtiny9: T9**x** (**x** stands for “die revision”).
4. Bottomside marking for ATtiny9: z**H**zzz [**H** stands for (-40°C to 85°C)].

Package Type	
6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)

6.4 ATtiny10

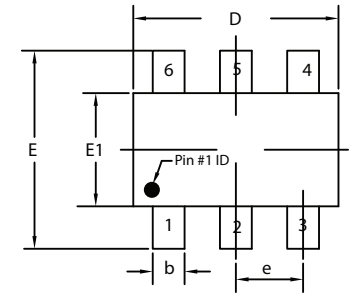
Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
12	1.8 - 5.5V	ATtiny10-TSHR[3][4]	6ST1	Industrial (-40°C to 85°C)[4]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Topside marking for ATtiny10: T10**x** (**x** stands for “die revision”).
4. Bottomside marking for ATtiny10: z**H**zzz [**H** stands for (-40°C to 85°C)].

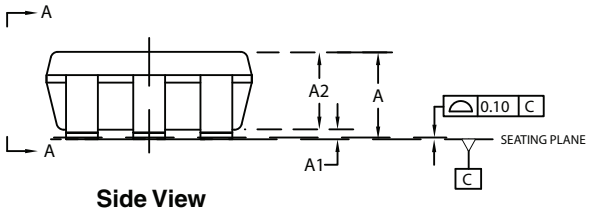
Package Type	
6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)

7. Packaging Information

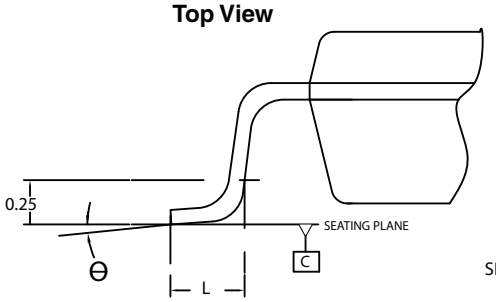
7.1 6ST1



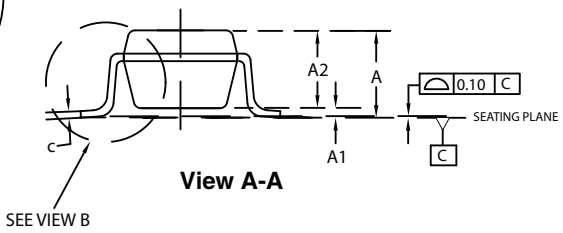
Top View



Side View



View B



View A-A

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.45	
A1	0	–	0.15	
A2	0.90	–	1.30	
D	2.80	2.90	3.00	2
E	2.60	2.80	3.00	
E1	1.50	1.60	1.75	
L	0.30	0.45	0.55	
e	0.95 BSC			
b	0.30	–	0.50	3
c	0.09	–	0.20	
θ	0°	–	8°	

Notes:
1. This package is compliant with JEDEC specification MO-178 Variation AB
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrustion or gate burrs shall not exceed 0.25 mm per end.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm
4. Die is facing down after trim/form.

6/30/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**6ST1,** 6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)	TAQ	6ST1	A

8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny4/5/9/10 device.

8.1 ATtiny4

8.1.1 Rev. D

- **ESD HBM (ESD STM 5.1) level ±1000V**
- **Lock bits re-programming**

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Lock bits re-programming

Attempt to re-program Lock bits to present, or lower protection level (tampering attempt), causes erroneously one, random line of Flash program memory to get erased. The Lock bits will not get changed, as they should not.

Problem Fix / Workaround

Do not attempt to re-program Lock bits to present, or lower protection level.

8.1.2 Rev. A – C

Not sampled.

8.2 ATtiny5

8.2.1 Rev. D

- **ESD HBM (ESD STM 5.1) level ±1000V**
- **Lock bits re-programming**

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Lock bits re-programming

Attempt to re-program Lock bits to present, or lower protection level (tampering attempt), causes erroneously one, random line of Flash program memory to get erased. The Lock bits will not get changed, as they should not.

Problem Fix / Workaround

Do not attempt to re-program Lock bits to present, or lower protection level.

8.2.2 Rev. A – C

Not sampled.

8.3 ATtiny9

8.3.1 Rev. D

- **ESD HBM (ESD STM 5.1) level ±1000V**
- **Lock bits re-programming**

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Lock bits re-programming

Attempt to re-program Lock bits to present, or lower protection level (tampering attempt), causes erroneously one, random line of Flash program memory to get erased. The Lock bits will not get changed, as they should not.

Problem Fix / Workaround

Do not attempt to re-program Lock bits to present, or lower protection level.

8.3.2 Rev. A – C

Not sampled.

8.4 ATtiny10

8.4.1 Rev. C – D

- **ESD HBM (ESD STM 5.1) level ±1000V**
- **Lock bits re-programming**

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Lock bits re-programming

Attempt to re-program Lock bits to present, or lower protection level (tampering attempt), causes erroneously one, random line of Flash program memory to get erased. The Lock bits will not get changed, as they should not.

Problem Fix / Workaround

Do not attempt to re-program Lock bits to present, or lower protection level.

8.4.2 Rev. A – B

Not sampled.

9. Datasheet Revision History

9.1 Rev. 8127C – 10/09

1. Updated values and notes:
   – Table 16-1 in Section 16.2 “DC Characteristics” on page 116
   – Table 16-3 in Section 16.4 “Clock Characteristics” on page 118
   – Table 16-6 in Section 16.5.2 “VCC Level Monitor” on page 119
   – Table 16-9 in Section 16.8 “Serial Programming Characteristics” on page 121
2. Updated Figure 16-1 in Section 16.3 “Speed Grades” on page 117
3. Added Typical Characteristics Figure 17-36 in Section 17.2.7 “Analog Comparator Offset” on page 140. Also, updated some other plots in Typical Characteristics.
4. Added topside and bottomside marking notes in Section 6. “Ordering Information” on page 10, up to page 13
5. Added ESD errata, see Section 8. “Errata” on page 15
6. Added Lock bits re-programming errata, see Section 8. “Errata” on page 15

9.2 Rev. 8127B – 08/09

1. Updated document template
2. Expanded document to also cover devices ATtiny4, ATtiny5 and ATtiny9
3. Added section:
   – “Comparison of ATtiny4, ATtiny5, ATtiny9 and ATtiny10” on page 4
4. Updated sections:
   – “ADC Clock – clkADC” on page 18
   – “Starting from Idle / ADC Noise Reduction / Standby Mode” on page 20
   – “ADC Noise Reduction Mode” on page 24
   – “Analog to Digital Converter” on page 25
   – “SMCR – Sleep Mode Control Register” on page 25
   – “PRR – Power Reduction Register” on page 26
   – “Alternate Functions of Port B” on page 48
   – “Overview” on page 83
   – “Physical Layer of Tiny Programming Interface” on page 96
   – “Overview” on page 107
   – “ADC Characteristics (ATtiny5/10, only)” on page 120
   – “Supply Current of I/O Modules” on page 122
   – “Register Summary” on page 6
   – “Ordering Information” on page 10
5. Added figure:
   – “Using an External Programmer for In-System Programming via TPI” on page 97
6. Updated figure:
   – “Data Memory Map (Byte Addressing)” on page 15
7. Added table:
   – “Number of Words and Pages in the Flash (ATtiny4/5)” on page 109

8. Updated tables:
   - “Active Clock Domains and Wake-up Sources in Different Sleep Modes” on page 23
   - “Reset and Interrupt Vectors” on page 35
   - “Number of Words and Pages in the Flash (ATtiny9/10)” on page 109
   - “Signature codes” on page 110

9.3 Rev. 8127A – 04/09

1. Initial revision

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