16-Bit Long-Reach Video SERDES with Bidirectional Side-Channel

The ISL34321 is a serializer/deserializer of LVCMOS parallel video data. The video data presented to the serializer on the parallel LVCMOS bus is serialized into a high-speed differential signal. This differential signal is converted back to parallel video at the remote end by the deserializer. It also transports auxiliary data bidirectionally over the same link during the video vertical retrace interval.

I^2C bus mastering allows the placement of external slave devices on the remote side of the link. An I^2C controller can be place on either side of the link allowing bidirectional I^2C communication through the link to the external devices on the other side. Both chips can be fully configured from a single controller or independently by local controllers.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL34321INZ*	ISL34321INZ	-40 to +85	48 Ld EPTQFP	Q48.7x7B

*Add "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
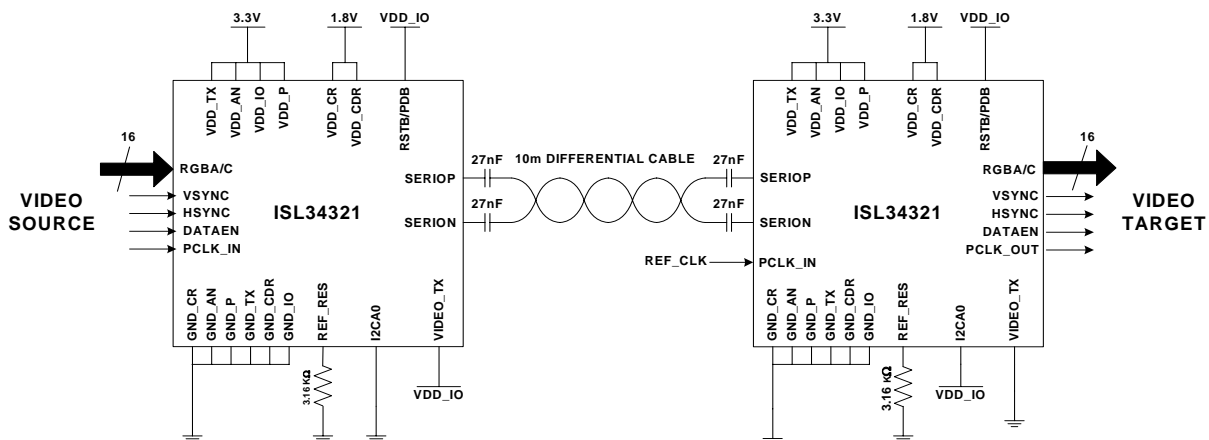
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
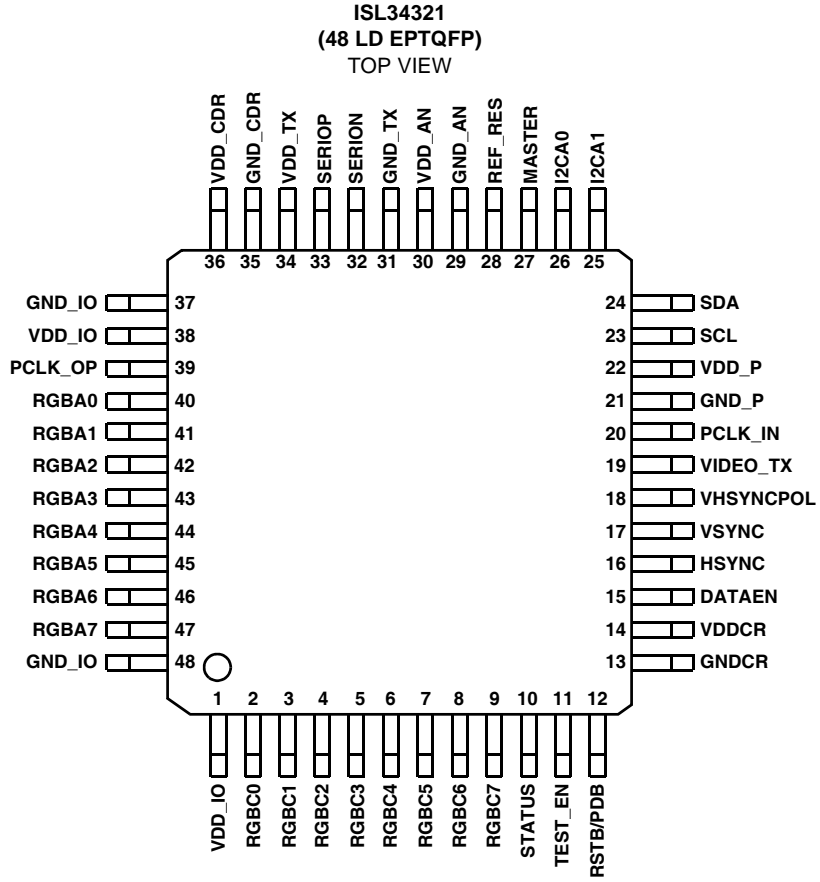
Features

- 16-bit RGB transport over single differential pair
- 6MHz to 45MHz pixel clock rates
- Bi-directional auxiliary data transport without extra bandwidth and over the same differential pair
- Hot plugging with automatic resynchronization every HSYNC.
- I^2C Bus Mastering to the remote side of the link with a controller on either the serializer or deserializer
- Selectable clock edge for parallel data output
- Internal 100Ω termination on high-speed serial lines
- DC balanced with industry standard 8b/10b line code allows AC-coupling
    - Provides immunity against ground shifts
- 16 programmable settings each for transmitter amplitude boost and pre-emphasis and receiver equalization allow for longer cable lengths and higher data rates
- Programmable powerdown of the transmitter and the receiver.
- Same device for serializer and deserializer simplifies inventory
- I^2C communication interface
- 8kV ESD rating for serial lines
- Pb-free (RoHS compliant)

Applications

- Video entertainment systems
- Industrial computing terminals
- Remote cameras

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pinout

ISL34321
(48 LD EPTQFP)
TOP VIEW

Pin assignments (top view, counterclockwise):

Top side (pins 36–25): VDD_CDR (36), GND_CDR (35), VDD_TX (34), SERIOP (33), SERION (32), GND_TX (31), VDD_AN (30), GND_AN (29), REF_RES (28), MASTER (27), I2CA0 (26), I2CA1 (25)

Left side (pins 37–48): GND_IO (37), VDD_IO (38), PCLK_OP (39), RGBA0 (40), RGBA1 (41), RGBA2 (42), RGBA3 (43), RGBA4 (44), RGBA5 (45), RGBA6 (46), RGBA7 (47), GND_IO (48)

Right side (pins 24–13): SDA (24), SCL (23), VDD_P (22), GND_P (21), PCLK_IN (20), VIDEO_TX (19), VHSYNCPOL (18), VSYNC (17), HSYNC (16), DATAEN (15), VDDCR (14), GNDCR (13)

Bottom side (pins 1–12): VDD_IO (1), RGBC0 (2), RGBC1 (3), RGBC2 (4), RGBC3 (5), RGBC4 (6), RGBC5 (7), RGBC6 (8), RGBC7 (9), STATUS (10), TEST_EN (11), RSTB/PDB (12)

Block Diagram

ISL34321

Absolute Maximum Ratings

Supply Voltage
  VDD_P to GND_P, VDD_TX to GND_TX,
    VDD_IO to GND_IO . . . . -0.5V to 4.6V
  VDD_CDR to GND_CDR, VDD_CR to GND_CR . . -0.5V to 2.5V
    Between any pair of GND_P, GND_TX,
    GND_IO, GND_CDR, GND_CR . . . . -0.1V to 0.1V
3.3V Tolerant LVTTL/LVCMOS Input Voltage -0.3V to VDD_IO+0.3V
Differential Input Voltage . . . . -0.3V to VDD_IO + 0.3V
Differential Output Current . . . . Short Circuit Protected
LVTTL/LVCMOS Outputs . . . . Short Circuit Protected
ESD Rating
  Human Body Model
    All pins 4kV
    SERIOP/N (all VDD Connected, all GND Connected) 8kV
  Machine Model. 200V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA}	θ_{JC} (°C/W)
EPTQFP.	38	12

Maximum Power Dissipation. 327mW
Maximum Junction Temperature . . . . +125°C
Maximum Storage Temperature Range. . . . .-65°C to +150°C
Operating Temperature Range . . . .-40°C to +85°C
Pb-free Reflow Profile . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise indicated, all data is for: VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, T_A = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE						
VDD_CDR, VDD_CR			1.7	1.8	1.9	V
VDD_TX, VDD_P, VDD_AN, VDD_IO			3.0	3.3	3.6	V
SERIALIZER POWER SUPPLY CURRENTS						
Total 1.8V Supply Current		PCLK_IN = 45MHz		62	80	mA
Total 3.3V Supply Current		(Note 3)		40	52	mA
DESERIALIZER POWER SUPPLY CURRENTS						
Total 1.8V Supply Current		PCLK_IN=45MHz		66	76	mA
Total 3.3V Supply Current		(Note 3)		50	63	mA
POWER-DOWN SUPPLY CURRENT						
Total 1.8V Power-Down Supply Current		RSTB = GND		10		mA
Total 3.3V Power-Down Supply Current				0.5		mA
PARALLEL INTERFACE						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}		-1	±0.01	1	µA
High Level Output Voltage	V_{OH}	I_{OH} = -4.0mA, VDD_IO = 3.0V	2.6			V
Low Level Output Voltage	V_{OL}	I_{OL} = 4.0mA, VDD_IO = 3.6V			0.4	V
Output Short Circuit Current	I_{OSC}				35	mA
Output Rise and Fall Times	t_{OR}/t_{OF}	Slew rate control set to min C_L = 8pF		1		ns
		Slew rate control set to max C_L = 8pF		4		ns

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ISL34321

Electrical Specifications
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIALIZER PARALLEL INTERFACE						
PCLK_IN Frequency	f_{IN}		6		45	MHz
PCLK_IN Duty Cycle	t_{IDC}		40	50	60	%
Parallel Input Setup Time	t_{IS}		3.5			ns
Parallel Input Hold Time	t_{IH}		1.0			ns
DESERIALIZER PARALLEL INTERFACE						
PCLK_OUT Frequency	f_{OUT}		6		45	MHz
PCLK_OUT Duty Cycle	t_{ODC}			50		%
PCLK_OUT Period Jitter (rms)	t_{OJ}	Clock randomizer off		0.5		$\%t_{PCLK}$
PCLK_OUT Spread Width	t_{OSPRD}	Clock randomizer on		±20		$\%t_{PCLK}$
PCLK_OUT to Parallel Data Outputs (includes Sync and DE pins)	t_{DV}	Relative to PCLK_OUT, (Note 4)	-1.0		5.5	ns
Deserializer Output Latency	t_{CPD}	Inherent in the design	4	9	14	PCLK
DESERIALIZER REFERENCE CLOCK (REF_CLK IS FED INTO PCLK_IN)						
REF_CLK Lock Time	t_{PLL}			100		µs
REF_CLK to PCLK_OUT Maximum Frequency Offset		PCLK_OUT is the recovered clock	1500	5000		ppm
HIGH-SPEED TRANSMITTER						
HS Differential Output Voltage, Transition Bit	VOD_{TR}	TXCN = 0x00	650	800	900	mV_{P-P}
		TXCN = 0x0F		900		mV_{P-P}
		TXCN = 0xF0		1100		mV_{P-P}
		TXCN = 0xFF		1300		mV_{P-P}
HS Differential Output Voltage, Non-Transition Bit	VOD_{NTR}	TXCN = 0x00	650	800	900	mV_{P-P}
		TXCN = 0x0F		900		mV_{P-P}
		TXCN = 0xF0		430		mV_{P-P}
		TXCN = 0xFF		600		mV_{P-P}
HS Generated Output Common Mode Voltage	V_{OCM}			2.35		V
HS Common Mode Serializer-Deserializer Voltage Difference	ΔV_{CM}			10	20	mV
HS Differential Output Impedance	R_{OUT}		80	100	120	Ω
HS Output Latency	t_{LPD}	Inherent in the design	4	7	10	PCLK
HS Output Rise and Fall Times	t_R/t_F	20% to 80%		150		ps
HS Differential Skew	t_{SKEW}			<10		ps
HS Output Random Jitter	t_{RJ}	PCLK_IN = 45MHz		6		ps_{rms}
HS Output Deterministic Jitter	t_{DJ}	PCLK_IN = 45MHz		25		ps_{P-P}
HIGH SPEED RECEIVER						
HS Differential Input Voltage	V_{ID}		75			mV_{P-P}
HS Generated Input Common Mode Voltage	V_{ICM}			2.32		V
HS Differential Input Impedance	R_{IN}		80	100	120	Ω
HS Maximum Jitter Tolerance				0.50		UI_{P-P}

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FN6870.0
March 16, 2009

Electrical Specifications Unless otherwise indicated, all data is for: VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, T_A = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C						
I²C Clock Rate (on SCL)	f_{I2C}			100	400	kHz
I²C Clock Pulse Width (HI or LO)			1.3			µs
I²C Clock Low to Data Out Valid			0		1	µs
I²C Start/Stop Setup/Hold Time			0.6			µs
I²C Data in Setup Time			100			ns
I²C Data in Hold Time			100			ns
I²C Data out Hold Time			100			ms

NOTES:

3. IDDIO is nominally 50µA and not included in this total as it is dominated by the loading of the parallel pins

4. This parameter is the output data skew from the invalid edge of PCLK_OUT. The setup and hold time provided to a system is dependent on the PCLK frequency and is calculated as follows: $0.5 * f_{IN} - t_{DV}$.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
		SERIALIZER	DESERIALIZER
47 to 40, 9 to 2	RGBA[7:0], RGBC[7:0]	Parallel video data LVCMOS inputs with Hysteresis	Parallel video data LVCMOS outputs
16	HSYNC	Horizontal (line) Sync LVCMOS input with Hysteresis	Horizontal (line) Sync LVCMOS output
17	VSYNC	Vertical (frame) Sync LVCMOS input with Hysteresis	Vertical (frame) Sync LVCMOS output
15	DATAEN	Video Data Enable LVCMOS input with Hysteresis	Video Data Enable LVCMOS output
20	PCLK_IN	Pixel clock LVCMOS input	PLL reference clock LVCMOS input
39	PCLK_OUT	Default; not used	Recovered clock LVCMOS output
33, 32	SERIOP, SERION	High speed differential serial I/O	High speed differential serial I/O
18	VHSYNCPOL	CMOS input for HSYNC and VSYNC Polarity 1: HSYNC & VSYNC active low 0: HSYNC & VSYNC active high	
19	VIDEO_TX	CMOS input for video flow direction 1: video serializer 0: video deserializer	
24, 23	SDA, SCL (Note 5)	I²C Interface Pins (I²C DATA, I²C CLK)	
25, 26	I2CA[1:0] (Note 5)	I²C Device Address	
27	MASTER	I²C Master Mode 1: Master 0: Slave	
12	RSTB/PDB	CMOS input for Reset and Power-down. For normal operation, this pin must be forced high. When this pin is forced low, the device will be reset. If this pin stays low, the device will be in PD mode.	
10	STATUS	CMOS output for Receiver Status: 1: Valid 8b/10b data received 0: otherwise Note: serializer and deserializer switch roles during side-channel reverse traffic	
28	REF_RES	Analog bias setting resistor connection; use 3.16kΩ ±1% to ground	

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION	
		SERIALIZER	DESERIALIZER
21	GND_P (Note 6)	PLL Ground	
37, 48	GND_IO (Note 6)	Digital (Parallel and Control) Ground	
35	GND_CDR (Note 6)	Analog (Serial) Data Recovery Ground	
31	GND_TX (Note 6)	Analog (Serial) Output Ground	
29	GND_AN (Note 6)	Analog Bias Ground	
13	GND_CR (Note 6)	Core Logic Ground	
14	VDD_CR	Core Logic VDD	
34	VDD_TX	Analog (Serial) Output VDD	
30	VDD_AN	Analog Bias VDD	
36	VDD_CDR	Analog (Serial) Data Recovery VDD	
1, 38	VDD_IO (Note 5)	Digital (Parallel and Control) VDD	
22	VDD_P	PLL VDD	
11	TEST_EN	Must be connected to ground	
Exposed Pad	Exposed Pad	Must be connected to ground	

NOTES:

5. Pins with the same name are internally connected together. However, this connection must NOT be used for connecting together external components or features.

6. The various differently-named Ground pins are internally weakly connected. They must be tied together externally. The different names are provided to assist in minimizing the current loops involved in bypassing the associated supply VDD pins. In particular, for ESD testing, they should be considered a common connection

Thin Plastic Quad Flatpack Exposed Pad Plastic Packages (EPTQFP)

TOP VIEW

PIN 1

BOTTOM VIEW
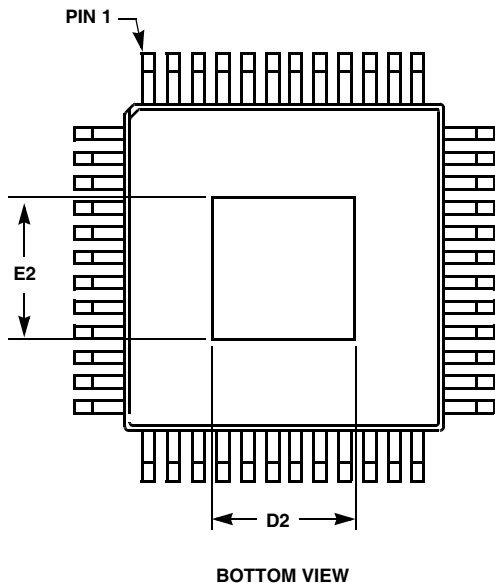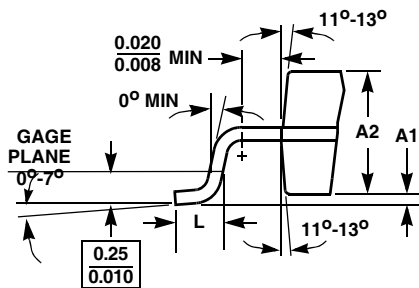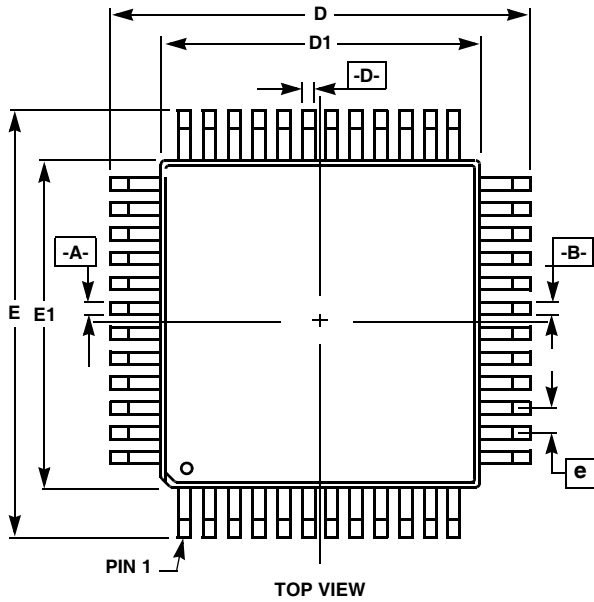
Q48.7X7B (JEDEC MS-026ABC-HU ISSUE D)
48 LEAD THIN PLASTIC QUAD FLATPACK EXPOSED PAD PACKAGE

SYMBOL	MILLIMETERS		NOTES
	MIN	MAX	
A	-	1.20	-
A1	0.05	0.15	-
A2	0.95	1.05	-
b	0.17	0.27	6
b1	0.17	0.23	-
D	8.80	9.20	3
D1	6.90	7.10	4, 5
D2	3.90	4.10	-
E	8.80	9.20	3
E1	6.90	7.10	4, 5
E2	3.90	4.10	-
L	0.45	0.75	-
N	48		7
e	0.50 BSC		-

Rev. 1 9/08

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

2. All dimensions and tolerances per ANSI Y14.5M-1982.

3. Dimensions D and E to be determined at seating plane -C-.

4. Dimensions D1 and E1 to be determined at datum plane -H-.

5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.

6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).

7. "N" is the number of terminal positions.