Data Sheet | December 15, 2008 | FN6827.0

WSVGA 24-Bit Long-Reach Video SERDES with Bi-directional Side-Channel

The ISL34341 is a serializer/deserializer of LVCMOS parallel video data. The video data presented to the serializer on the parallel LVCMOS bus is serialized into a high-speed differential signal. This differential signal is converted back to parallel video at the remote end by the deserializer. It also transports auxiliary data bi-directionally over the same link during the video vertical retrace interval.

I^2C bus mastering allows the placement of external slave devices on the remote side of the link. An I^2C controller can be placed on either side of the link allowing bi-directional I^2C communication through the link to the external devices on the other side. Both chips can be fully configured from a single controller or independently by local controllers.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL34341INZ*	ISL34341INZ	-40 to +85	64 Ld EPTQFP	Q64.10x10C

*Add “-T13” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

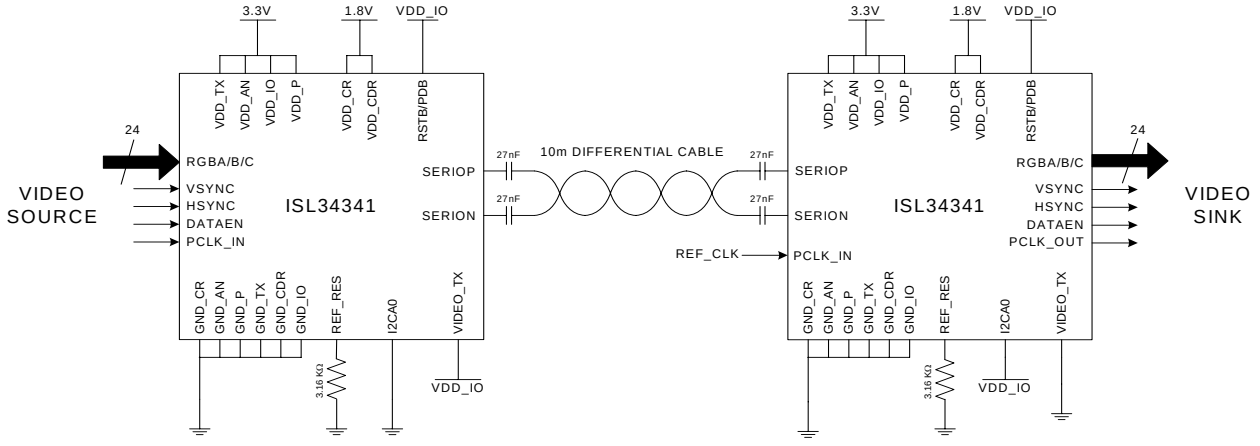
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- 24-bit RGB transport over single differential pair
- 6MHz to 40MHz pixel clock rates
- Bi-directional auxiliary data transport without extra bandwidth and over the same differential pair
- I^2C Bus Mastering to the remote side of the link with a controller on either the serializer or deserializer
- 40MHz PCLK transports
  - SVGA 800x600 @ 70fps, 16% blanking
  - WSVGA 1024x600 @ 60fps, 8% blanking
- Internal 100Ω termination on high-speed serial lines
- DC balanced with industry standard 8b/10b line code allows AC-coupling
  - Provides immunity against ground shifts
- Hot plugging with automatic resynchronization every line
- 16 programmable settings each for transmitter amplitude boost and pre-emphasis and receiver equalization allow for longer cable lengths and higher data rates
- Programmable power-down of the transmitter and the receiver
- Same device for serializer and deserializer simplifies inventory
- I^2C communication interface
- 8kV ESD rating for serial lines
- Pb-free (RoHS compliant)

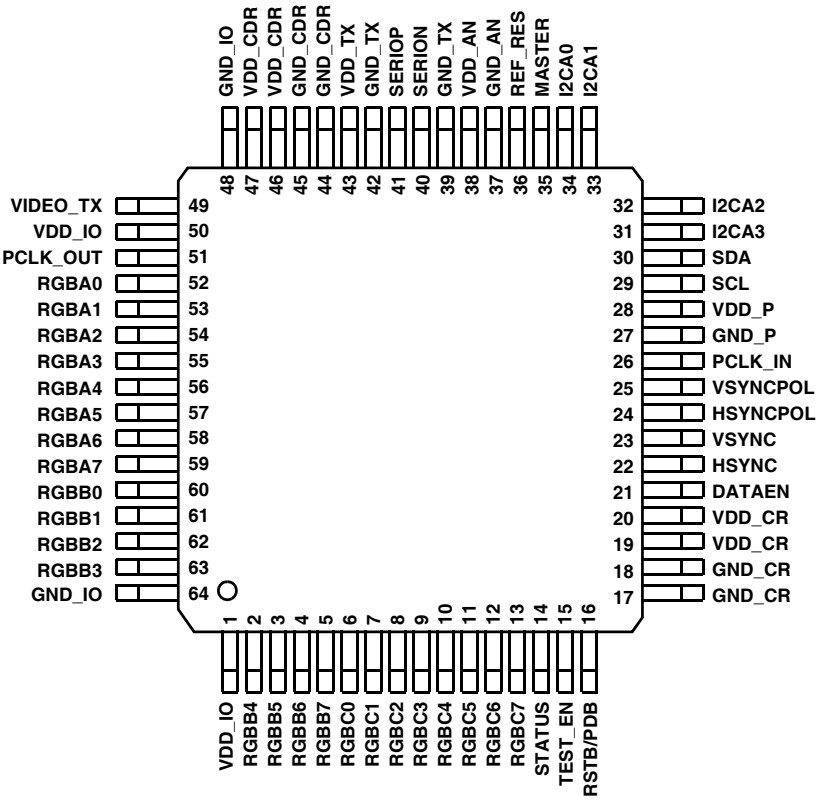
Applications

- Navigation and display systems
- Video entertainment systems
- Industrial computing terminals
- Remote cameras

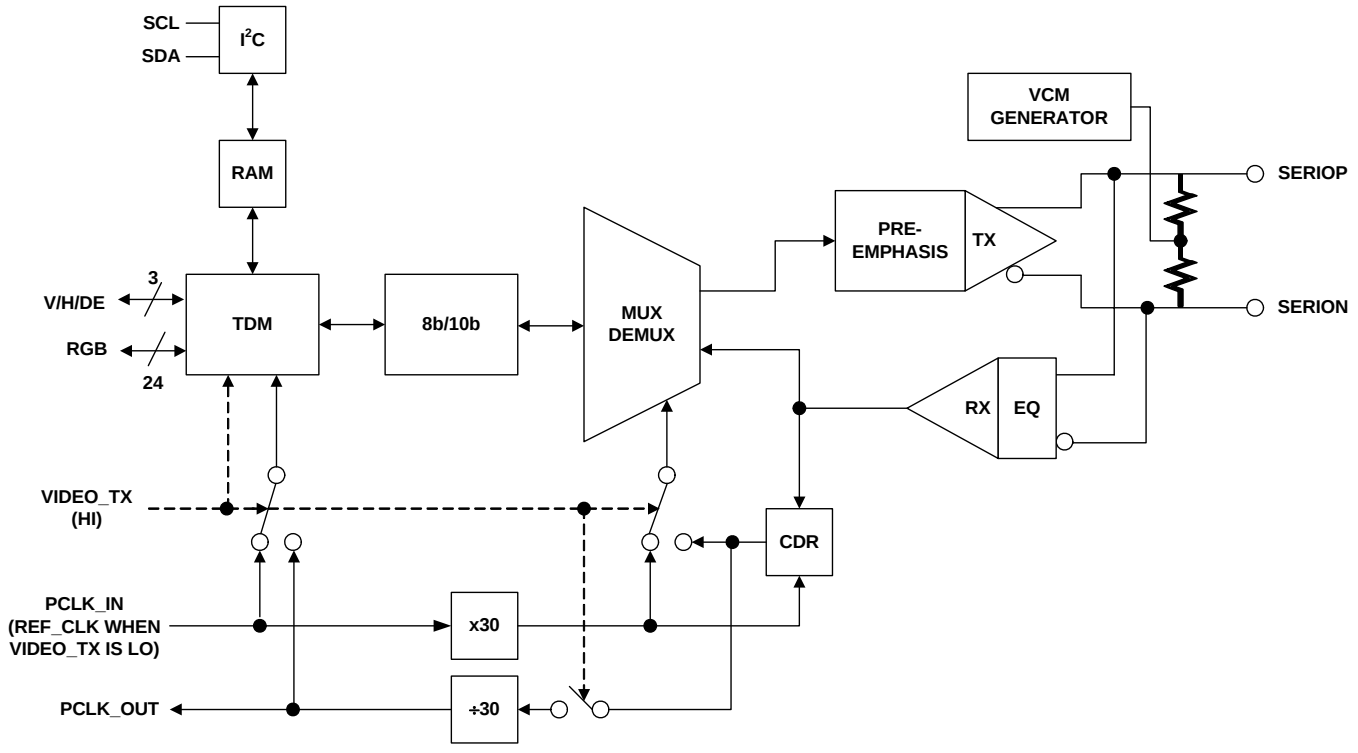


Pinout

ISL34341
(64 LD TQFP)
TOP VIEW



Block Diagram



Absolute Maximum Ratings

Supply Voltage
- VDD_P to GND_P, VDD_TX to GND_TX, VDD_IO to GND_IO . . . . . -0.5V to 4.6V
- VDD_CDR to GND_CDR, VDD_CR to GND_CR . . -0.5V to 2.5V
- Between any pair of GND_P, GND_TX, GND_IO, GND_CDR, GND_CR . . . . . -0.1V to 0.1V

3.3V Tolerant LVTTL/LVCMOS
- Input Voltage . . . . . .-0.3V to VDD_IO + 0.3V

Differential Input Voltage . . . . . .-0.3V to VDD_IO + 0.3V
Differential Output Current . . . . . .Short Circuit Protected
LVTTL/LVCMOS Outputs. . . . . .Short Circuit Protected
ESD Rating
- Human Body Model
  - All pins 4kV
  - SERIOP/N (all VDD Connected, all GND Connected) 8kV
- Machine Model. 200V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA}	θ_{JC} (°C/W)
EPTQFP.	33	4.5

Maximum Power Dissipation. 327mW
Maximum Junction Temperature . . . . . .+125°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Operating Temperature Range . . . . . .-40°C to +85°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise indicated, all data is for: VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, T_A = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE						
VDD_CDR, VDD_CR			1.7	1.8	1.9	V
VDD_TX, VDD_P, VDD_AN, VDD_IO			3.0	3.3	3.6	V
SERIALIZER POWER SUPPLY CURRENTS						
Analog TX Supply Current	I_{DDTX}	VIDEO_TX = 1 PCLK_IN = 40MHz		17		mA
Analog CDR Supply Current	I_{DDCDR}			57		mA
Digital I/O Supply Current	I_{DDIO}			1	2	mA
Digital Supply Current	I_{DDCR}			20		mA
PLL/VCO Supply Current	I_{DDP}			17		mA
Analog Bias Supply Current	I_{DDAN}			5.5		mA
Total 1.8V Supply Current				77	90	mA
Total 3.3V Supply Current				40	46	mA
DESERIALIZER POWER SUPPLY CURRENTS						
Analog TX Supply Current	I_{DDTX}	VIDEO_TX = 0 REF_CLK = 40MHz		24		mA
Analog CDR Supply Current	I_{DDCDR}			45		mA
Digital I/O Supply Current	I_{DDIO}			17	25	mA
Digital Supply Current	I_{DDCR}			32		mA
PLL/VCO Supply Current	I_{DDP}			17		mA
Analog Bias Supply Current	I_{DDAN}			5.4		mA
Total 1.8V Supply Current				77	90	mA
Total 3.3V Supply Current				64	80	mA

Electrical Specifications *Unless otherwise indicated, all data is for:* VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, T_A = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-DOWN SUPPLY CURRENT						
Total 1.8V Power-Down Supply Current		RSTB = GND; spec is per device		0.5		mA
Total 3.3V Power-Down Supply Current				1		mA
PARALLEL INTERFACE						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}		-10	±0.01	10	µA
High Level Output Voltage	V_{OH}	I_{OH} = -2.0mA, VDD_IO = 3V	0.8*VDD_IO			V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0mA, VDD_IO = 3V			0.2*VDD_IO	V
Output Short Circuit Current	I_{OSC}				50	mA
Output Rise and Fall Times	t_{OR}/t_{OF}	Slew rate control set to min, C_L = 8pF		1		ns
		Slew rate control set to max, C_L = 8pF		4		ns
SERIALIZER PARALLEL INTERFACE						
PCLK_IN Frequency	f_{IN}		6		40	MHz
PCLK_IN Duty Cycle	t_{IDC}		40	50	60	%
Parallel Input Setup Time	t_{IS}		3.6			ns
Parallel Input Hold Time	t_{IH}		1.6			ns
DESERIALIZER PARALLEL INTERFACE						
PCLK_OUT Frequency	f_{OUT}		6		40	MHz
PCLK_OUT Duty Cycle	t_{ODC}			50		%
PCLK_OUT Period Jitter (rms)	t_{OJ}	Clock randomizer off		0.5		$\%t_{PCLK}$
PCLK_OUT Spread Width	t_{OSPRD}	Clock randomizer on		±20		$\%t_{PCLK}$
Time to Parallel Output Data Valid	t_{DV}	Relative to PCLK_OUT	-4.7		5.5	ns
Deserializer Output Latency	t_{CPD}	Part-to-part, side-channel disabled	4	9	14	PCLK
DESERIALIZER REFERENCE CLOCK (REF_CLK IS FED INTO PCLK_IN)						
REF_CLK Lock Time	t_{PLL}			100		µs
REF_CLK to PCLK_OUT Maximum Frequency Offset		PCLK_OUT is the recovered clock	1500	5000		ppm
HIGH-SPEED TRANSMITTER						
HS Differential Output Voltage, Transition Bit	VOD_{TR}	TXCN = 0x00	600	825	990	mV_{P-P}
		TXCN = 0x0F		1170		mV_{P-P}
		TXCN = 0xF0		975		mV_{P-P}
		TXCN = 0xFF		1300		mV_{P-P}
HS Differential Output Voltage, Non-Transition Bit	VOD_{NTR}	TXCN = 0x00	600	825	990	mV_{P-P}
		TXCN = 0x0F		460		mV_{P-P}
		TXCN = 0xF0		975		mV_{P-P}
		TXCN = 0xFF		600		mV_{P-P}

Electrical Specifications *Unless otherwise indicated, all data is for:* VDD_CDR = VDD_CR = 1.8V, VDD_IO = 3.3V, VDD_TX = VDD_P = VDD_AN = 3.3V, T_A = +25°C, Ref_Res = 3.16kΩ, High-speed AC-coupling capacitor = 27nF. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HS Generated Output Common Mode Voltage	V_{OCM}			2.35		V
HS Common Mode Serializer-Deserializer Voltage Difference	ΔV_{CM}			20	120	mV
HS Differential Output Impedance	R_{OUT}		80	100	120	Ω
HS Output Latency	t_{LPD}	Part-to-part	4	7	10	PCLK
HS Output Rise and Fall Times	t_R/t_F	20% to 80%		150		ps
HS Differential Skew	t_{SKEW}			<10		ps
HS Output Random Jitter	t_{RJ}			13.4		ps_{rms}
HS Output Deterministic Jitter	t_{DJ}			40		ps_{P-P}
HIGH SPEED RECEIVER						
HS Differential Input Voltage	V_{ID}		150			mV_{P-P}
HS Generated Input Common Mode Voltage	V_{ICM}			2.32		V
HS Differential Input Impedance	R_{IN}		80	100	120	Ω
HS Maximum Jitter Tolerance				0.52		UI_{P-P}
I^2C						
I^2C Clock Rate (on SCL)	f_{I2C}			100	400	kHz
I^2C Clock Pulse Width (HI or LO)			1.3			µs
I^2C Clock Low to Data Out Valid			0		1	µs
I^2C Start/Stop Setup/Hold Time			0.6			µs
I^2C Data in Setup Time			100			ns
I^2C Data in Hold Time			100			ns
I^2C Data out Hold Time			100			ms

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
		SERIALIZER	DESERIALIZER
52 to 63, 2 to 13	RGBA[7:0], RGBB[7:0], RGBC[7:0]	Parallel video data LVCMOS inputs	Parallel video data LVCMOS outputs
22	HSYNC	Horizontal (line) Sync LVCMOS input	Horizontal (line) Sync LVCMOS output
23	VSYNC	Vertical (frame) Sync LVCMOS input	Vertical (frame) Sync LVCMOS output
21	DATAEN	Video Data Enable LVCMOS input	Video Data Enable LVCMOS output
26	PCLK_IN	Pixel clock LVCMOS input	PLL reference clock LVCMOS input
51	PCLK_OUT	Default; not used	Recovered clock LVCMOS output
41, 40	SERIOP, SERION	High speed differential serial I/O	High speed differential serial I/O
24	HSYNCPOL	CMOS input for HSYNC 1: HSYNC is active low 0: HSYNC is active high	
25	VSYNCPOL	CMOS input for VSYNC 1: VSYNC is active low 0: VSYNC is active high	

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION	
		SERIALIZER	DESERIALIZER
49	VIDEO_TX	CMOS input for video flow direction 1: video serializer 0: video deserializer	
29, 30	SCL, SDA	I^2C Interface Pins (I^2C DATA, I^2C CLK)	
31 to 34	I2CA[3:0]	I^2C Device Address	
35	MASTER	I^2C Master Mode 1: Master 0: Slave	
16	RSTB/PDB	CMOS input for Reset and Power-down. For normal operation, this pin must be forced high. When this pin is forced low, the device will be reset. If this pin stays low, the device will be in PD mode.	
14	STATUS	CMOS output for Receiver Status: 1: Valid 8b/10b data received 0: otherwise Note: serializer and deserializer switch roles during side-channel reverse traffic	
36	REF_RES	Analog bias setting resistor connection; use 3.16kΩ ±1% to ground	
27	GND_P	PLL Ground	
48, 64	GND_IO	Digital (Parallel and Control) Ground	
44, 45	GND_CDR	Analog (Serial) Data Recovery Ground	
39, 42	GND_TX	Analog (Serial) Output Ground	
37	GND_AN	Analog Bias Ground	
17, 18	GND_CR	Core Logic Ground	
19, 20	VDD_CR	Core Logic VDD	
43	VDD_TX	Analog (Serial) Output VDD	
38	VDD_AN	Analog Bias VDD	
46, 47	VDD_CDR	Analog (Serial) Data Recovery VDD	
1, 50	VDD_IO	Digital (Parallel and Control) VDD	
28	VDD_P	PLL VDD	
15	TEST_EN	Must be connected to ground	
Exposed Pad	Exposed Pad	Must be connected to ground	

NOTES:

3. Pins with the same name are internally connected together. However, this connection must NOT be used for connecting together external components or features.
4. The various differently-named Ground pins are internally weakly connected. They must be tied together externally. The different names are provided to assist in minimizing the current loops involved in bypassing the associated supply VDD pins. In particular, for ESD testing, they should be considered a common connection.

Diagrams

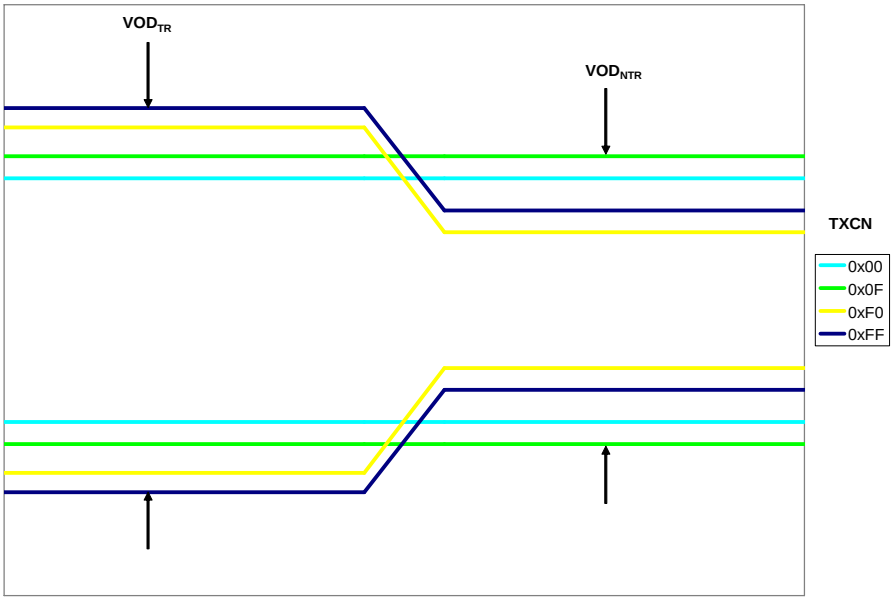


FIGURE 1. VOD vs TXCN SETTING

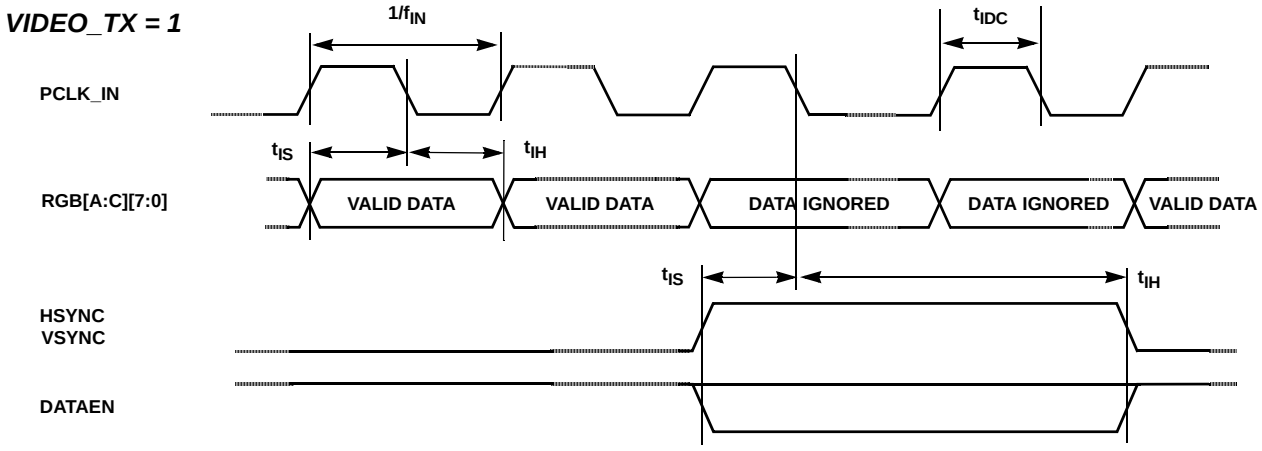


FIGURE 2. PARALLEL VIDEO INPUT TIMING [HSYNCPOL = 0, VSYNCPOL = 0, PCLKPOL (reg) = 0]

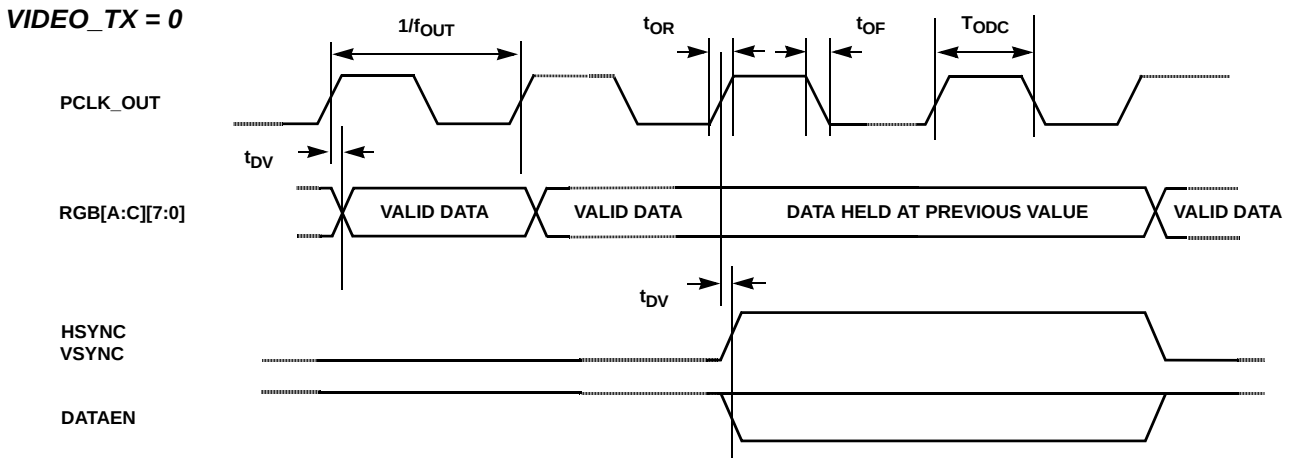


FIGURE 3. PARALLEL VIDEO OUTPUT TIMING [HSYNCPOL = 0, VSYNCPOL = 0, PCLKPOL (reg) = 0]

Applications

Overview

A pair of ISL34341 SERDES transports 24-bit parallel video (16-bit parallel video for the ISL34321) along with auxiliary data over a single 100Ω differential cable either to a display or from a camera. Auxiliary data is transferred in both directions and can be used for remote configuration and telemetry.

The benefits include lower EMI, lower costs, greater reliability and space savings. The same device can be configured to be either a serializer or deserializer by setting one pin (VIDEO_TX), simplifying inventory. RGBA/B/C, VSYNC, HSYNC, and DATAEN pins are inputs in serializer mode and outputs in deserializer mode.

The video data presented to the serializer on the parallel LVCMOS bus is serialized into a high-speed differential signal. This differential signal is converted back to parallel video at the remote end by the deserializer. The Side Channel data is transferred between the SERDES pair during two lines of the vertical video blanking interval.

When the side-channel is enabled, there will be a number of PCLK cycles uncertainty from frame-to-frame. This should not cause sync problems with most displays, as this occurs during the vertical front porch of the blanking period. When properly configured, the SERDES link supports end-to-end transport with fewer than one error in 10^{10} bits.

Differential Signals and Termination

The ISL34341 serializes the 24-bit parallel data along with 3 sync signals at 30x the PCLK_IN frequency. The ISL34321 serializes the 16-bit parallel data plus 3 sync signals at 20x the PCLK_IN frequency. The extra 2 bits per word come from the 8b/10b encoding scheme which helps create the highest quality serial link.

The high bit rate of the differential serial data requires special care in the layout of traces on PCBs, in the choice and assembly of connectors, and in the cables themselves.

PCB traces need to be adjacent and matched in length (so as to minimize the imbalanced coupling to other traces or elements) and of a geometry to match the impedance of the transmitter and receiver to minimize reflections. Similar care needs to be applied to the choice of connectors and cables.

SERIOP and SERION pins incorporate internal differential termination of the serial signal lines.

SERIO Pin AC-Coupling

AC-coupling minimizes the effects of DC common mode voltage difference and local power supply variations between two SERDES. The serializer outputs DC balanced 8b/10b line code, which allows AC-coupling.

The AC-coupling capacitor on SERIO pins must be 27nF on the serializer board and 27nF on the deserializer board. The value of the AC-coupling capacitor is very critical since a value too small will attenuate the high speed signal at low clock rate. A value too big will slow down the turn around time for the side-channel.

Receiver Reference Clock (REF_CLK)

The reference clock (REF_CLK) for the PLL is fed into PCLK_IN pin. REF_CLK is used to recover the clock from the high speed serial stream. REF_CLK is very sensitive to any instability. The following conditions must be met at all times after power is applied to the deserializer, or else the deserializer may need a manual reset:

- REF_CLK frequency must be within the limits specified
- REF_CLK amplitude must be stable.

A simple 3.3V CMOS crystal oscillator can be used for REF_CLK.

Power Supply Sequencing

The 3.3V supply must be higher than the 1.8V supply at all times, including during power-up and power-down. To meet this requirement, the 3.3V supply must be powered up before the 1.8V supply.

For the deserializer, REF_CLK must not be applied before the device is fully powered up. Applying REF_CLK before power-up may require the deserializer to be manually reset. A 10ms delay after the 1.8V supply is powered up guarantees normal operation.

Power Supply Bypassing

The serializer and deserializer functions rely on the stable functioning of PLLs locked to local reference sources or locked to an incoming signal. It is important that the various supplies (VDD_P, VDD_AN, VDD_CDR, VDD_TX) be well bypassed over a wide range of frequencies, from below the typical loop bandwidth of the PLL to approaching the signal bit rate of the serial data. A combination of different values of capacitors from 1000pF to 5µF or more with low ESR characteristics is generally required.

The parallel LVCMOS VDD_IO supply is inherently less sensitive, but since the RGB and SYNC/DATAEN signals can all swing on the same clock edge, the current in these pins and the corresponding GND pins can undergo substantial current flow changes, so once again, a combination of different values of capacitors over a wide range, with low ESR characteristics, is desirable.

A set of arrangements of this type is shown in Figure 4, where each supply is bypassed with a ferrite-bead-based choke, and a range of capacitors. A “choke” is preferable to an “inductor” in this application, since a high-Q inductor will be likely to cause one or more resonances with the shunt capacitors. This potentially causes problems at or near those frequencies, while a “lossy” choke will reflect a high impedance over a wide frequency range.

The higher value capacitor, in particular, needs to be chosen carefully with special care regarding its ESR. Very good results can be obtained with multilayer ceramic capacitors, available from many suppliers, and generally in small outlines (such as the 1210 outline suggested in the schematic shown in Figure 4), which provide good bypass capabilities down to a few mΩ at 1MHz to 2MHz. Other capacitor technologies may also be suitable (perhaps niobium oxide), but “classic” electrolytic capacitors frequently have ESR values of above 1Ω, that nullify any decoupling effect above the 1kHz to 10kHz frequency range.

Capacitors of 0.1µF offer low impedance in the 10MHz to 20MHz region, and 1000pF capacitors in the 100MHz to 200MHz region. In general, one of the lower value capacitors should be used at each supply pin on the IC. Figure 4 shows the grounding of the various capacitors to the pin corresponding to the supply pin. Although all the ground supplies are tied together, the PCB layout should be arranged to emulate this arrangement, at least for the smaller value (high frequency) capacitors, as much as possible.

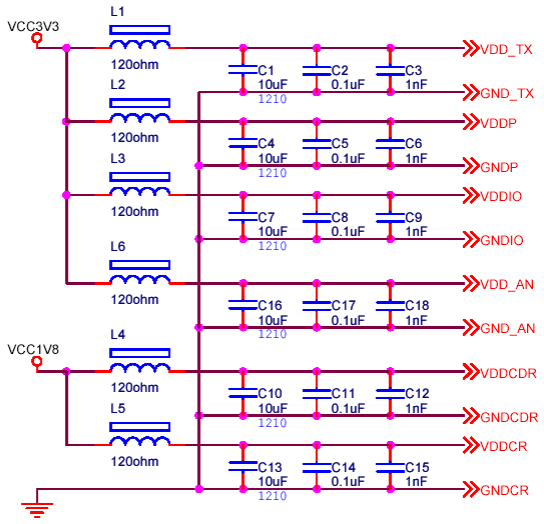


FIGURE 4. POWER SUPPLY BYPASSING

I^2C Interface

The I^2C interface allows access to internal registers used to configure the SERDES and to obtain status information. A serializer must be assigned a different address than its deserializer counterpart. The upper 3 bits are permanently set to 011 and the lower 4 bits determined by pins as follows:

0	1	1	I2CA3	I2CA2	I2CA1	I2CA0	R/$\overline{W}$

Thus, 16 SERDES can reside on the same bus. By convention, when all address pins are tied low, the device address is referred to as 0x60.

SCL and SDA are open drain to allow multiple devices to share the bus. If not used, SCL and SDA should be tied to VDD_IO.

Side Channel Interface

The Side Channel is a mechanism for transferring data between the two chips on each end of the link. This data is transferred during video blanking so none of the video bandwidth is used. It has three basic uses:

- Data exchanges between two processors
- Master Mode I^2C commands to remote slaves
- Remote SERDES configuration

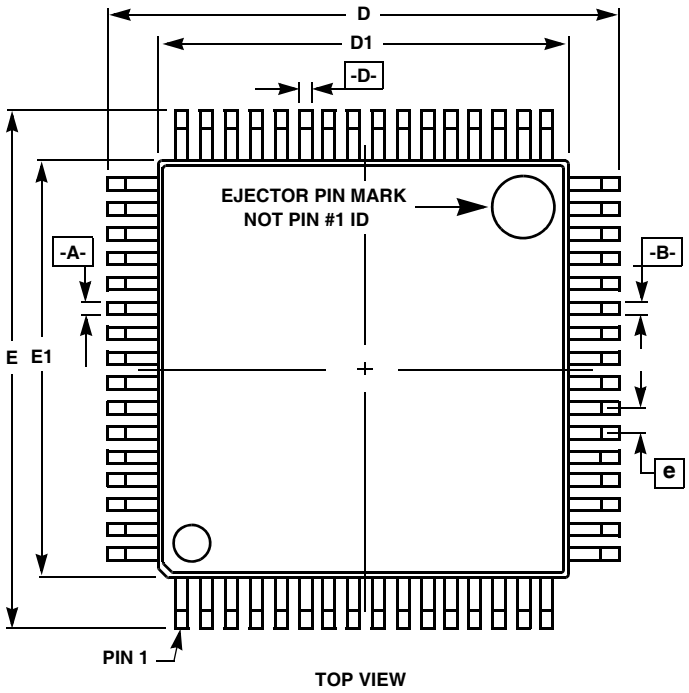
This interface allows the user to initialize registers, control and monitor both SERDES chips from a single micro-controller which can reside on either side of the serial link. This feature is used to automatically transport the remote side chip’s status which is available in a local register. The Side Channel needs to be enabled for this to work which is the default mode. In the case where there is a

micro-controller on each side of the of the link data can be buffered and exchanged between the two. Up to 224 bytes can be sent in each direction during each VSYNC active period.

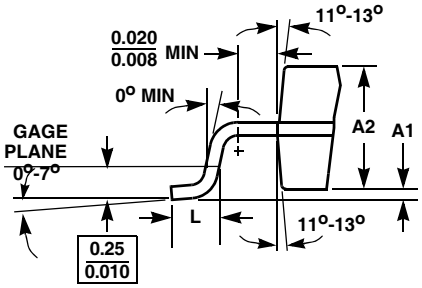
Master Mode

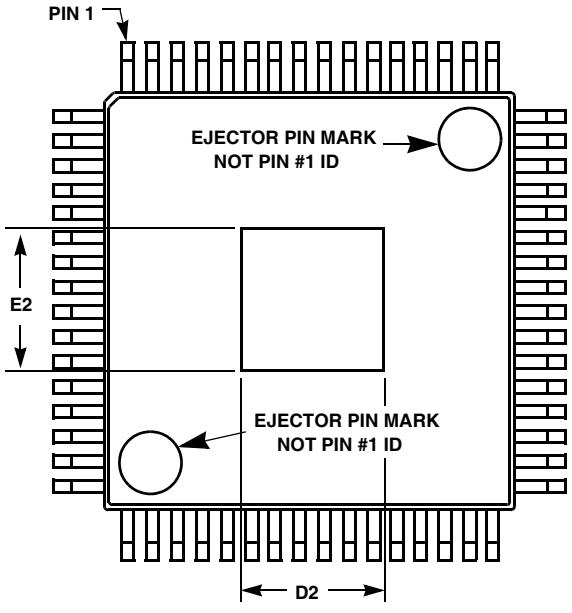
This is a mode activated by strapping the MASTER pin to a '1' on the 34341 on the remote side of the controller. This is a virtual extension of the I^2C interface across the link that allows the local processor to read and write slave devices connected to the remote side I^2C bus. No additional wires or components are needed other than the serial link. The I^2C commands and data are transferred during video blanking causing no interruptions in the video data. Data is transported by the Side Channel across the link so the maximum throughput would be the same.

Thin Plastic Quad Flatpack Exposed Pad Plastic Packages (EPTQFP)



TOP VIEW





BOTTOM VIEW

Q64.10x10C (JEDEC MS-026ACD-HU ISSUE D)
64 LEAD THIN PLASTIC QUAD FLATPACK EXPOSED PAD PACKAGE

SYMBOL	MILLIMETERS		NOTES
	MIN	MAX	
A	-	1.20	-
A1	0.05	0.15	-
A2	0.95	1.05	-
b	0.16	0.28	6
b1	0.17	0.23	-
D	11.80	12.20	3
D1	9.90	10.10	4, 5
D2	2.90	3.10	-
E	11.80	12.20	3
E1	9.90	10.10	4, 5
E2	2.90	3.10	-
L	0.45	0.75	-
N	64		7
e	0.50 BSC		-

Rev. 0 10/08

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. "N" is the number of terminal positions.