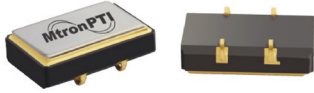
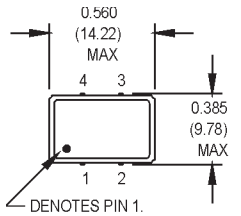


M5RJ Series

9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator



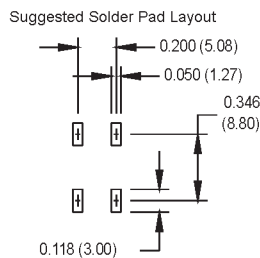
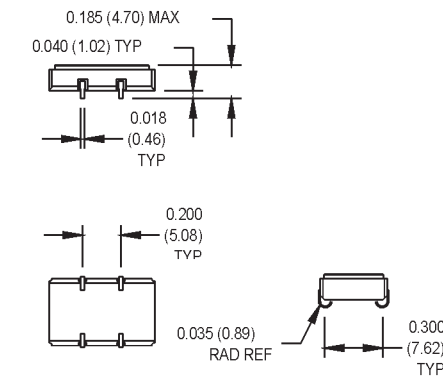
- Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz
- Ideal for 10 and 40 Gigabit Ethernet and Optical Carrier applications



FREQUENCY RANGE	AVAILABLE OUTPUT TYPES
19.440 to 170.000 MHz	Z, E, R
170.000 to 250 MHz	S, U

Ordering Information	
Product Series	M5RJ 1 8 Z Q J -R 00.0000 MHz
Temperature Range	1: 0°C to +70°C 2: -40°C to +85°C 6: -20°C to +70°C 7: -0°C to +85°C 8: 0°C to +50°C
Stability	3: ±100 ppm 4: ±50 ppm 5: ±35 ppm 6: ±25 ppm 8: ±20 ppm
Output Type	E: Complementary, pins 1 & 4, enable (enabled w/pin 2 low) R: Complementary, pins 1 & 4, enable (enabled w/pin 2 high) S: Complementary, pins 4 & 5, enable (enabled w/pin 2 low) U: Complementary, pins 4 & 5 Z: Complementary, pins 1 & 3
*Symmetry/Output Logic Type	P: 45/55% PECL Q: 40/60% PECL
Package/Lead Configurations	J: J-lead
RoHS Compliance	Blank: non-RoHS compliant part -R: RoHS compliant part Frequency (customer specified)

* Contact the factory regarding LVDS output availability
M2003Sxxx - Contact factory for datasheet.



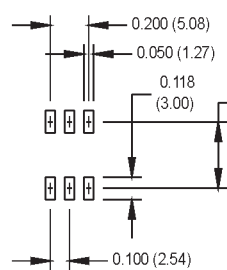
Pin Connections (Z, E, and R Output Types)

FUNCTION	4 Pin	6 Pin
Output/Q	1	1
Enable		2
Ground/Cover	2	3
Output Q	3	4
N/C		5
+Vcc	4	6

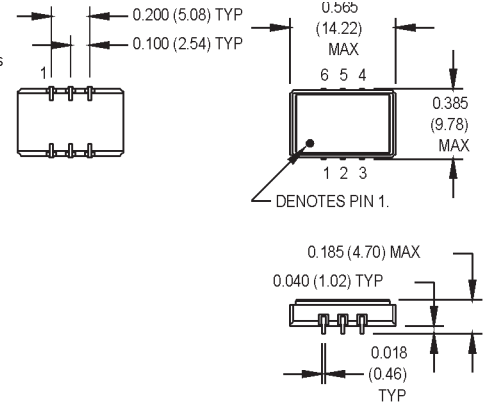
Pin Connections (S and U Output Types)

PIN	FUNCTION
1	N/C
2	N/C or Enable
3	Ground/Cover
4	Output Q
5	Output/Q
6	+Vcc

SUGGESTED SOLDER PAD LAYOUT



All dimensions in inches (mm).



PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	19.44		250	MHz	See Note 1
Operating Temperature	T _A					(See ordering information)
Storage Temperature	T _s	-55		+125	°C	
Frequency Stability	ΔF/F					(See ordering information)
Aging						See Note 2
1st Year			±2		ppm	
Thereafter (per year)			±1		ppm	
Input Voltage	V _{cc}	3.135	3.3	3.465	V	
Supply Current	I _{cc}			75	mA	<150 MHz
	I _{cc}			85	mA	>150 MHz
Output Type						LVPECL/LVDS
Load						50 Ohms to V _{cc} - 2.0 V Or Thevenin equivalent
Symmetry (Duty Cycle)						PECL load @ V _{cc} -1.3 VDC
Output Skew				200	ps	PECL
Differential Voltage		250	350	450	mV	LVDS
Logic "1" Level	V _{oh}	V _{cc} -1.02			V	PECL
Logic "0" Level	V _{ol}			V _{cc} -1.63	V	PECL
Rise/Fall Time	T _r /T _f		0.50	0.55	ns	@ 20/80% LVPECL
				1.0	ns	@ 20/80% LVDS
Enable Function						PECL low: output active PECL high: output disables 80% V _{cc} min or N/C: output active 20% V _{cc} max: output disables to high-Z
						"E" & "S" output types
						"R" output types
Start up Time				10	ms	
Phase Jitter	φ _J					
Below 75 MHz				1.5	ps RMS	Integrated 12 kHz - 20 MHz
75 MHz & above				1.0	ps RMS	Integrated 12 kHz - 20 MHz
Mechanical Shock		MIL-STD-202, Method 213, C (100 g's)				
Vibration		MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)				
Thermal Cycle		MIL-STD-883, Method 1010, B (-55°C to +125°C, 15 min dwell, 10 cycles)				
Hermeticity		MIL-STD-202, Method 112				
Solderability		Per EIAJ-STD-002				
Max Soldering Conditions		See solder profile, Figure 1				

1. Consult factory for exact frequency availability.
2. Calibration, deviation over temperature, shock, vibration and aging.
3. PECL load - see Load Circuit Diagram #5. LVDS load - see load circuit diagram #9.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

MtronPTI Lead Free Solder Profile

