CADEKA
Amplify the Human Experience

SPT7852

DUAL 10-BIT, 20 MSPS, 160 mW A/D CONVERTER

FEATURES

- Dual 10-Bit/20 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Internal Track-and-Hold
- Low Power Dissipation: 160 mW
- 4 Vp-p Analog Input Range for Each ADC
- Single +5 Volt Power Supply
  with Option for 3.3 V Digital Outputs
- Tri-State, TTL-Compatible Outputs
- Overrange Bit
- Selectable Two's Complement or Straight Binary Output

APPLICATIONS

- Video Set-Top Boxes
- Cellular Base Stations
- QPSK/QAM RF Demodulation
- S-Video Digitizers
- Composite Video Digitizers
- Portable and Handheld Instrumentation

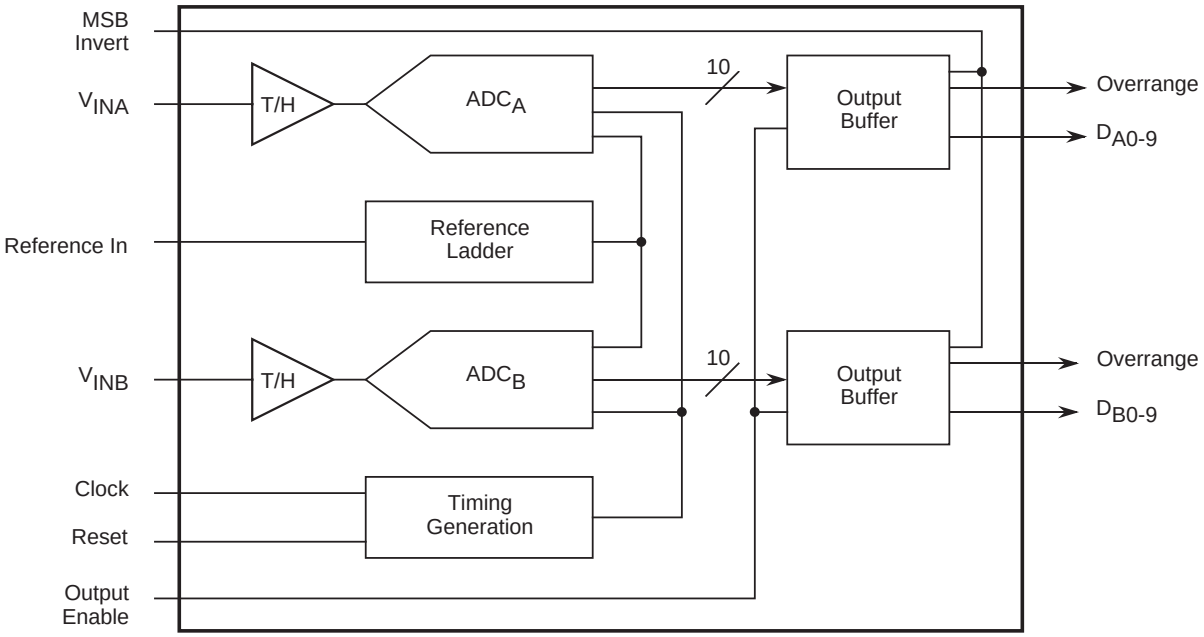
GENERAL DESCRIPTION

The SPT7852 has two 10-Bit CMOS analog-to-digital converters that can sample data at speeds up to 20 MSPS. It has excellent low noise performance with a very low typical power dissipation of only 160 mW—that's the total power for *both* converters. The SPT7852 uses a dual configuration of the proprietary circuit design found in our 10-bit CMOS single converter family, to achieve its high performance in a CMOS process.

The SPT7852 is specifically designed for video decoding applications and is ideal for S-video decoding and decoding of multiple composite video sources. It also has excellent application in the area of coherent I/Q demodulation in such applications as QAM demodulation and TV set-top box converters.

Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS-logic systems. Output data format is selectable for either straight binary or two's complement. The SPT7852 is available in a 44L TQFP package in commercial and industrial temperature ranges. It is also available in die form. For availability of extended temperature ranges, please contact the factory.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... –0.5 V to AV_{DD} +0.5 V
V_{Ref} ..... –1.5 V to AV_{DD} +0.8 V
CLK Input ..... V_{DD}
$AV_{DD} – DV_{DD}$ ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS FOR EACH CHANNEL

$T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +5.0 V, V_{IN} =0 to 4 V, f_S =20 MSPS, f_{CLK} =40 MHz, V_{RHS} =4.0 V, V_{RLS} =0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		IV		±1.0		LSB
Differential Nonlinearity		IV		±1.0		LSB
Analog Input						
Input Voltage Range		V	V_{RLS}		V_{RHS}	V
Input Resistance		V	50			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	Full Power	V		35		MHz
Offset		VI		±2.0		LSB
Gain Error		VI		±2.0		LSB
Reference Input						
Resistance	$V_{RHS} – V_{RLS}$	VI	350	425	500	Ω
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
$V_{RHS} – V_{RLS}$		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} – V_{RHS})$		V		150		mV
$\Delta(V_{RLS} – V_{RLF})$		V		150		mV
Conversion Characteristics						
Maximum Conversion Rate[1]		VI	20			MHz
Minimum Conversion Rate[1]		IV			100	kHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		15		ps
Dynamic Performance						
Effective Number of Bits						
f_{IN}=3.58 MHz		VI	8.4	8.9		Bits
f_{IN}= 10 MHz		VI	7.9	8.4		Bits

[1]2X Clock required.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD}$ = +5.0 V, V_{IN} =0 to 4 V, f_S =20 MSPS, f_{CLK} =40 MHz, V_{RHS} = 4.0 V, V_{RLS} =0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=3.58 MHz		VI	53	57		dB
f_{IN}=10 MHz		VI	52	56		dB
Harmonic Distortion						
f_{IN}=3.58 MHz		VI	56	59		dB
f_{IN}=10 MHz		VI	52	54		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=3.58 MHz		VI	52	55		dB
f_{IN}=10 MHz		VI	49	52		dB
Channel-to-Channel Crosstalk	f_{IN}=3.58 MHz	IV		70		dB
Channel-to-Channel Gain Matching	Full Scale	IV		0.04		dB
Spurious Free Dynamic Range	f_{IN}=3.58 MHz @ –3 dB FS	V		66		dB
Differential Phase		V		0.2		Degree
Differential Gain		V		0.3		%
Digital Inputs						
Logic "1" Voltage		VI	2.0			V
Logic "0" Voltage		VI			0.8	V
Maximum Input Current Low	V_{IL}=0 V	VI	–10		+10	µA
Maximum Input Current High	V_{IH}=5 V	VI	–10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	I_{OH}=0.5 mA	VI	OV_{DD}–0.5			V
Logic "0" Voltage	I_{OS}=1.6 mA	VI			0.4	V
t_{RISE}/t_{FALL}	15 pF Load	V		10		ns
Output Enable to Data Output Delay	20 pF Load, T_A=+25 °C	V		10		ns
	50 pF Load Over Temp.	V		22		ns
Power Supply Requirements						
Voltages DV_{DD}		IV	4.75	5.0	5.25	V
AV_{DD}		IV	4.75	5.0	5.25	V
OV_{DD}		IV	2.7	5.0	5.25	V
Currents AI_{DD}	Total for Both Converter	VI		15	18	mA
DI_{DD}	Channels	VI		17	20	mA
Power Dissipation		VI		160	190	mW

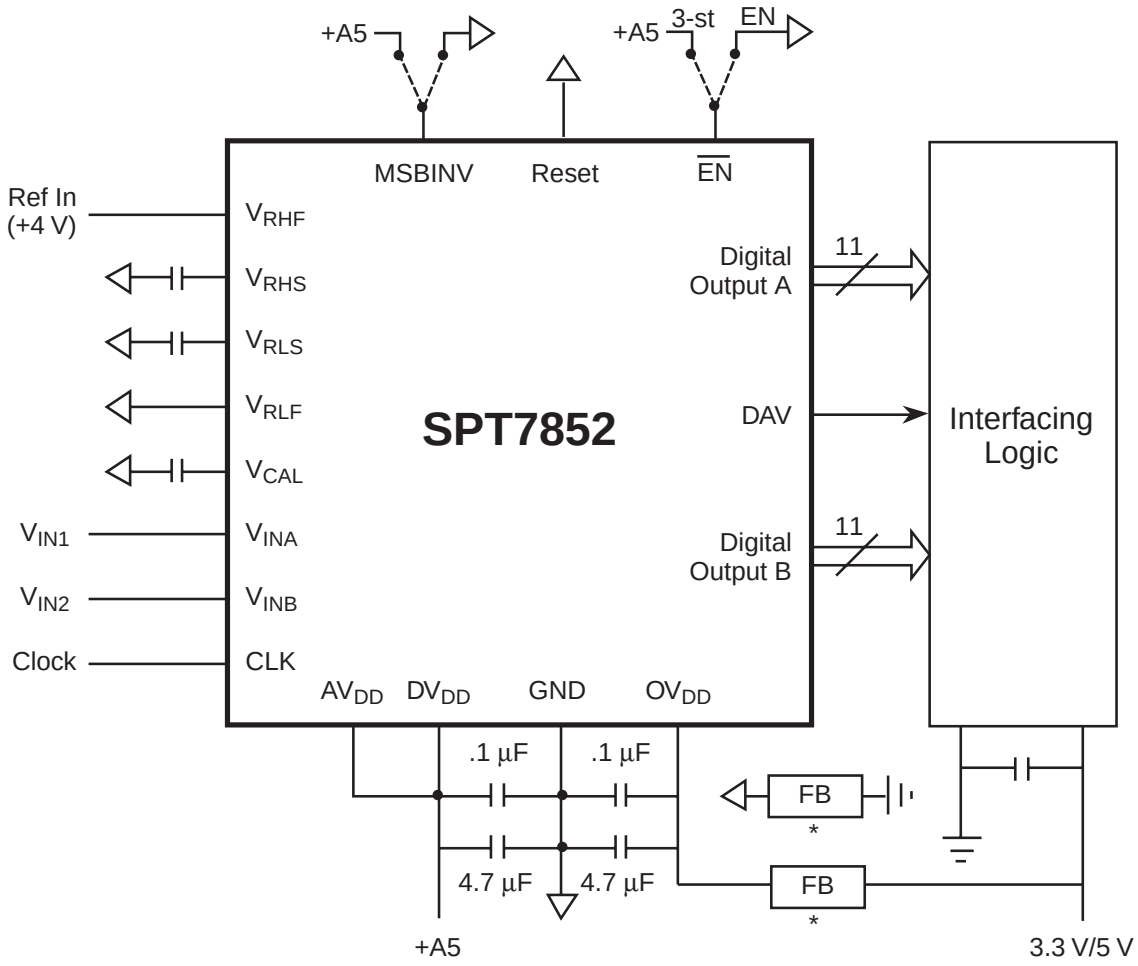
TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=+25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 –Typical Interface Circuit



1. Place the ferrite bead (*) as close to the ADC as possible.
2. Place 0.1 µF decoupling capacitors as close to the ADC as possible.
3. All capacitors are 0.1 µF surface-mount unless otherwise specified.
4. All analog input pins (references, analog input, clock input) must be protected. (See absolute maximum ratings.)

TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 1 shows the typical interface requirements when using the SPT7852 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

CADEKA suggests that both the digital and the analog supply voltages on the SPT7852 be derived from a single analog supply as shown in figure 1. A separate digital supply must be used for all interface circuitry. CADEKA suggests using this power supply configuration to prevent a possible latch-up condition on powerup.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains two sets of eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

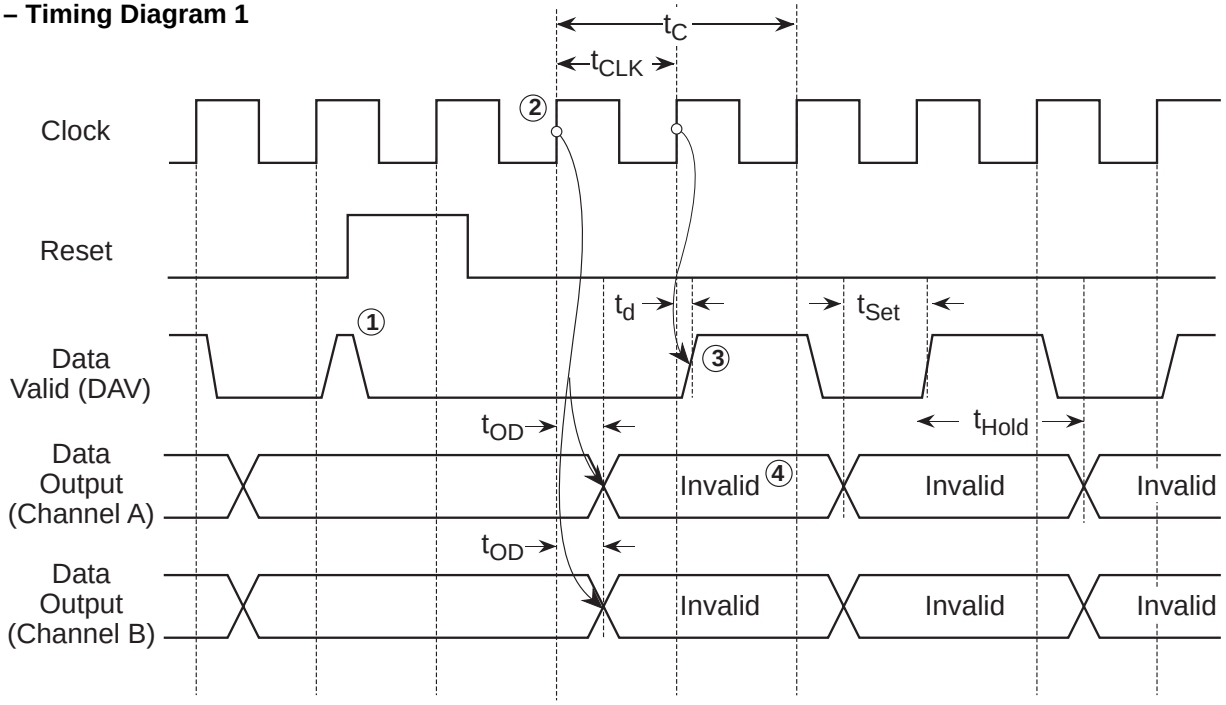
Table I – Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5–15	11-bit SAR conversion
16	Data transfer

The 16-phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 40 MHz clock rate, the input sample rate is 20 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only sixteen comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparator's response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator per V_{IN} input samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

Figure 2 – Timing Diagram 1



Notes:
1) Data Valid is forced low on Reset = High.
2) Data updated on first rising edge of clock after Reset goes low.
3) Data Valid rising edge will occur on the second rising edge of Clock after Reset goes low. Use the rising edge of Data Valid to latch the ADC output data.
4) Analog Input Data is sampled during the first clock cycle after Reset goes low. Valid data output from this sample will be available 12 clock cycles later (6 Data Valid cycles). All data during the 12 clock cycle latency is invalid.

CLOCK INPUT

The SPT7852 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. **The device's sample rate is 1/2 of the input clock frequency. (See timing diagram.)**

TIMING AND RESET FUNCTION

The two on-board ADCs in the SPT7852 are driven off of a single external TTL clock. This external clock must be 2X the desired sample rate. In applications that require a known phase relationship between the clock, analog input sampling and valid data output, a reset function is provided to establish a known phase relationship. (Because of the 2X clock, an exact phase relationship will not be known otherwise.) Refer to figure 2, Timing Diagram 1.

The reset pin is low for normal device operation. When reset is brought high, Data Valid (DAV) is immediately forced low and data output updates are suspended. Operation will resume on the first rising edge of the clock after the reset pin has been brought low. The first Data Valid rising edge will occur on the second edge of the clock after the reset goes low.

The first analog input sample will be taken during the first clock cycle after reset goes low. Valid data from this sample will be available 12 clock cycles later. All data during this 12 cycle latency will be invalid (Refer to figure 3, Timing Diagram 2.)

Figure 3 – Timing Diagram 2

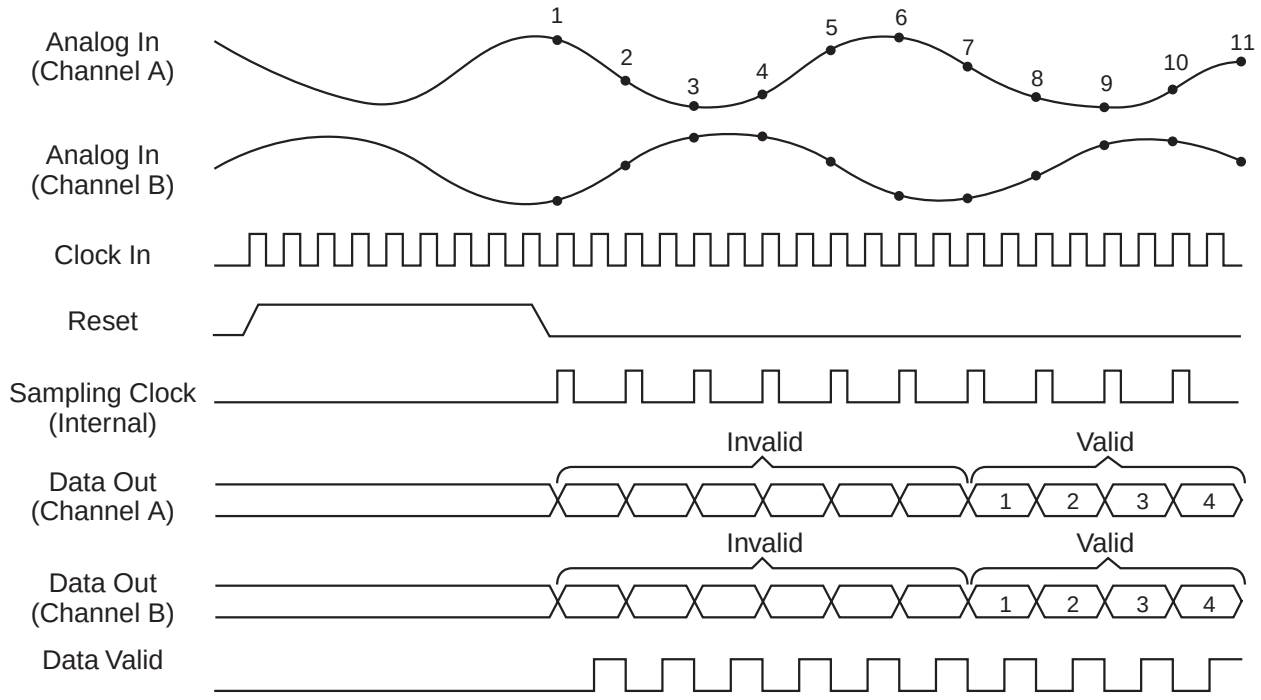
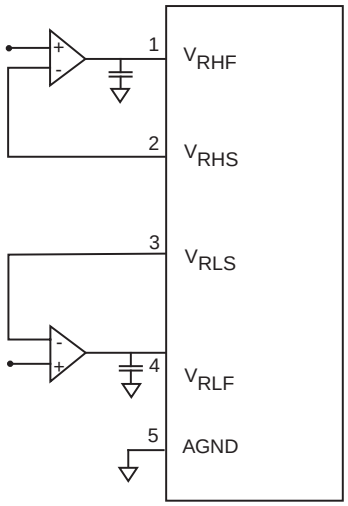


Table II – Timing Parameters Table

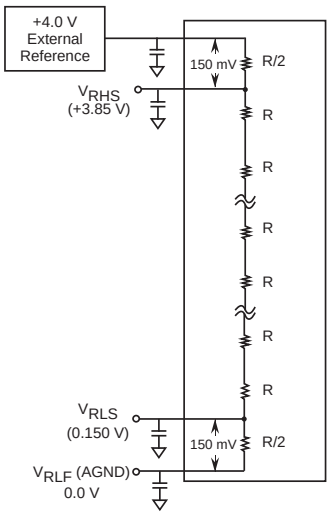
DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	$2*t_{CLK}$			ns
Clock Period	t_{CLK}	25			ns
Clock Duty Cycle		40	50	60	%
Output Delay (15 pF Load)	t_{OD}		11		ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to DAV	t_d		15		ns
Data Set Up Time	t_{Set}	22			
Data Hold Time	t_{Hold}	28			

Figure 4 – Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 5 – Simplified Reference Ladder Drive Circuit Without Force/Sense Circuit



R=30 Ω (typ)
All capacitors are 0.01 µF

VOLTAGE REFERENCE

The SPT7852 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. Both ADCs share the same reference ladder. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 4, offset and gain errors of less than ±2 LSB can be obtained.

In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 5. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 5 is a simplified representation of the actual reference ladder with force and sense taps shown. Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} – V_{RHS}$ = 3.75% of ($V_{RHF} – V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} – V_{RLF}$ = 3.75% of ($V_{RHF} – V_{RLF}$) (typical).

Figure 5 shows an example of expected voltage drops for a specific case. V_{Ref} of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 150 mV drop is seen at V_{RHS} (= 3.85 V) and a 150 mV increase is seen at V_{RLS} (= 0.150 V).

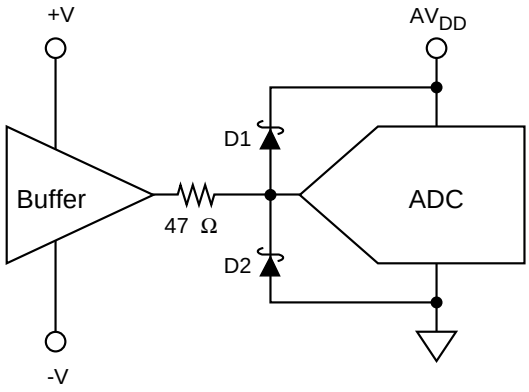
ANALOG INPUT

V_{INA} and V_{INB} are the analog inputs for channel A and channel B, respectively. Both channels share the same reference ladder. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7852's extremely low input capacitance of only 5 pF and very high input resistance of 50 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 6.

Figure 6 – Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

CALIBRATION

The SPT7852 uses an auto-calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

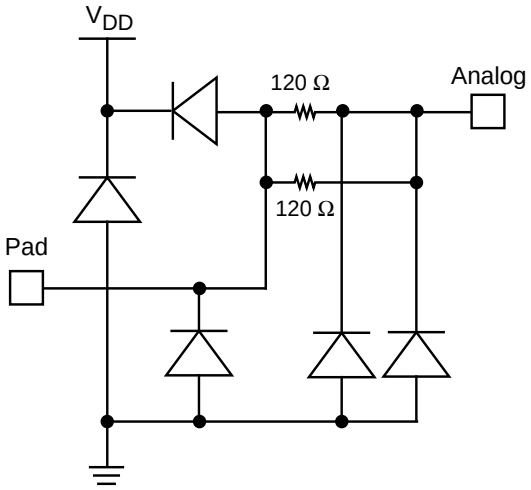
Upon powerup, the SPT7852 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon powerup of 250 µsec (for a 20 MHz sample rate). Once calibrated, the SPT7852 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7852 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 7. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 7 – On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

DIGITAL OUTPUTS, DATA VALID, AND MSB INVERT

The output data for both channels can be latched using the rising edge of Data Valid (DAV). Refer to table II for minimum data setup and hold times. The format of the data is straight binary when the MSB Invert pin (MSBINV) is held low and Two's Complement format when MSB Invert is high.

OVERRANGE OUTPUT

An OVERRANGE OUTPUT from D10A or D10B is an indication that the analog input signal has exceeded the positive full-scale input voltage by 1 LSB. When this condition occurs, D10A/B will switch to logic 1. All other data outputs (D0A/B to D9A/B) will remain at logic 1 as long as D10A/B remains at logic 1. This feature makes it possible to include the SPT7852 in higher resolution systems.

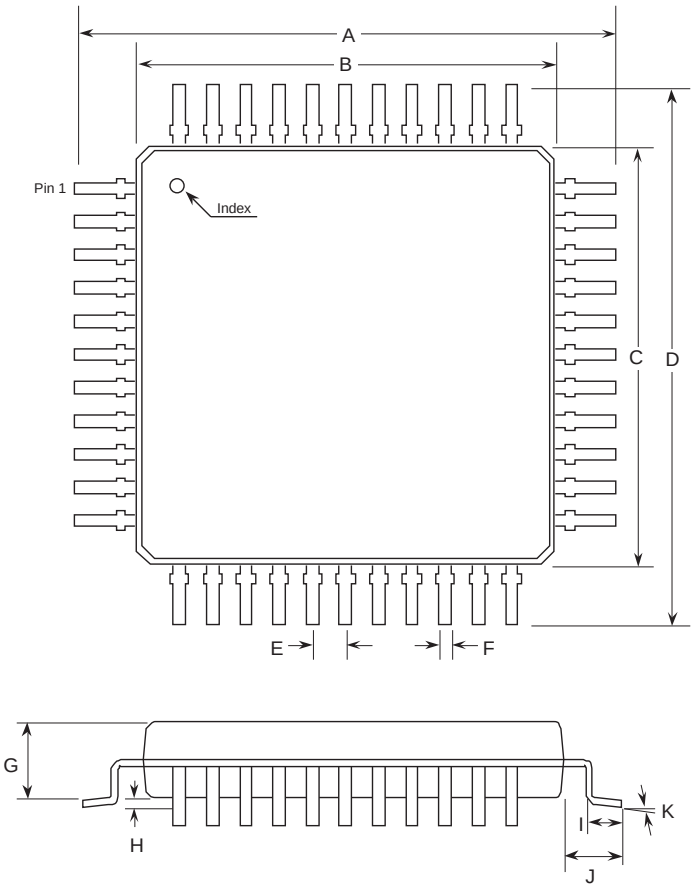
Table III – Output Data Information (Binary Code)

Analog Input	Overrange D10A/B	Output Code (MSBINV=0) D9A/B–D0A/B	Output Code (MSBINV=1) D9A/B–D0A/B
+FS + 1/2 LSB	1	11 1111 1111	01 1111 1111
+FS – 1/2 LSB	0	11 1111 111Ø	01 1111 111Ø
[+FS –(–FS)]/2	0	ØØ ØØØØ ØØØØ	ØØ ØØØØ ØØØØ
–FS + 1/2 LSB	0	00 0000 000Ø	10 0000 000Ø
–FS	0	00 0000 0000	10 0000 0000

Ø indicates the flickering bit between logic 0 and 1.
+FS = V_{RHS}; –FS = V_{RLS}

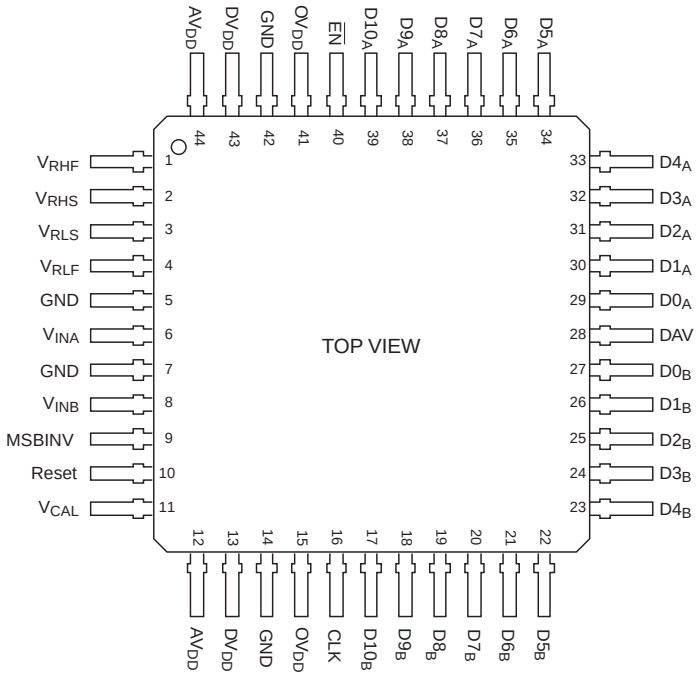
PACKAGE OUTLINE

44-LEAD TQFP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.472 Typ		12.00 Typ	
B	0.394 Typ		10.00 Typ	
C	0.394 Typ		10.00 Typ	
D	0.472 Typ		12.00 Typ	
E	0.031 Typ		0.80 Typ	
F	0.012	0.017	0.300	0.45
G	0.035	0.040	0.85	1.05
H	0.002	0.006	0.05	0.15
I	0.018	0.030	0.450	0.750
J	0.039 Typ		1.00 Typ	
K	0-7°		0-7°	

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{INA}	Channel A Analog Input
V_{INB}	Channel B Analog Input
AV_{DD}	Analog Power Supply
DV_{DD}	Digital Power Supply
OV_{DD}	Digital Output Supply (3.3 V/5 V)
GND	Common Device Ground
CLK	Input Clock ($f_{CLK} = 2 * f_S$)
$\overline{EN}$	Output Enable (Low = Data)
D0A – D9A	Channel A Tri-State Data Output (D0A = LSB)
D0B – D9B	Channel B Tri-State Data Output (D0B = LSB)
D10A	Channel A Overrange Bit
D10B	Channel B Overrange Bit
DAV	Data Valid Output
MSBINV	MSB Invert (High = 2's complement) (Low = binary)
Reset	Reset (Low = Normal) (High = Reset)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7852SCT	0 to +70 °C	44L TQFP
SPT7852SIT	–40 to +85 °C	44L TQFP
SPT7852SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.