Terawins, Inc.

***Release***
***Version 1.0***

*May 27, 2007*

# T108 Video Display Controller

# Contents

# 1 Introduction

## 1.1 Features

- **Cost Effective Highly Integrated Triple ADC + ITU656/601 Decoder + Digital RGB + 2D Video Decoder + OSD + Scaler + TCON + DAC + DC-to-DC + LED/CCFL controls**
  - Integrates 10-bit Triple Analog to Digital Converters (ADC) & Phase Locked Loop (PLL), for supporting CVBS, S-Video, YPbPr and RGB inputs
  - Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ration.
  - Requires no external Frame Buffer Memory for de-interlace.
  - ITU656/601_8/L601_16 Decoder with digital input ports for standard ITU656/601 input data.
  - Support digital RGB565 inputs
  - Advanced On Screen Display (OSD) function
  - Programmable Timing Controller (Tcon) for Car TV applications
  - Multi-standard color decoder with 2D adaptive comb filter
  - Innovative and flexible design to reduce total system cost
- **Triple 10-bits ADCs**
  - 80MSPS Conversion Rate ADC
  - Built-in Pre-amp, mid-level & ground clamp
  - Automatic Clamp Control for CVBS, Y and C
  - Programmable Static Gain Control or Automatic Gain Control for CVBS or Y/C
  - Max Input configuration up to 9xCVBS, 3xS-video+3xCVBS, 3YPbPr
  - Build-in Line-Lock PLL for RGB and YPbPr
  - Phases Tracking and Boundary for adjusting input quality.
- **Digital Video Enhancement**
  - Separate Luminance and Chroma Enhancer
  - Y Supports Luminance Black Level Extension., Contrast and Brightness adjustment
  - C Supports DCTI, Saturation and Hue adjustment.
- **FIR Based Advanced Scaling Engine**
  - Coefficient based sharpness filters
  - Independent vertical and horizontal scaling ratio
  - 16:9 Non-linear Aspect ratio
- **LCD Interface**
  - Provides 256-entry TBL Gamma correction for panel compensation
  - Supports image pan functions
  - Programmable Timing Controller
  - Built-in software adjustable VCOM voltage
  - RGB Triple DAC output
  - Integrated high efficiency DC-DC power conversion unit for gate and source drivers reduces energy consumption
  - Integrated TFT-LCD backlight inverter drive unit supports CCFL/LED typed backlight
  - Software adjustable lamp dimming
- **Built-in On Screen Display Engine**
  - 8K-word OSD1 memory
  - Supports text or bitmap modes
  - Supports character blinking and overlay functions
  - Fully programmable character mapping
  - Supports alpha blending & Zoom-in/Zoom-out function
  - Built-in 114+ fonts (18x12, 24x16 each)
  - Optional fonts stored in off-chip serial ROM
  - Optional Pattern-Filled background
- **Crystal Oscillator Circuit**
  - Direct interface to a (27.0MHz or other frequency) Crystal
  - Also provide a buffered clock output for external Micro-controller
- **Digital Test Pattern Generator**
  - Programmable standard & special panel burn-in test patterns
  - Support special border frame blocking mode
- **Independent Display Phase Lock Loop**
  - Generates pixel clock output to panel
  - Supports free run OSD mode
- **Serial Bus Interface**
  - Supports 2-wire $I^2C$ (Slave/Master)
- **Pulse Width Modulation Outputs**
- **Design For Testability**
  - Scan chain insertion
  - Separated analog & digital test modes
- **Power Supply: +1.8V, +3.3V and +5V**
- **Package: 100 pin LQFP**

## 1.2 General Description

The T108 is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T108 has built-in high performance Triple ADCs, TCON, triple DACs. Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative integrated "Frame-Buffer-Less" De-interlacer can significantly reduce system cost. The T108 also integrates enhanced two layer OSD engines. The device can interface to an external micro-controller through 2-wire serial bus interface.

## 1.3 Applications

1. Small to medium sized displayer, In-car TV
2. Progressive CRT TV
3. GPS mobile display application

## 1.4 System Architecture

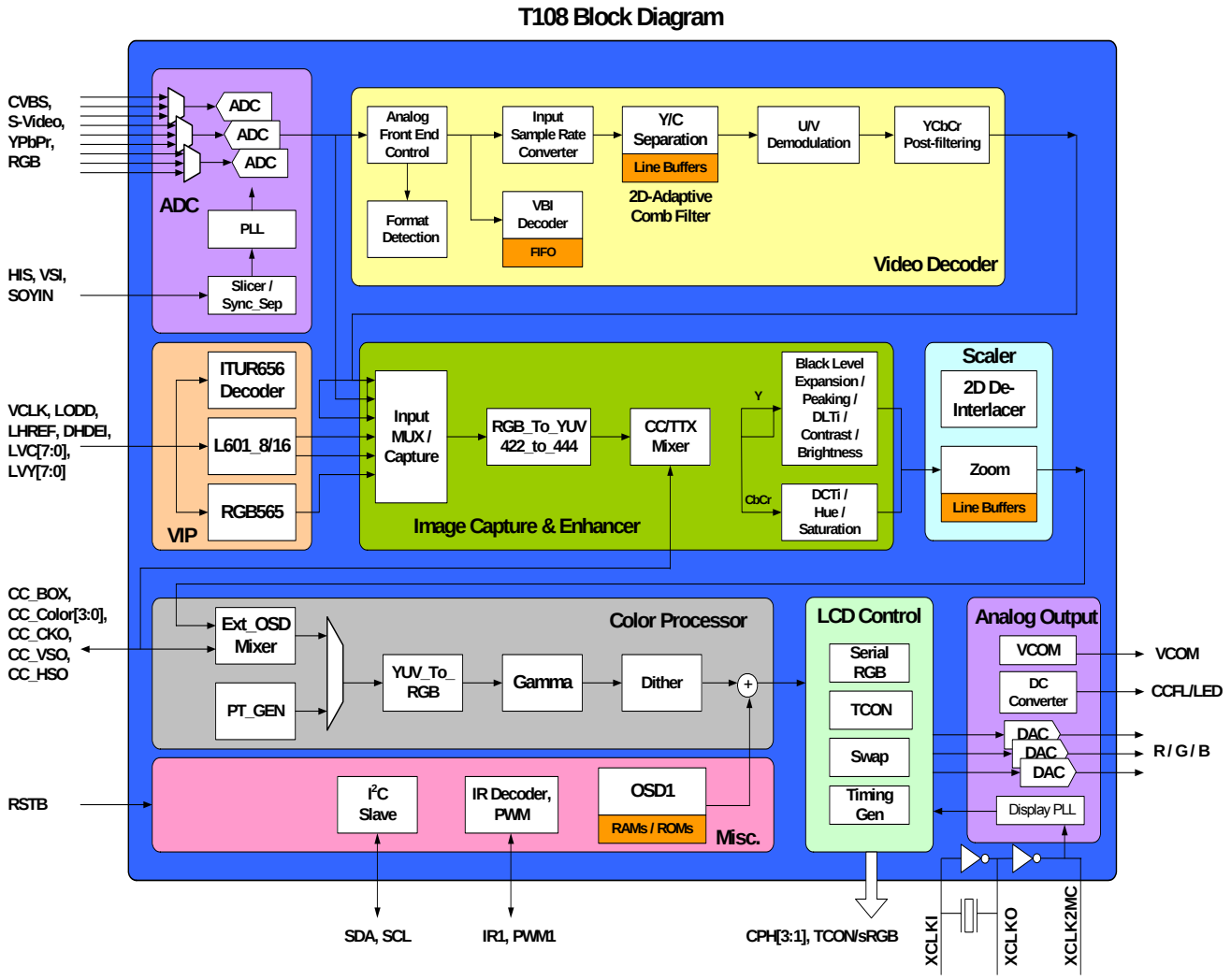



**Figure 1-1 System Architecture**

## 1.5 System Configurations

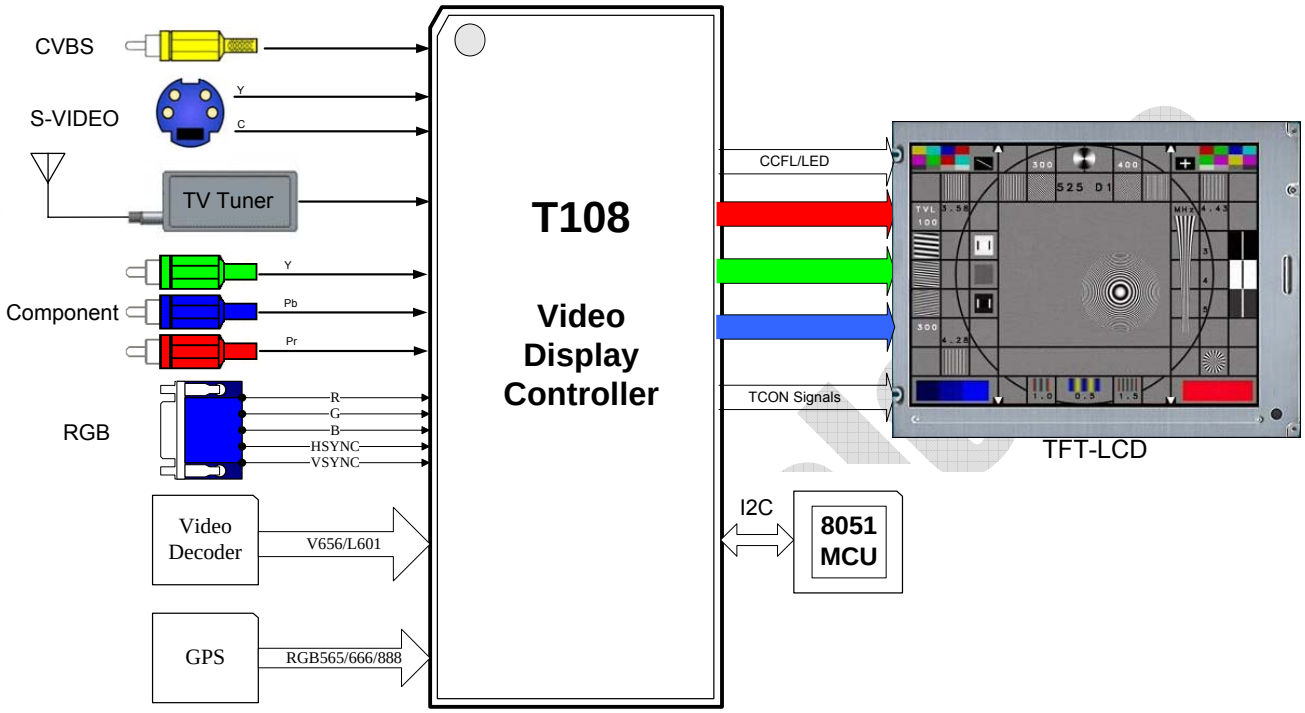



**Figure 1-2 System Configurations**

## 1.6 Pinout Diagram

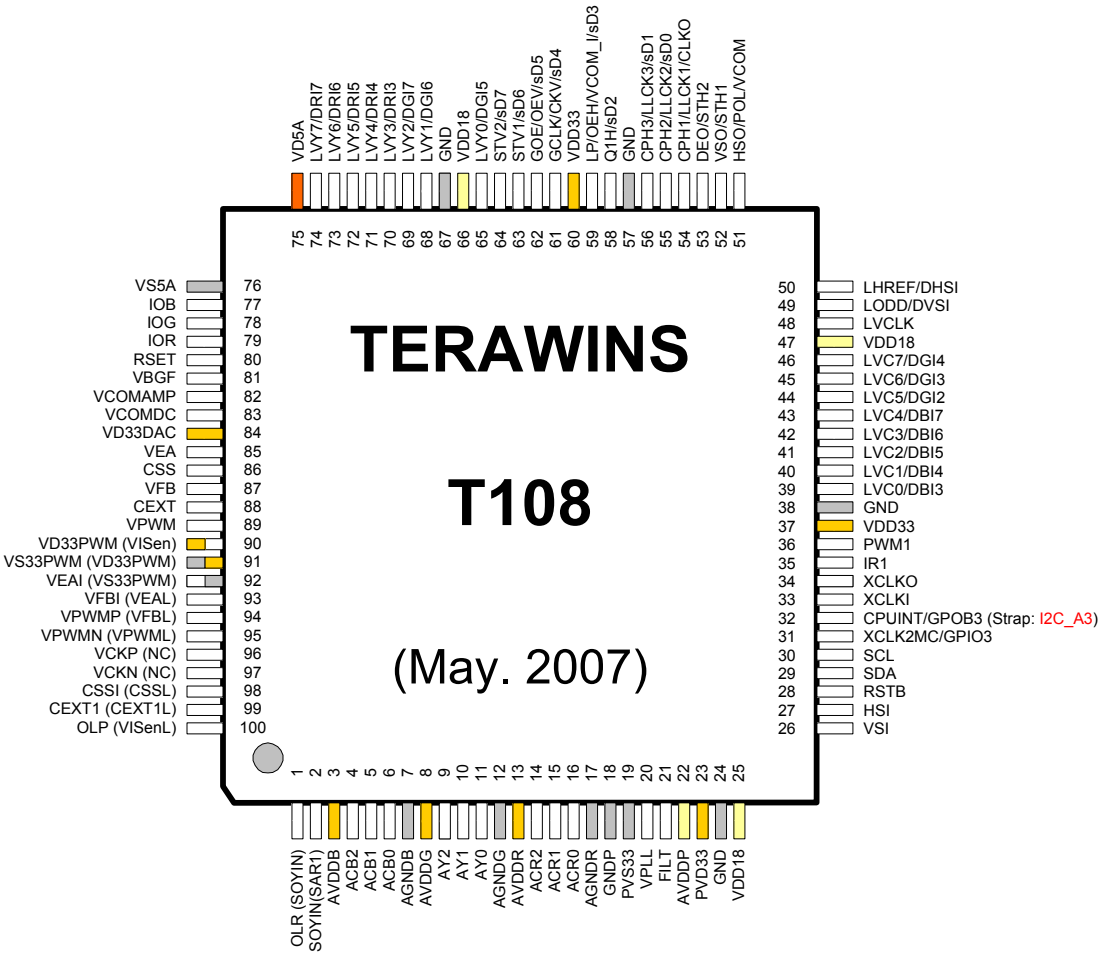



**Figure 1-3 Pinout Diagram**

**Pin 90-100, 1, 2: CCFL (LED) Backlight Pin Definitaion**

## 1.7 Pin Description

**Table 1-1 Pin Description**

| Symbol | Pin # | Type | Description |
|---|---|---|---|
| **Power Supplies** | | | |
| VDD18 | 25, 47, 66 | PWR | +1.8V digital core power supply |
| VDD33 | 37, 60 | PWR | +3.3V digital output power supply |
| AVDDB | 3 | PWR | +3.3V analog power supply for ADC channel 2 |
| AVDDG | 8 | PWR | +3.3V analog power supply for ADC channel 1 |
| AVDDR | 13 | PWR | +3.3V analog power supply for ADC channel 0 |
| VD5A | 75 | PWR | +5.0V analog power supply for DAC |
| VD33DAC | 84 | PWR | +3.3V analog power supply for DAC |
| VD33PWM | 90 or 91(LED) | PWR | +3.3V analog power supply for DC Converter |
| AVDDP | 22 | PWR | +1.8V analog power supply for PLL |
| PVD33 | 23 | PWR | +3.3V analog power supply for PLL |
| GND | 24, 38, 57, 67 | GND | Digital ground |
| AGNDB | 7 | GND | Analog ground for ADC channel 2 |
| AGNDG | 12 | GND | Analog ground for ADC channel 1 |
| AGNDR | 17 | GND | Analog ground for ADC channel 0 |
| VS5A | 76 | GND | Analog ground for DAC |
| VS33PWM | 91 or 92(LED) | GND | Analog ground for DC Converter |
| GNDP | 18 | GND | Analog ground for PLL |
| PVS33 | 19 | GND | Analog ground for PLL |
| **Output Interface Signals** | | | |
| IOR | 79 | AO | Channel R current output |
| IOG | 78 | AO | Channel G current output |
| IOB | 77 | AO | Channel B current output |
| VCOMAMP | 82 | AO | VCOM output |
| VCOMDC | 83 | AO | VCOM output |
| VCOM_i | 59 | DI, P/D | VCOM input |
| LLCk1 | 54 | DO, P/D | Output Data Clock |
| LLCk2 | 55 | DO, P/D | Output Data Clock |
| LLCk3 | 56 | DO, P/D | Output Data Clock |
| **Timing Controller Interface Signals** | | | |
| POL/VCOM | 51 | DO, P/D | Horizontal Polarity Output Signal. Share w/ HSO |
| STH1 | 52 | DO, P/D | Horizontal Start Pulse 1 Signal. Share w/ VSO |
| STH2 | 53 | DO, P/D | Horizontal Start Pulse 2 Signal. Share w/ DEO |
| Q1H | 58 | DO, P/D | Panel polarity control |
| LP/OEH | 59 | DO, P/D | Latch pulse for column driver |
| GCLK/CKV | 61 | DO, P/D | Gate driver clock |
| GOE/OEV | 62 | DO, P/D | Gate driver output enable |
| STV1 | 63 | DO, P/D | Gate driver start pulse |
| STV2 | 64 | DO, P/D | Gate driver start pulse |
| **Power Management Signals** | | | |
| VEA | 85 | AO | Error Amplifier output |
| CSS | 86 | AO | Soft Start |
| VFB | 87 | AI | Feedback of Lamp current |

| Symbol | Pin # | Type | Description |
|---|---|---|---|
| CEXT | 88 | AO | Switching frequency of DC-DC converter |
| VPWM | 89 | AO | PWM output, connect o external N-channel power MOSFET |
| VISen | 90(LED) | AI | Feedback of DC-DC current |
| VEAI/VEAL | 92/93 | AO | Error Amplifier output |
| VFBI/VFBL | 93/94 | AI | Feedback of Lamp current |
| VPWMP/VPWML | 94/95 | AO | PWM output, drive PMOSFET switch |
| VPWMN | 95(CCFL) | AO | PWM output, drive NMOSFET switch |
| VCKP/NC | 96 | AO | Clock output, drive PMOSFET switch |
| VCKN/NC | 97 | AO | Clock output, drive NMOSFET switch |
| CSSI/CSSL | 98 | AO | Soft Start |
| CEXT1/CEXT1L | 99 | AO | Switching frequency of Inverter |
| OLP/VISenL | 100 | AI | Open Lamp Protection/Current Limit |
| OLR | 1(CCFL) | AI | Open Lamp Regulation |
| **Serial Panel Interface Signals** | | | |
| VSO | 52 | DO, P/D | Vertical Synchronization Output Control Signal. Share w/ STH1 |
| HSO | 51 | DO, P/D | Horizontal Synchronization Output Control Signal. Share w/ POL/VCOM |
| DEO | 53 | DO, P/D | Horizontal Output Data Enable Signal. Share w/ STH2 |
| CLKO | 54 | DO, P/D | sPanel clock |
| sD0~sD7 | 55~56, 58~59, 61~64 | DO, P/D | sPanel data, share w/ TCON signals |
| **Configuration Interface Signals** | | | |
| RSTB | 28 | DI, P/U | Whole chip reset. |
| SDA | 29 | DIO, P/U | 2-wire serial bus data. Power down does not affect SDA. |
| SCL (SCANB) | 30 | DIO, P/U | 2-wire serial bus clock. Power down does not affect SCL. This pin should be high when RSTB asserted for avoid entering Scan test mode. |
| XCLK2MC | 31 | DO | Buffered XCLKI for external microprocessor. |
| CPUINT (A3) | 32 | DIO, P/U | Internal Interrupt.<br>This pin is a reset strap pin for $I^2C$ device address. When RSTB goes high, if this pin is high, then default $I^2C$ device address is 50h, else 40h. |
| **ADC, PLL, Slicer Interface** | | | |
| ACB2 | 4 | AI | Analog input 2 of channel 2 |
| ACB1 | 5 | AI | Analog input 1 of channel 2 |
| ACB0 | 6 | AI | Analog input 0 of channel 2 |
| AY2 | 9 | AI | Analog input 2 of channel 1 |
| AY1 | 10 | AI | Analog input 1 of channel 1 |
| AY0 | 11 | AI | Analog input 0 of channel 1 |
| ACR2 | 14 | AI | Analog input 2 of channel 0 |
| ACR1 | 15 | AI | Analog input 1 of channel 0 |
| ACR0 | 16 | AI | Analog input 0 of channel 0 |
| VSI | 26 | DI, P/D | RGB Vertical Synchronous input |
| HSI | 27 | DI, P/U | RGB Horizontal Synchronous input |
| SOYIN | 2(CCFL), 1(LED) | AI | Sync on Y (of component) input |
| SAR1 | 2(LED) | AI | SARADC for keypads sense |
| VPLL | 20 | AI | PLL Reference |
| FILT | 21 | AI | PLL filter |
| **Video-In Interface: ITUR656** | | | |
| LVC0~7 | 39~46 | DI, P/D | Video data port of the 2nd ITU-656 |

| Symbol | Pin # | Type | Description |
|---|---|---|---|
| LVCLK | 48 | DI, P/D | Video clock of the 2nd ITU-656 (2x pixel rate) |
| **Video-In Interface: L601_8bit** | | | |
| LVC0~7 | 39~46 | DI, P/D | Video data port of 8-bit 601 or Chroma |
| LVCLK | 48 | DI, P/D | Video clock (2x pixel rate) |
| LODD/LVSYNC | 49 | DIO, P/D | ITU-601 Odd or VSync input |
| LHREF/LHSYNC | 50 | DIO, P/D | ITU-601 HREF(HDE) or HSync input |
| **Video-In Interface: L601_16bit** | | | |
| LVC0~7 | 39~46 | DI, P/D | Video chroma data port of 16-bit 601 |
| LVY0~7 | 65, 68~74 | DI, P/D | Video Luma data port of 16-bit 601 |
| LVCLK | 48 | DI, P/D | Video clock (1x pixel rate) |
| LODD/LVSYNC | 49 | DIO, P/D | ITU-601 Odd or VSync input |
| LHREF/LHSYNC | 50 | DIO, P/D | ITU-601 HREF(HDE) or HSync input |
| **Video-In Interface: RGB565** | | | |
| DRI3~7 | 70~74 | DI, P/D | Digital RGB input: 5 MSB bits of Color R |
| DGI2~7 | 44~46, 65, 68~69 | DI, P/D | Digital RGB input: 6 MSB bits of Color G |
| DBI3~7 | 39~43 | DI, P/D | Digital RGB input: 5 MSB bits of Color B |
| LVCLK | 48 | DI, P/D | Video clock (1x pixel rate) |
| DVSI | 49 | DIO, P/D | Digital RGB VSync input |
| DHSI | 50 | DIO, P/D | Digital RGB HSync input |
| **Misc. Signals** | | | |
| XCLKI | 33 | DI | Output PLL reference clock input and I2C, timer operating clock |
| XCLKO | 34 | DO | Output PLL reference clock output |
| IR1 | 35 | DI, P/U | IR input |
| PWM1 | 36 | DIO, P/D | Pulse Width Modulation 1 for backlight control / Volume / … |
| RSET | 80 | AI | DAC reference current adjust |
| VBGF | 81 | AI | DAC voltage reference output |

# 2 Theory of Operations

## 2.1 I²C Command Protocol

Before your tester writes I²C commands to T108, slave address must be set at 50h. The timing sequence can be shown as below. After 4 cycles, the tester can get started IIC commands. CPUINT(A3) can affect slave address. Set it low for 40h, and high for 50h.

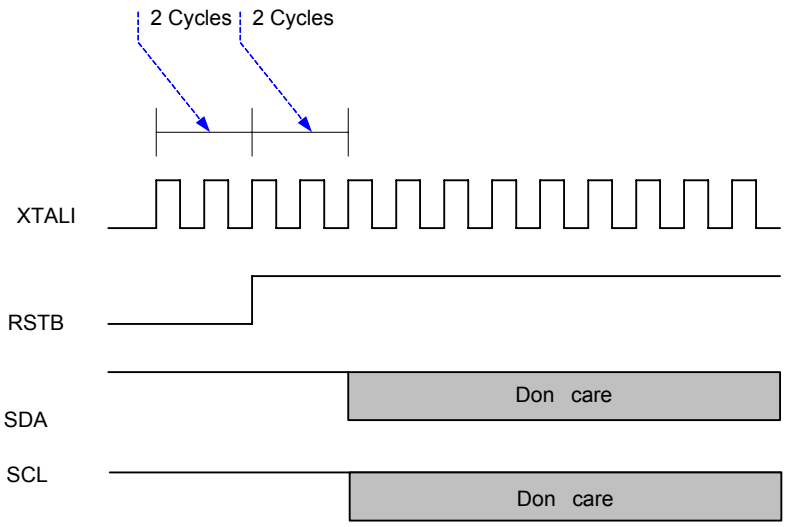



**Figure 2-1 Power-Up Initialization**

When tester issues commands to the T108, the only way the user can program the T108 is using the 2-wire serial bus protocol. This section describes the 2-wire serial bus protocol. Data transfers on the 2-wire serial bus are initiated with a START condition and are terminated with a STOP condition. Normal data on the SDA line must be stable during the high period of the SCL. The transition on the SDA is only allowed while SCL is low. The START condition is unique case and is defined by a high-to-low transition on the SDA while the SCL is high. The STOP condition is a unique case and is defined by a low-to-high transition on the SDA while the SCL is high. Each data packet on the 2-wire serial bus consists of 8 bits of data followed by an ACK bit. Data is transferred with MSB first. The transmitter releases the SDA line during the ACK bit and the receiver of data transfer must drive the SDA line low during the ACK bit to acknowledge receipt of the data. The frequency of SCL can be from 50 KHz up to 2 MHz (~=XCLK/12).

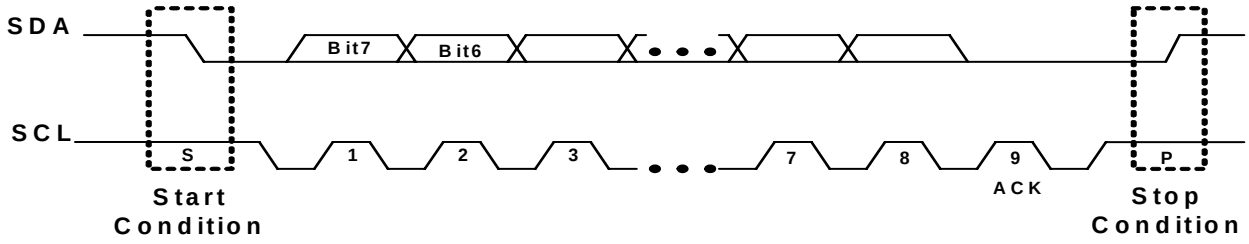



**Figure 2-2 Basic I²C Bus Protocol**

The timing below shows a typical T108 I²C single byte write command,

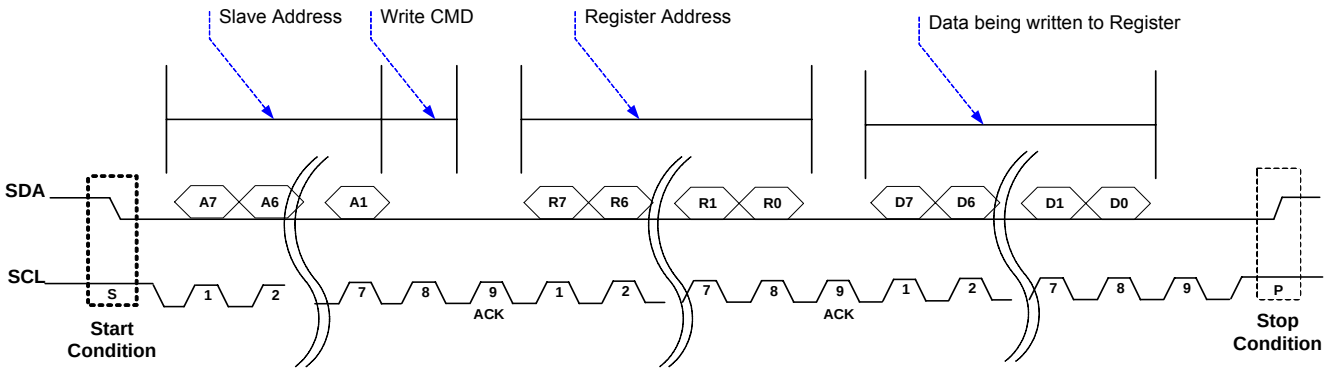



**Figure 2-3 T108 I²C Single Byte Write Command**

The timing below shows a typical T108 I²C single byte read command,

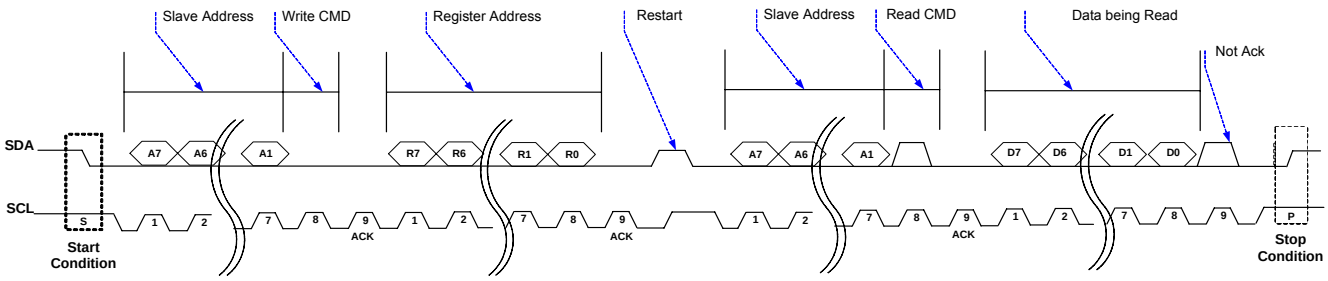



**Figure 2-4 T108 I²C Single Byte Write Command**

## 2.2 Analog Front End

T108 contains 3 ADCs in Analog Front End. Each channel of ADCs can digitalize SDTV signals from analog to digital. The figure shown below can describe how to select a SDTV signal from 3 inputs prior to ADC.

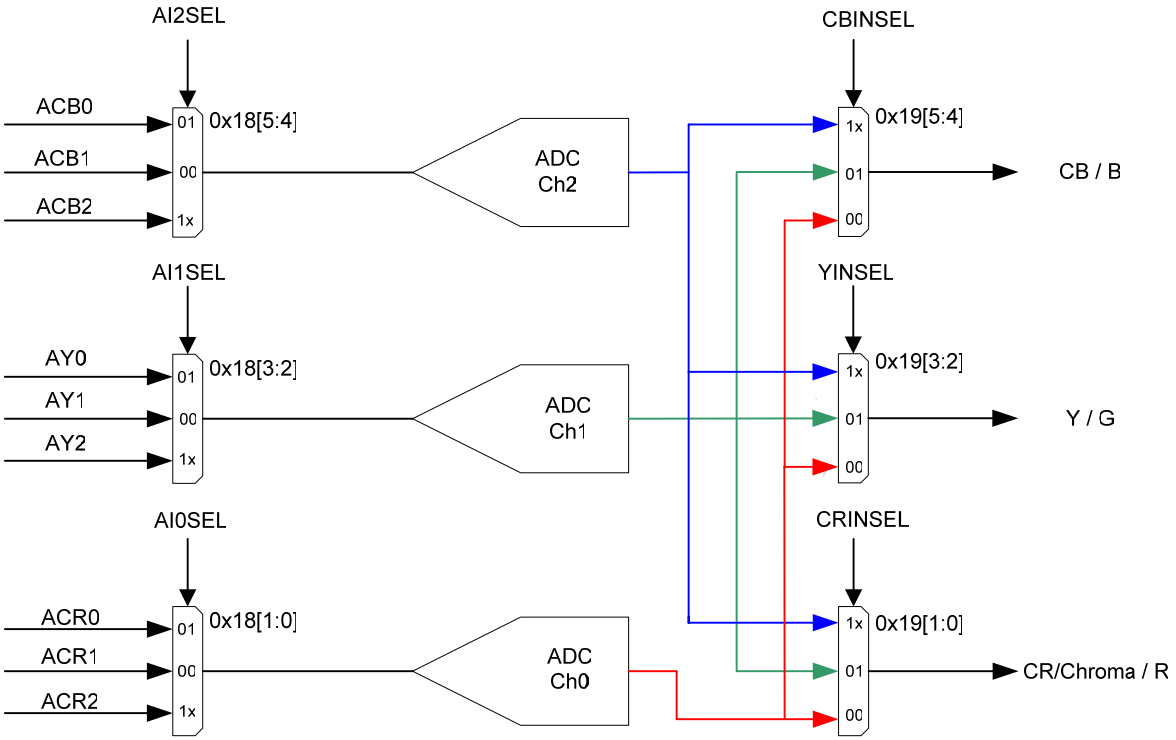



**Figure 2-5 Analog Front End MUX**

## 2.3 Black-Level Extension (BLE)

Black Level Expansion (BLE) can enhance image contrast that makes dark regions of image darker, while bright regions remain unchanged. The figure shown below is BLE transfer function.

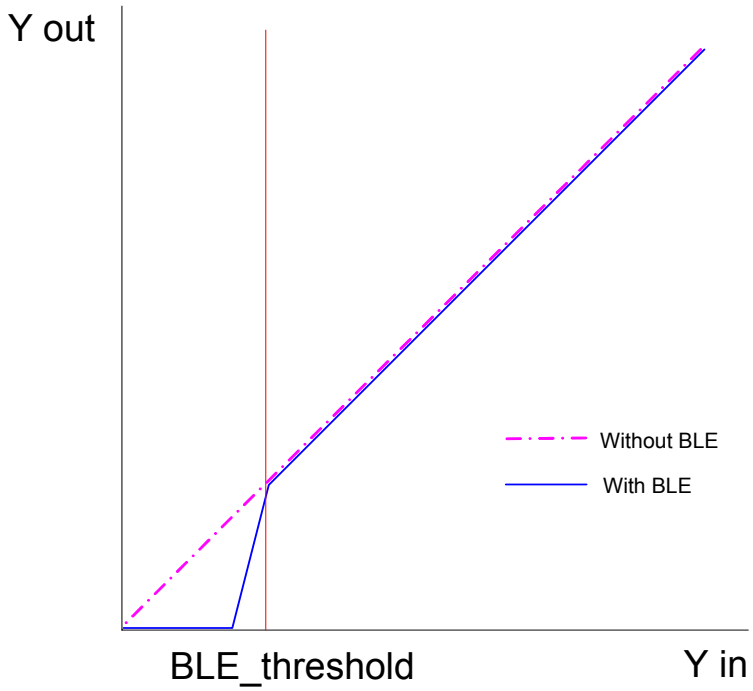



**Figure 2-6 Black Level Expansion**

$$Yout = Yin - (Yoffset - Yin) * BLE\_Gain / 16$$

Where $Yoffset$ and $BLE\_Gain$ can be programmed by register P0_96h.

## 2.4 Color Space Converter

A pixel in YCbCr color space can be converted to RGB color space by using following equations,

$$R = YCoef\_R * (Y - 16) + /- CbCoef\_R * (Cb - 128) + CrCoef\_R * (Cr - 128)$$
$$G = YCoef\_G * (Y - 16) - CbCoef\_G * (Cb - 128) - CrCoef\_G * (Cr - 128)$$
$$B = YCoef\_B * (Y - 16) + CbCoef\_B * (Cb - 128) + /- CrCoef\_B * (Cr - 128)$$

The equations shown as below correspond to a typical YCbCR-to-RGB converter.

## 2.5 Gamma Correction

The relation between input video signal and LCD panel may exist non-linear transfer function such as figure shown below,

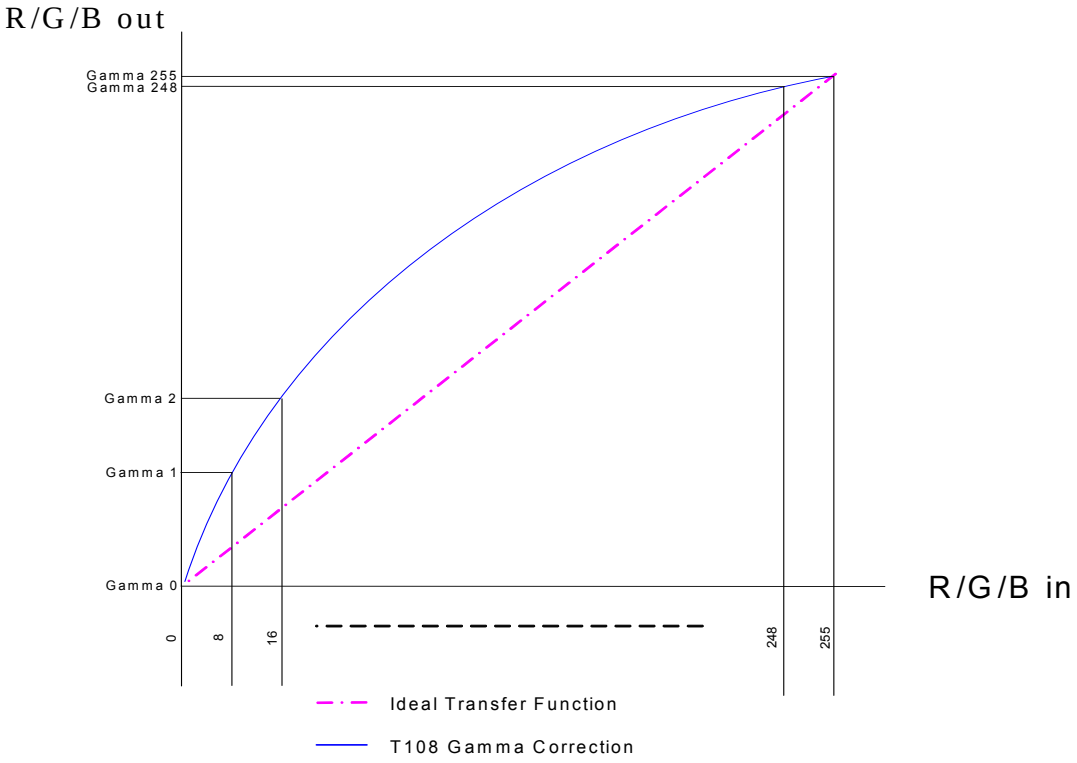



**Figure 2-7 Gamma LUT**

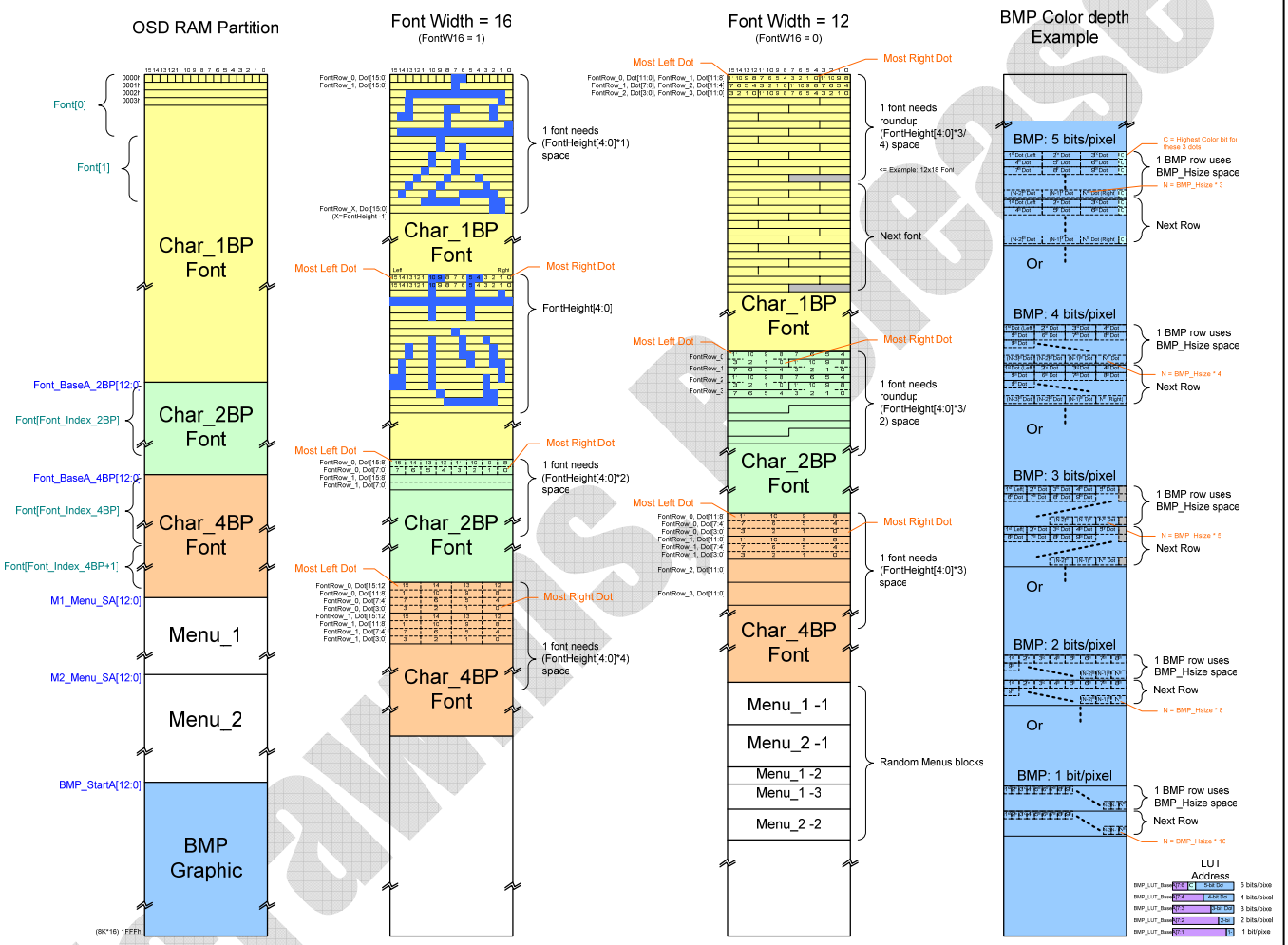
T108 uses 33-point piece-wise linear interpolation instead of RAM-based LUTs. Each point can be programmed via register at P0_93h and P0_94h.

## 2.6 OSD1

The OSD1 in T108 is improved in rendering and efficient memory usage. The legacy OSD is either one thread Menu or one graphic (BMP) mode. T108 OSD1 supports two threads menus and 1 graphic rendering simultaneously. So it will be easier to have menu control and Closed Caption.

### 2.6.1 OSD1 RAM Partition

The OSD1 Font/Menus/BMP memory share the same built-in 8Kx16 SRAM.



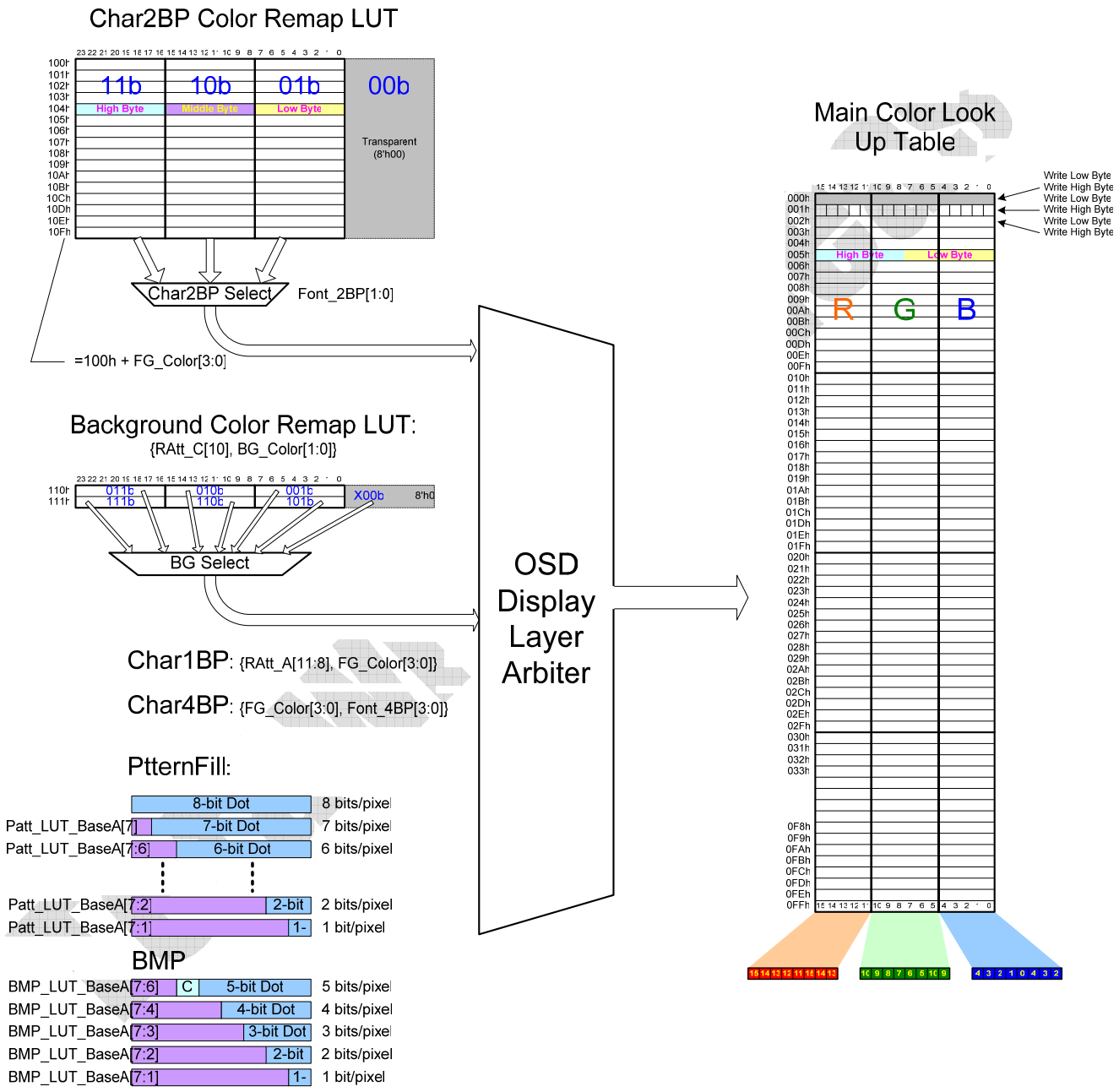
## 2.6.2 OSD1 Register Map

| I/O Port | Groups | Index | Description |
|---|---|---|---|
| A0h – OSD1_Index<br>A1h – OSD1_Data | Global Setting | 00h | OSD1 Enable/Blinking Register |
| | | 01h | Font Size |
| | | 02h | Char2BP Font Index Base |
| | | 03h | Char4BP Font Index Base |
| | | 04h | Char2BP Font Memory Base Address, LSB |
| | | 05h | Char2BP Font Memory Base Address, MSB |
| | | 06h | Char4BP Font Memory Base Address, LSB |
| | | 07h | Char4BP Font Memory Base Address, MSB |
| | | 08h | OSD1 Color LUT Address port |
| | | 09h | OSD1 Color LUT Data Port |
| | | 0Ah | OSD1 Window Shadow |
| | | 0Bh | Global Alpha Blending Control |
| | | 0Ch | Char1BP color high bits offset |
| | | 0Dh | ROM Font Index Base |
| | | 0Fh | Revision ID |
| | Menu-1 Setting | 10h | Menu-1 Enable |
| | | 11h | Menu-1 Start Address, LSB |
| | | 12h | Menu-1 Start Address, MSB |
| | | 13h | Menu-1 End Address, LSB |
| | | 14h | Menu-1 End Address, MSB |
| | ROM Font | 16h | ROM Font Memory Base Address, LSB |
| | | 17h | ROM Font Memory Base Address, MSB |
| | Menu-2 Setting | 18h | Menu-2 Enable |
| | | 19h | Menu-2 Start Address, LSB |
| | | 1Ah | Menu-2 Start Address, MSB |
| | | 1Bh | Menu-2 End Address, LSB |
| | | 1Ch | Menu-2 End Address, MSB |
| | BMP Setting | 20h | BMP Control Register |
| | | 21h | BMP Start Address, LSB |
| | | 22h | BMP Start Address, MSB |
| | | 23h | BMP Alpha Blending Control |
| | | 24h | BMP Horizontal Size, LSB |
| | | 25h | BMP Horizontal Size, MSB |
| | | 26h | BMP Vertical Size, LSB |
| | | 27h | BMP Vertical Size, MSB |
| | | 28h | BMP Position, Horizontal Start, LSB |
| | | 29h | BMP Position, Horizontal Start, MSB |
| | | 2Ah | BMP Position, Vertical Start, LSB |
| | | 2Bh | BMP Position, Vertical Start, MSB |
| | | 2Ch | BMP LUT Base Address |
| | | 2Dh | BMP Background Color |

| I/O Port | Groups | Index | Description |
|---|---|---|---|
| | Block Write | 40h | Block Write Data LSB |
| | | 41h | Block Write Data MSB |
| | | 42h | Block Write Starting Address LSB |
| | | 43h | Block Write Starting Address MSB |
| | | 44h | Block Write Count |
| | | 45h | Block Write Control |
| A2h – ORAM_A | | | OSD1 RAM Address Port of Starting Access (LSB A[7:0] first, then MSB A[12:8]). |
| A3h – ORAM_D | | | OSD1 RAM Data Port (Low Byte first, then High Byte). After two Writes, the address will be increased by 1. |

### 2.6.3 OSD1 Color Scheme

For drawing a graphic menu, a colorful icon or logo, …., T108 OSD1 provides 1BPP (one bit per pixel) ~ 5BPP (5 bits per pixel) BMP coding. For n-BPP BMP, it has one background color and (2^n – 1) foreground colors. For character menus with pre-defined fonts, T108 OSD1 provides mono characters (Char1BP) and color characters (Char2BP, Char4BP), randomly mix-able. So that, simple icon can be implemented by color characters. The color mapping of character/menu is more complicate, please refer to the following drawing. The OSD1 main Color LUT is 256 entries SRAM, color in RGB565 format.



### 2.6.4 Character RAM Format

T108 OSD1 character decoding supports 512 fonts. By setting FontROM, Char2BP and Char4BP Font Index Base, we could assign different percentage for those character fonts, depends on application, menu color requirement, memory size, fonts replacing, ...

The character “MENU” in T108 OSD1 is combined with 1~n character “ROW”s, each ROW can have its own rendering behavior, such as alpha blending, position, zooming ratio, color groups, border/shadow modes, row length,…, these are defined as ROW Attributes (RAtt, current version supports 8 types). Or, few rows can share the same setting without redefining those RAtt.

#### 2.6.4.1 Character Format

Each character is 16-bits length, includes foreground/background color, blinking, font index.

| Bit | Symbol | Description |
|---|---|---|
| [15:14] | BG_Color[1:0] | Background Color, which combined with the RAtt_C<10> to become 3 bit, selects 6 background remap colors. If both 0, then transparent background. |
| [13] | Blink | Enable this Character display with blinking feature. |
| [12:9] | FG_Color[3:0] | Foreground (FG) Color, depends font index is Char1BP, Char2BP or Char4BP:<br>1. When Char1BP, these 4 bits as FG LSB 4 bits, combine with RAtt_A<11:8> (as FG MSB 4 bits), total 8 bits for selecting color LUT as character FG color. If the value is set as 0000b, then there will be no foreground, i.e. transparent. (Char1BP only)<br>2. When Char2BP, these 4 bits select one of 16 Char2BP remap LUT. Each Char2BP remap LUT entry is 3*8 bits for 2BP font pixel value: 01b, 10b and 11b. For 2BP font pixel value = 00b, then it will render as transparent.<br>3. When Char4BP, these 4 bits as FG MSB, then combine with 4BP font pixel 4 bits value to become 8 bits for addressing LUT. For 4BP font pixel value = 0000b, then it will render as transparent. |
| [8:0] | Char_Index[8:0] | Character Address (Index), selects the character font (i.e., 0,1,2,.. A,B,C, a,b,c,$,%,…). If the value is number N, then it selects the $N^{th}$ font, and that font starting address is (N x Font_Height ). The Font_Height is defined in OSD1_01h<4:0>. |

#### 2.6.4.2 Row Attribute Alpha-Blending Type Format (RAtt_A)

| Bit | Symbol | Description |
|---|---|---|
| [15:12] | RAtt_ID = 1101b | Must set value 1101b for RAtt_A |
| [11:8] | FGC_1BP[7:4] | Defines the MSB 4 bits for Char1BP FG color for current row or below in same thread menu. |
| [7:6] | Reserved | |
| [5:4] | FG_aB_Mode[1:0] | Defines the FG alpha-Blending mode (see OSD1 configuration register OSD1_0B for detail) for current row or below in same thread menu. |
| [3:0] | aB_Source_Percentage[3:0] | Defines the alpha-Blending ratio (of source video/graphic) for current row or below in same thread menu. |

#### 2.6.4.3 Row Attribute Character Type Format (RAtt_C)

This RAtt_C is a must-have attribute for each menu row, and those content in OSD1 memory followed will be rendering as characters, not other row attributes except exceeding the row length (see Row_Length[5:0] below).

| Bit | Symbol | Description |
|---|---|---|
| [15:13] | RAtt_ID = 000b | Must set value 000b for RAtt_C |
| [12] | Skip_This | When set to 1, the following one character row of current thread menu could be skipped, and continues the next row instead. |
| [11] | End_After | When set to 1, the following all character rows of current thread menu will be skipped. |
| [10] | BG_RGB[2] | Background color bit 2, combined with the BG_Color[1:0] in each character become 3 bits to select background remap color. |
| [9:8] | CharHeight_Scale[1:0] | Defines the enlarge ratio (x1, x2, x3, x4) of the character height of the menu rows following and after. |
| [7:6] | CharWidth_Scale[1:0] | Defines the enlarge ratio (x1, x2, x3, x4) of the character width of the menu rows following and after. |
| [5:0] | Row_Length[5:0] | Indicates the following character row length (how many characters), valid value range is 1 to 63. |

#### 2.6.4.4 Row Attribute Dummy Type Format (RAtt_D)

This RAtt_D is a dummy attribute, it is used for replacing other non-RAtt_C type attributes when changing rendering behavior if need, also it is used when switch between rows with different BDS behavior, 4 lines will be inserted.

| Bit | Symbol | Description |
|---|---|---|
| [15:0] | RAtt_ID = E001h | Must set value E001h for RAtt_D |

#### 2.6.4.5 Row Attribute Gap Type Format (RAtt_G)

This RAtt_G is used to insert fix vertical null lines between menu rows.

| Bit | Symbol | Description |
|---|---|---|
| [15:13] | RAtt_ID = 001b | Must set value 001b for RAtt_G |
| [12:11] | Reserved | |
| [10:0] | Gap[10:0] | Line number inserted before the following menu row. |

#### 2.6.4.6 Row Attribute Jump Menu Type Format (RAtt_J)

This RAtt_J is used to redirect menu to other assigned new menu block in OSD1 memory. This is useful for controlling menu flows.

| Bit | Symbol | Description |
|---|---|---|
| [15:14] | RAtt_ID = 10b | Must set value 10b for RAtt_J |
| [13] | Jump_En | Set to 1 enables the menu jump to new assigned address in RAtt_J<12:0>. When set to 0, this RAtt_J has no effect. |
| [12:0] | Jump_MenuA[12:0] | Jump to the OSD1 RAM address, which should still point to a row attribute of menu. |

### 2.6.4.7 Row Attribute Horizontal Position Type Format (RAtt_H)

| Bit | Symbol | Description |
|---|---|---|
| [15:13] | RAtt_ID = 011b | Must set value 011b for RAtt_H |
| [12:11] | Reserved | |
| [10:0] | HStart[10:0] | Set the horizontal start position of the following menu rows. |

### 2.6.4.8 Row Attribute Vertical Position Type Format (RAtt_V)

| Bit | Symbol | Description |
|---|---|---|
| [15:13] | RAtt_ID = 010b | Must set value 010b for RAtt_V |
| [12:11] | Reserved | |
| [10:0] | VStart[10:0] | Set the vertical start position of the following menu rows. |

## 2.6.5 OSD1 Configuration Registers

### 2.6.5.1 OSD1 Enable/Blinking Register

Address Offset: OSD1_00h Access: Read/Write
Default Value: 0Ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | OSD1_En | Set to 1 for globally enabling OSD1 function. |
| [6] | R/W | Color_1_Half | Set to 1 for allowing shadow effect when color value is 1 |
| [5:4] | R/W | CRAM_ByteAccess[1:0] | Byte Access mode when programming character of menu:<br>0Xb: Word access (LSB first, then MSB byte)<br>10b: LSB only (not affect font index >= 256)<br>11b: MSB only (character BG/FG colors, Blinking, and Index bit 8) |
| [3:2] | R/W | BlinkFreq[1:0] | Blinking Frequency Select (internal 4x BCLK for Blinking State Machine). Set 00b for Refresh Rate /16; 01b for 1/32; 10b for 1/64; 11b for 1/128. |
| [1:0] | R/W | BlinkDuty[1:0] | For adjusting the blinking duty cycle, Set:<br>00b for Global Blink Off, i.e., 0% Background, 100% Pattern Fill.<br>01b for 25% Background, 75% Pattern Fill.<br>10b for 50% Background, 50% Pattern Fill.<br>11b for 75% Background, 25% Pattern Fill. |

### 2.6.5.2 OSD1 Font Size Register

Address Offset: OSD1_01h Access: Read/Write
Default Value: 12h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | vDE_from_VS | Shift OSD1 more up |
| [6] | R/W | hDE_from_HS | Shift OSD1 more left |
| [5] | R/W | FontW16 | Set Font Width:<br>0b: Font Width = 12<br>1b: Font Width = 16 |
| [4:0] | R/W | FontHeight[4:0] | Font Height, valid value between 1 and 24 |

### 2.6.5.3 OSD1 Char2BP Font Index Base Register

Address Offset: OSD1_02h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Font_Index_2BP[8:1] | Defines the Char2BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char). And if the character index greater than or equal to this value*2 will be decoded as Char2BP (<= Font_Index_4BP * 2). |

### 2.6.5.4 OSD1 Char4BP Font Index Base Register

Address Offset: OSD1_03h Access: Read/Write
Default Value: C0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Font_Index_4BP[8:1] | Defines the Char4BP font index base (offset). When character index small than this value*2 will be decoded as Char1BP (mono char) or Char2BP; else, Char4BP. |

### 2.6.5.5 OSD1 Char2BP Font Memory Base Address LSB Register

Address Offset: OSD1_04h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Font_BaseA_2BP[7:0] | Defines the Char2BP font in memory, start with this base address (offset). |

### 2.6.5.6 OSD1 Char2BP Font Memory Base Address MSB Register

Address Offset: OSD1_05h Access: Read/Write
Default Value: 0Ch Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | Font_BaseA_2BP[12:8] | Defines the Char2BP font in memory, start with this base address (offset). |

### 2.6.5.7 OSD1 Char4BP Font Memory Base Address LSB Register

Address Offset: OSD1_06h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Font_BaseA_4BP[7:0] | Defines the Char4BP font in memory, start with this base address (offset). |

### 2.6.5.8 OSD1 Char4BP Font Memory Base Address MSB Register

Address Offset: OSD1_07h Access: Read/Write
Default Value: 0Fh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | Font_BaseA_4BP[12:8] | Defines the Char4BP font in memory, start with this base address (offset). |

### 2.6.5.9 OSD1 LUT Address Register

Address Offset: OSD1_08h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | LUT_A[8:1] | Assign access pointer of Color LUT. When assigning, LUT_A[0] always = 0. LUT[0..255] are main color LUT (16-bits); LUT[256..271] are Char2BP remap LUT (24-bits); LUT[272..273]are BMP remap LUT (24-bits). |

### 2.6.5.10 OSD1 LUT Data Port Register

Address Offset: OSD1_09h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | LUT_D[7:0] | Data written to this port will overwrite OSD1 LUT. |

### 2.6.5.11 OSD1 Window Shadow Width/Height Register

Address Offset: OSD1_0Ah Access: Read/Write
Default Value: 46h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | Wx_ShadowWidth[3:0] | Defines the shadow width (count in 2 dots). |
| [3:0] | R/W | Wx_ShadowHeight[3:0] | Defines the shadow height (count in 2 lines). |

### 2.6.5.12 OSD1 Global Alpha-Blending Control Register

Address Offset: OSD1_0Bh Access: Read/Write
Default Value: 1Ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | Global_aB_Control | Set to 1 for all the alpha-blending behavior of Menu-1, Menu-2 and BMP are control by this register; Set to 0 for separate controls. |
| [6] | RO | Reserved | |
| [5:4] | R/W | Global_FG_aB_Mode[1:0] | Defines global alpha-blending for foreground when BG already alpha-Blended:<br>00b: All FG need alpha-Blended if BG is alpha-Blended;<br>01b: All FG no need alpha-Blended;<br>10b: All FG no need alpha-Blended, except their color is LUT[1];<br>11b: All FG no need alpha-Blended, except their color is LUT[1..3]; |
| [3:0] | R/W | Global_aB_SourcePercent[3:0] | Defines the percentage of source image/video for mixed with OSD1 menu. |

### 2.6.5.13 OSD1 Char1BP Color High bits Register

Address Offset: OSD1_0Ch Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | RO | Reserved | |
| [3:0] | R/W | FGC_1BP_Color[7:4] | Defines the Char1BP FG color [7:4] |

### 2.6.5.14 OSD1 FontROM Index Base Register

Address Offset: OSD1_0Dh Access: Read/Write
Default Value: 40h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | FontROM_IndexBase [8:1] | For font index value less than this value is mono character (Char1BP) RAM font segment;<br>For font index >= this value but less than Char2BP_IndexBase is mono character (Char1BP) ROM font segment. |

### 2.6.5.15 OSD1 Revision ID Register

Address Offset: OSD1_0Fh Access: Read Only
Default Value: 31h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | Revision_ID[7:0] | |

### 2.6.5.16 OSD1 Menu-1 Enable Register

Address Offset: OSD1_10h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | M1_En | Set to 1 enable Menu-1 thread to display |
| [6:0] | RO | Reserved | |

### 2.6.5.17 OSD1 Menu-1 Start Address LSB Register

Address Offset: OSD1_11h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | M1_Menu_SA[7:0] | Point to the 1st row attribute of Menu-1 in OSD1 RAM. |

### 2.6.5.18 OSD1 Menu-1 Start Address MSB Register

Address Offset: OSD1_12h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | M1_Menu_SA[12:8] | Point to the 1st row attribute of Menu-1 in OSD1 RAM. |

### 2.6.5.19 OSD1 Menu-1 End Address LSB Register

Address Offset: OSD1_13h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | M1_Menu_EA[7:0] | Point to the end of Menu-1 in OSD1 RAM. |

### 2.6.5.20 OSD1 Menu-1 End Address MSB Register

Address Offset: OSD1_14h Access: Read/Write
Default Value: 14h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | M1_Menu_EA[12:8] | Point to the end of Menu-1 in OSD1 RAM. |

### 2.6.5.21 OSD1 FontROM Base Address LSB Register

Address Offset: OSD1_16h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Font_BaseA_ROM[7:0] | Point to the start address in ROM, i.e., point to the 1st Font in ROM. |

### 2.6.5.22 OSD1 FontROM Base Address MSB Register

Address Offset: OSD1_17h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | Font_BaseA_ROM[12:8] | Point to the start address in ROM, i.e., point to the 1st Font in ROM. |

### 2.6.5.23 OSD1 Menu-2 Enable Register

Address Offset: OSD1_18h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | M2_En | Set to 1 enable Menu-2 thread to display |
| [6:0] | RO | Reserved | |

### 2.6.5.24 OSD1 Menu-2 Start Address LSB Register

Address Offset: OSD1_19h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | M2_Menu_SA[7:0] | Point to the 1st row attribute of Menu-2 in OSD1 RAM. |

### 2.6.5.25 OSD1 Menu-2 Start Address MSB Register

Address Offset: OSD1_1Ah Access: Read/Write
Default Value: 15h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | M2_Menu_SA[12:8] | Point to the 1st row attribute of Menu-2 in OSD1 RAM. |

### 2.6.5.26 OSD1 Menu-2 End Address LSB Register

Address Offset: OSD1_1Bh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | M2_Menu_EA[7:0] | Point to the end of Menu-2 in OSD1 RAM. |

### 2.6.5.27 OSD1 Menu-2 End Address MSB Register

Address Offset: OSD1_1Ch Access: Read/Write
Default Value: 16h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | M2_Menu_EA[12:8] | Point to the end of Menu-2 in OSD1 RAM. |

### 2.6.5.28 OSD1 BMP Control Register

Address Offset: OSD1_20h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | BMP_En | Set to 1 enable BMP to display |
| [6:4] | R/W | BMP_Nbpp | Defines current BMP for displaying is N bits per pixel.<br>000b: Reserved<br>001b: 1 bit/pixel<br>010b: 2 bits/pixel<br>011b: 3 bits/pixel<br>100b: 4 bits/pixel<br>101b: 5 bits/pixel<br>11Xb: 5 bits/pixel |
| [3:2] | R/W | BMP_Extra_Height[1:0] | BMP enlarge ratio in vertical direction: x1, x2, x3, x4 lines |
| [1:0] | R/W | BMP_Extra_Width[1:0] | BMP enlarge ratio in horizontal direction: x1, x2, x3, x4 dots |

### 2.6.5.29 OSD1 BMP Start Address LSB Register

Address Offset: OSD1_21h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BMP_SA[7:0] | Point to the top-left dot of BMP for displaying in OSD1 RAM. |

### 2.6.5.30 OSD1 BMP Start Address MSB Register

Address Offset: OSD1_22h Access: Read/Write
Default Value: 0Bh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | BMP_SA[12:8] | Point to the top-left dot of BMP for displaying in OSD1 RAM. |

### 2.6.5.31 OSD1 BMP Alpha-Blending Control Register

Address Offset: OSD1_23h Access: Read/Write
Default Value: 1Ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | BMP_FG_aB_Mode[1:0] | Defines BMP alpha-blending for foreground when BG already alpha-Blended:<br>00b: All FG need alpha-Blended if BG is alpha-Blended;<br>01b: All FG no need alpha-Blended;<br>10b: All FG no need alpha-Blended, except their color is LUT[1];<br>11b: All FG no need alpha-Blended, except their color is LUT[1..3]; |
| [3:0] | R/W | BMP_aB_SourcePercent[3:0] | Defines the percentage of source image/video for mixed with OSD1 BMP. |

### 2.6.5.32 OSD1 BMP Horizontal Size LSB Register

Address Offset: OSD1_24h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BMP_HSize[7:0] | Defines the horizontal size of BMP for displaying in OSD1 RAM. Unit is how manys word (16-bits) count (before enlarged). |

### 2.6.5.33 OSD1 BMP Horizontal Size MSB Register

Address Offset: OSD1_25h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | BMP_HSize[10:8] | Defines the horizontal size of BMP for displaying in OSD1 RAM. |

### 2.6.5.34 OSD1 BMP Vertical Size LSB Register

Address Offset: OSD1_26h Access: Read/Write
Default Value: 60h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BMP_HSize[7:0] | Defines the vertical size of BMP for displaying in OSD1 RAM. Unit is how many lines count (before enlarged). |

### 2.6.5.35 OSD1 BMP Vertical Size MSB Register

Address Offset: OSD1_27h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | BMP_HSize[10:8] | Defines the vertical size of BMP for displaying in OSD1 RAM. |

### 2.6.5.36 OSD1 BMP Horizontal Start Position LSB Register

Address Offset: OSD1_28h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BMP_HStart[7:0] | Defines the left boundary position of BMP for displaying, count in display clocks. |

### 2.6.5.37 OSD1 BMP Horizontal Start Position MSB Register

Address Offset: OSD1_29h Access: Read/Write
Default Value: 03h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | BMP_HStart[10:8] | Defines the left boundary position of BMP for displaying. |

### 2.6.5.38 OSD1 BMP Vertical Start Position LSB Register

Address Offset: OSD1_2Ah Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BMP_VStart[7:0] | Defines the top boundary position of BMP for displaying, count in lines. |

### 2.6.5.39 OSD1 BMP Vertical Start Position MSB Register

Address Offset: OSD1_2Bh Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | BMP_VStart[10:8] | Defines the top boundary position of BMP for displaying. |

### 2.6.5.40 OSD1 BMP LUT Base Address Register

Address Offset: OSD1_2Ch Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:1] | R/W | BMP_LUT_BaseA[7:1] | Defines the LUT offset. For N-BPP BMP, its LUT segment starts with {BMP_LUT_BaseA[7:N], N'b0}; |
| [0] | RO | Reserved | |

### 2.6.5.41 OSD1 BMP Background Color Register

Address Offset: OSD1_2Dh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BMP_BG_Color[7:0] | Defines the address of one LUT as BMP background color. |

### 2.6.5.42 OSD1 Block Write Data LSB Register

Address Offset: OSD1_40h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1_BlockWr_D[7:0] | LSB Data to be block fill |

### 2.6.5.43 OSD1 Block Write Data MSB Register

Address Offset: OSD1_41h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1_BlockWr_D[15:8] | MSB Data to be block fill |

### 2.6.5.44 OSD1 Block Write Starting Address LSB Register

Address Offset: OSD1_42h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1_BlockWr_SA[7:0] | Starting Address of block fill |

### 2.6.5.45 OSD1 Block Write Starting Address MSB Register

Address Offset: OSD1_43h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | OSD1_BlockWr_SA[12:8] | Starting Address of block fill |

### 2.6.5.46 OSD1 Block Write Length Register

Address Offset: OSD1_44h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1_BlockWr_L[7:0] | Block fill length (count) |

### 2.6.5.47 OSD1 Block Write Control Register

Address Offset: OSD1_45h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | WO/<br>RO | OSD1_BlockWr_Trig<br>OSD1_BlockWr_Done | Set to 1 to trigger block fill operation<br>Get 1 means the block fill operation is done |
| [6] | R/W | OSD1_BlockWr_mode | |
| [5] | RO | Reserved | |
| [4:0] | R/W | OSD1_BlockWr_L[12:8] | Block fill length (count) |

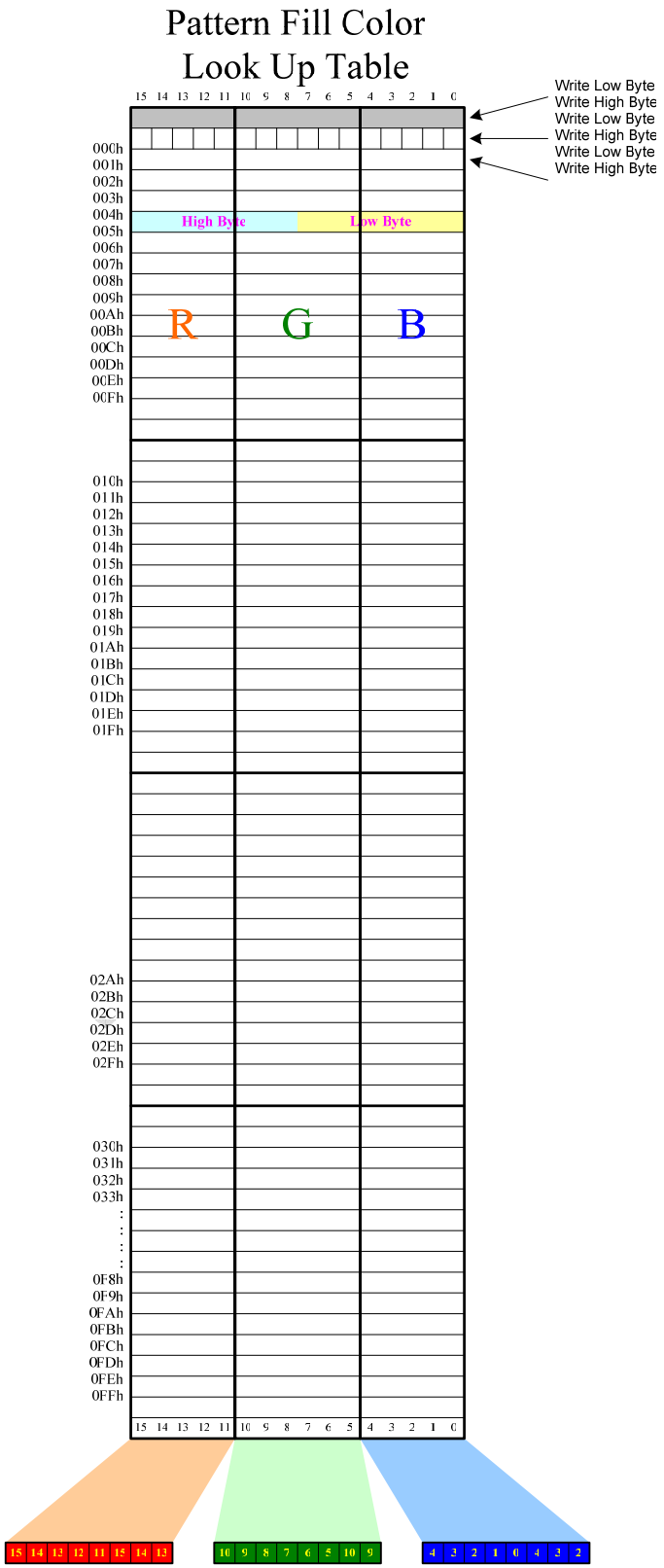
## 2.7 Pattern Fill

### 2.7.1 Pattern Fill Register Map

| I/O Port | Groups | Index | Description |
|---|---|---|---|
| A8h – OSD1_Index<br>A9h – OSD1_Data | Pattern Fill | 00h | OSD1 Pattern Fill Enable/Blinking Register |
| | | 08h | OSD1 Pattern Fill Color LUT Address port |
| | | 09h | OSD1 Pattern Fill Color LUT Data Port |
| | | 30h | Pattern Fill Control Register |
| | | 31h | Pattern Fill LUT Base Address |
| | | 32h | Pattern Fill Horizontal Size |
| | | 33h | Pattern Fill Vertical Size |
| | | 34h | Pattern Fill Row Shift |
| | | 35h | Pattern Fill Alpha Blending Control |
| | | 36h | OSD1 BIST Result and Pattern Fill Enlarge |
| | | 37h | Pattern Fill RAM Write Data Port |
| | | 38h | Pattern Fill Horizontal Start, LSB |
| | | 39h | Pattern Fill Horizontal Start, MSB |
| | | 3Ah | Pattern Fill Vertical Start, LSB |
| | | 3Bh | Pattern Fill Vertical Start, MSB |
| | | 3Ch | Pattern Fill Horizontal End, LSB |
| | | 3Dh | Pattern Fill Horizontal End, MSB |
| | | 3Eh | Pattern Fill Vertical End, LSB |
| | | 3Fh | Pattern Fill Vertical End, MSB |

### 2.7.2 OSD1 Pattern Fill Color Scheme

Pattern Fill can be implemented by Bitmap. The color mapping of Bitmap is more complicate, please refer to the following drawing. The OSD1 Pattern Fill main Color LUT is 256 entries SRAM, color in RGB565 format.



## 2.7.3 OSD1 Pattern Fill Configuration Registers

### 2.7.3.1 OSD1 Pattern_Fill Enable/Blinking Register

Address Offset: OSD1PF_00h Access: Read/Write
Default Value: 0Ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | OSD1PF_En | Set to 1 for globally enabling OSD1 Pattern Fill function. |
| [6] | R/W | Reserved | |
| [5:4] | R/W | CRAM_ByteAccess[1:0] | Byte Access mode when programming character of menu:<br>0Xb: Word access (LSB first, then MSB byte)<br>10b: LSB only (not affect font index >= 256)<br>11b: MSB only (character BG/FG colors, Blinking, and Index bit 8) |
| [3:0] | R/W | Reserved | |

### 2.7.3.2 OSD1 Pattern_Fill LUT Address Register

Address Offset: OSD1PF_08h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | LUT_A[8:1] | Assign access pointer of Color LUT. When assigning, LUT_A[0] always = 0. LUT[0..255] are main color LUT (16-bits); LUT[256..271] are Char2BP remap LUT (24-bits); LUT[272..273]are BMP remap LUT (24-bits). |

### 2.7.3.3 OSD1 Pattern_Fill LUT Data Port Register

Address Offset: OSD1 PF _09h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | LUT_D[7:0] | Data written to this port will overwrite OSD2 LUT. |

### 2.7.3.4 OSD1 Pattern_Fill Control Register

Address Offset: OSD1 PF _30h Access: Read/Write
Default Value: 48h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | Patt_En | Set to 1 enable Pattern_Fill to display |
| [6:4] | R/W | Patt_ColorDepth[2:0] | Defines nBP color:<br>000b: 8BPP<br>001b: 1BPP<br>010b: 2BPP<br>011b: 3BPP<br>100b: 4BPP<br>101b: 5BPP<br>110b: 6BPP<br>111b: 7BPP |
| [3:2] | R/W | Patt_RAM_Bit[1:0] | Defines the usage in Pattern RAM:<br>00b: 1 bit/pixel<br>01b: 2 bits/pixel<br>10b: 4 bits/pixel<br>11b: 8 bits/pixel |
| [1] | R/W | Patt_Independ_AB | Set to 1 for independent Alpha-Blending setting for Pattern_Fill;<br>set to 0 for by OSD1_0B |
| [0] | WO | Reset_PRAM_Pointer | Write 1 to reset the Pattern RAM pointer for loading pattern data |

### 2.7.3.5 OSD1 Pattern_Fill LUT Base Address Register

Address Offset: OSD1 PF _31h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:7] | R/W | Patt_LUT_BaseA[7:0] | Defines the MSB color in LUT for PatternFill color. Bit 0 is not used. |

### 2.7.3.6 OSD1 Pattern_Fill Pattern Horizontal Size Register

Address Offset: OSD1 PF _32h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_HSize[7:0] | For repeated pattern, this defines its width in the unit: Byte. |

### 2.7.3.7 OSD1 Pattern_Fill Pattern Vertical Size Register

Address Offset: OSD1 PF _33h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_VSize[7:0] | For repeated pattern, this defines its height in the unit: line. |

### 2.7.3.8 OSD1 Pattern_Fill Pattern Row Shift Register

Address Offset: OSD1 PF _34h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_Row_Shift[7:0] | For repeated pattern, this defines horizontal shift in the unit: Byte, to build a delta-type pattern. |

### 2.7.3.9 OSD1 Pattern_Fill Color High Bits Register

Address Offset: OSD1 PF _35h Access: Read/Write
Default Value: 05h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | RO | Reserved | |
| [3:0] | R/W | Patt_aB_ SourcePencent[3:0] | Alpha Blending percentage (n/16) for Filled patterns only.<br>If set 0000b, alpha blending is disabled (0/16 * Original Video Source + 8/8 * PatternFill display);<br>If set 0001b, blending as 1/16 * Original Video Source + 15/16 * PatternFill display;<br>. . .<br>If set N, blending as N/16 * Original Video Source + (16-N)/16 * PatternFill display; |

### 2.7.3.10 OSD1 BIST Result and Pattern Enlarge Register

Address Offset: OSD1 PF _36h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6] | RO | OSD1_PRAM_Fail | After OSD BIST done, get 1 in this bit shows the OSD1 PatternFill RAM is failed. |
| [5:4] | RO | Reserved | |
| [3:2] | R/W | Patt_V_Enlarge[1:0] | For each repeated pattern, enlarge it in verical direction |
| [1:0] | R/W | Patt_H_Enlarge[1:0] | For each repeated pattern, enlarge it in horizontal direction |

### 2.7.3.11 OSD1 Pattern_Fill Pattern RAM Write Port Register

Address Offset: OSD1 PF _37h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | PRAM_WrD_Port[10:8] | For building pattern, need to load via writing pattern to PRAM (Pattern RAM). After reset PRAM pointer, the PRAM pointer will increase after each burst write. |

### 2.7.3.12 OSD1 Pattern_Fill Position, Horizontal Start LSB Register

Address Offset: OSD1 PF _38h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_HStart[7:0] | Allowable pattern display region: horizontal start |

### 2.7.3.13 OSD1 Pattern_Fill Position, Horizontal Start MSB Register

Address Offset: OSD1 PF _39h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | Patt_HStart[10:8] | Allowable pattern display region: horizontal start |

### 2.7.3.14 OSD1 Pattern_Fill Position, Vertical Start LSB Register

Address Offset: OSD1 PF _3Ah Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_VStart[7:0] | Allowable pattern display region: vertical start |

### 2.7.3.15 OSD1 Pattern_Fill Position, Vertical Start MSB Register

Address Offset: OSD1 PF _3Bh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | Patt_VStart[10:8] | Allowable pattern display region: vertical start |

### 2.7.3.16 OSD1 Pattern_Fill Position, Horizontal End LSB Register

Address Offset: OSD1 PF _3Ch Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_HEnd[7:0] | Allowable pattern display region: horizontal End |

### 2.7.3.17 OSD1 Pattern_Fill Position, Horizontal End MSB Register

Address Offset: OSD1 PF _3Dh Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | Patt_HEnd[10:8] | Allowable pattern display region: horizontal End |

### 2.7.3.18 OSD1 Pattern_Fill Position, Vertical End LSB Register

Address Offset: OSD1 PF _3Eh Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Patt_VEnd[7:0] | Allowable pattern display region: vertical End |

### 2.7.3.19 OSD1 Pattern_Fill Position, Vertical End MSB Register

Address Offset: OSD1 PF _3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | Patt_VEnd[10:8] | Allowable pattern display region: vertical End |

# 3 Register Description

## *Serial Bus Register Set Page 0*

## 3.1 ADC Register Set

### 3.1.1 Mid-level Clamp Voltage Register

Address Offset: 05h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | B_Clamp_Volt_Sel[1:0] | Blue channel Clamp voltage select |
| [3:2] | R/W | G_Clamp_Volt_Sel[1:0] | Green channel Clamp voltage select |
| [1:0] | R/W | R_Clamp_Volt_Sel[1:0] | Red channel Clamp voltage select |

### 3.1.2 ADC Channel 0 Static Gain

Address Offset: 07h Access: Read/Write
Default Value: FFh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADCRSG | This register can set a fixed gain for ADC channel 0 when static gain control is enabled |

### 3.1.3 ADC Channel 1 Static Gain

Address Offset: 08h Access: Read/Write
Default Value: FFh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADCGSG | This register can set a fixed gain for ADC channel 1 when static gain control is enabled |

### 3.1.4 ADC Channel 2 Static Gain

Address Offset: 09h Access: Read/Write
Default Value: FFh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADCBSG | This register can set a fixed gain for ADC channel 2 when static gain control is enabled |

### 3.1.5 ADC Channel 0 Offset

Address Offset: 0Ah Access: Read/Write
Default Value: 60h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | R/W | ADC_ROFF | ADC Channel 0 DC Offset Control |
| [1:0] | RO | Reserved | |

### 3.1.6 ADC Channel 1 Offset

Address Offset: 0Bh Access: Read/Write
Default Value: 60h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | R/W | ADC_GOFF | ADC Channel 1 DC Offset Control |
| [1:0] | RO | Reserved | |

### 3.1.7 ADC Channel 2 Offset

Address Offset: 0Ch Access: Read/Write
Default Value: 60h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | R/W | ADC_BOFF | ADC Channel 2 DC Offset Control |
| [1:0] | RO | Reserved | |

### 3.1.8 ADC General Control Configuration Register

Address Offset: 0Dh Access: Read/Write
Default Value: 20h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6] | R/W | CLPMD | Clamping mode<br>Mode: Type<br>0: Fixed window<br>1: Locked Window |
| [5] | R/W | DCEN | DC Clamping Enable |
| [4] | R/W | DCSEL | Clamping Source Selection |
| [3] | R/W | Reserved | Test only, vmode |
| [2] | RO | DC_CAL_RDY | DC Calibration Ready |
| [1] | R/W | DC_CALEN | DC Calibration Enable |
| [0] | R/W | DC_CALMD | DC Calibration Mode<br>Mode: Type<br>0: minimum<br>1: average |

### 3.1.9 ADC Gain ReadBack

Address Offset: 0Eh Access: Read Only
Default Value: - Size: 6 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R | adc_auto_gain | ADC automatic gain control read back. |

### 3.1.10 ADC Power Down Control

Address Offset: 0Fh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | PwDn_SOY | 1 for Power down SOY slicer |
| [6] | R/W | PD2 (B) | 1: Power down<br>0: Power up |
| [5] | R/W | PD1 (G) | 1: Power down<br>0: Power up |

| | | | |
|---|---|---|---|
| [4] | R/W | PD0 (R) | 1: Power down<br>0: Power up |
| [3:1] | R/W | Reserved | |
| [0] | RO | Reserved | |

### 3.1.11 ADC Polarity Control

Address Offset: 10h Access: Read/Write
Default Value: E8h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO/WO | HSi_Polarity / HSi_Inv_ | When Read: get input HSync polarity<br>When writing, to invert (0) or non-invert (1) input HSync |
| [6] | RO/WO | VSi_Polarity / VSi_Inv_ | When Read: get input VSync polarity<br>When writing, to invert (0) or non-invert (1) input VSync |
| [5] | R/W | SOY_Inv_ | For invert (0) or non-invert (1) input SOY |
| [4] | R/W | Auto_Polarity | Set to 1 for enabling auto-adjusting HSync/VSync polarity. |
| [3] | R/W | Clamp_Polarity | Set to 1 for controlling Clamp positive polarity. |
| [2] | R/W | Clamp_Sel_GfbHS | Set to 1 to use PLL feedback HSync as clamp reference |
| [1] | R/W | Clamp_Leading | Set to 1 to use leading edge of HSync as clamp reference point. |
| [0] | R/W | Clamp_Sel_RGB | Clamp control by: 1: RGB/SOY logic, 0: VD logic. |

### 3.1.12 YPbPr Clamping Control Register

Address Offset: 11h Access: Read/Write
Default Value: 98h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | R/W | SOY_Threshold | Voltage threshold for SOY slicing |
| [4:3] | R/W | SOY_Discharge | SOY Discharge option |
| [2] | R/W | BSCALE | ADC Channel 2 Clamping Mode<br>0: Clamp to Ground; 1: Clamp to mid-scale |
| [1] | R/W | GSCALE | ADC Channel 1 Clamping Mode<br>0: Clamp to Ground; 1: Clamp to mid-scale |
| [0] | R/W | RSCALE | ADC Channel 0 Clamping Mode<br>0: Clamp to Ground; 1: Clamp to mid-scale |

### 3.1.13 SOY Slice Control

Address Offset: 12h Access: Read/Write
Default Value: 06h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO/WO | Done_ / En_Slicer_Status | When read: get flag of Slicer status ready or not<br>When write, to enable monitoring Slicer status |
| [6:5] | RO | Slicer_Status | 0:Slicer always low, 1: always high, 2: almost low, 3: almost high |
| [4] | R/W | Reserved | |
| [3:2] | R/W | SOY_ClampPlacement | SOY Clamp Placement |
| [1:0] | R/W | SOY_ClampDuration | SOY Clamp Duration. |

### 3.1.14 VSync Separation Register

Address Offset: 13h Access: Read/Write
Default Value: 08h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | CSync_Detect_Done | flag of whether CSync Detection is done or not |
| [6] | RO | Fs_TooFast | Get 1 if CSync Detecting operation clock is too fast |
| [5] | R/W | En_CSync_Detect | Set to 1 for enabling CSync Detection function |
| [4] | R/W | Reserved | Reserved for chip testing, should set 0 for normal operation |
| [3] | R/W | Reserved | Reserved for special case, set to 1 for normal conditions |
| [2] | R/W | Reserved | Reserved for special case, set to 0 for normal conditions |
| [1:0] | R/W | Div_To14[1:0] | 00b: power down or reset, 01b: XCLK/1,<br>10b:XCLK/2 (normal operation for XCLK=27MHz); 11b: XCLK/3 |

### 3.1.15 Sync Routine Control

Address Offset: 14h Access: Read/Write
Default Value: D1h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | HS2PLL_Polarity | HRef polarity |
| [6] | R/W | Coast2PLL_Polarity | Coast polarity |
| [5] | R/W | ADC_is_RGB | ADC Color space select: Set 1 for RGB input, 0 for YPbPr input. |
| [4] | R/W | HSo_Sel_Fdbk | ADC HSo source from PLL when set to 1 |
| [3] | R/W | HRef_Sel_SOY | PLL HRef from: 1: SOY Slicer (SOY); 0: HS input pin (SS/CS) |
| [2] | R/W | VS_Sel_Sep | ADC VSo from: 1: VSync Detect (SOY/CS); 0: VS input pin (SS) |
| [1] | R/W | Coast_Sel_Sep | PLL Coast from: 1: VSync Detect (SOY/CS); 0: Ground (SS) |
| [0] | R/W | Reserved | |

### 3.1.16 Line Lock PLL Divider Register 1

Address Offset: 15h Access: Read/Write
Default Value: 5Ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | APLL_Div[7:0] | PLL divider LSB |

### 3.1.17 Line Lock PLL Divider Register 2

Address Offset: 16h Access: Read/Write
Default Value: C3h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | APLL_PowerDown | 1: power down, 0: enable |
| [6] | R/W | APLL_Sel_HighFreq | Reserved for testing, 1: high freq., 0: low freq. |
| [5] | R/W | APLL_Reset | 1: Reset Line-lock PLL 0: normal operation for RGB and SOY inputs |
| [4] | RO | ADC_Clock_From | ADC clock source: 1: XCLK; 0:APLL output |
| [3:0] | R/W | APLL_Div[11:8] | PLL divider MSB |

### 3.1.18 VCO & Charge Pump Register

Address Offset: 17h Access: Read/Write
Default Value: 48h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | ADC_VCO | |
| [5:3] | R/W | ADC_ChargePump | |
| [2] | R/W | AutoClampV_B | Reserved for testing |
| [1] | R/W | AutoClampV_G | Reserved for testing |
| [0] | R/W | AutoClampV_R | Reserved for testing |

### 3.1.19 Analog Source MUX Selection

Address Offset: 18h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | AI2SEL (B) | Analog mux selection for ADC channel 2<br>00: ACB1<br>01: ACB0<br>1x: ACB2 |
| [3:2] | R/W | AI1SEL (G) | Analog mux selection for ADC channel 1<br>00: AY1<br>01: AY0<br>1x: AY2 |
| [1:0] | R/W | AI0SEL (R) | Analog mux selection for ADC channel 0<br>00: ACR1<br>01: ACR0<br>1x: ACR2 |

### 3.1.20 Y/Cb/Cr Data Switching Control

Address Offset: 19h Access: Read/Write
Default Value: 07h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | CBINSEL | The digitaized CB or B data can be taken from one of 3 ADCs:<br>00: ADC Ch0<br>01: ADC Ch1<br>1X: ADC Ch2 |
| [3:2] | R/W | YINSEL | The digitaized Y or Composite or G data can be taken from one of 3 ADCs:<br>00: ADC Ch0<br>01: ADC Ch1<br>1X: ADC Ch2 |
| [1:0] | R/W | CRINSEL | The digitaized CR or Chroma or R data can be taken from one of 3 ADCs:<br>00: ADC Ch0<br>01: ADC Ch1<br>1X: ADC Ch2 |

### 3.1.21 ADC Analog AGC Selection

Address Offset: 1Ah Access: Read/Write
Default Value: 87h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | AGC_GAINMD | Mode: Type<br>0: Positive gain<br>1: Positive gain 1x~2x<br>2: Negative gain 1x~2x<br>3: Negative gain |
| [5:3] | RO | Reserved | |
| [2] | R/W | CB_AGC_SEL | If 0, refer to ADCBSG (P0_09h):<br>0: Static gain; 1: Dynamic gain |
| [1] | R/W | Y_AGC_SEL | If 0, refer to ADCGSG (P0_08h)<br>0: Static gain; 1: Dynamic gain |
| [0] | R/W | CR_AGC_SEL | If 0, refer to ADCRSG (P0_07h)<br>0: Static gain; 1: Dynamic gain |

### 3.1.22 Blank Sync Level

Address Offset: 1Ch Access: Read/Write
Default Value: F0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BLANK_SL | |

### 3.1.23 ADC Phase Setting Register

Address Offset: 20h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | R/W | ADC_Phase[4:0] | 32 phases per clock |
| [2] | R/W | ADC_Clk_Div2 | Clock divided by 2 if set to 1 |
| [1] | R/W | ADC_Clk_Dly | Clock delay if set to 1 |
| [0] | R/W | ADC_Clk_Inv | Clock inverted if set to 1 |

### 3.1.24 ADC Detection Register

Address Offset: 21h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO/WO | Done_ATK /<br>En_ATK | When read: get flag of Phases Tracking finish or not<br>When write, to enable Phases Tracking |
| [6:5] | R/W | ATK_Channel[1:0] | Select which channel to perform ATK:<br>00: R+G+B<br>01: R<br>10: G<br>11: B |
| [4:3] | RO | Reserved | |
| [2] | RO/WO | Done_Exist_ADC /<br>En_Exist_ADC | When read: get flag of Checking ADC HS/VS finish or not<br>When write, to enable Checking ADC HS/VS |
| [1] | RO | Exist_HSync | HSync input toggle when read 1 |
| [0] | RO | Exist_VSync | HSync input toggle when read 1 |

### 3.1.25 ADC Phase Tracking Register 1

Address Offset: 22h Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | ATK_Accu[7:0] | Accumulated Phase Tracking Result |

### 3.1.26 ADC Phase Tracking Register 2

Address Offset: 23h Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | ATK_Accu[15:8] | Accumulated Phase Tracking Result |

### 3.1.27 ADC Phase Tracking Register 3

Address Offset: 24h Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | ATK_Accu[23:16] | Accumulated Phase Tracking Result |

### 3.1.28 Boundary Control Register

Address Offset: 26h Access: Read/Write
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO/WO | Done_Boundary / En_Boundary | When read: get flag of Boundary Detection finish or not<br>When write, to enable Boundary Detection |
| [6] | R/W | Boundary_hDE | Check boundary when:<br>0: in all range<br>1: in HDE window |
| [5:3] | R/W | Boundary_Mask_HS_L | Set the do not care range near HSync leading edge |
| [2:0] | R/W | Boundary_Mask_HS_T | Set the do not care range near HSync trailing edge |

### 3.1.29 Boundary Control Register

Address Offset: 27h Access: Read/Write
Default Value: 40h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Boundary_Threshold | Set the color threshold for boundary detection |

### 3.1.30 Boundary Left LSB Register

Address Offset: 28h Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | Left_Bound[7:0] | Left Boundary Position |

### 3.1.31 Boundary Left MSB Register

Address Offset: 29h Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | RO | Left_Bound[10:8] | Left Boundary Position |

### 3.1.32 Boundary Right LSB Register

Address Offset: 2Ah Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | Right_Bound[7:0] | Right Boundary Position |

### 3.1.33 Boundary Right MSB Register

Address Offset: 2Bh Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | RO | Right_Bound[10:8] | Right Boundary Position |

### 3.1.34 Boundary Top LSB Register

Address Offset: 2Ch Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | Top_Bound[7:0] | Top Boundary Position |

### 3.1.35 Boundary Top MSB Register

Address Offset: 2Dh Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | RO | Top_Bound[9:8] | Top Boundary Position |

### 3.1.36 Boundary Bottom LSB Register

Address Offset: 2Eh Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | Bottom_Bound[7:0] | Bottom Boundary Position |

### 3.1.37 Boundary Bottom MSB Register

Address Offset: 2Fh Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | RO | Bottom_Bound[9:8] | Bottom Boundary Position |

## 3.2 Input Timing Register Set

### 3.2.1 De-Interlaced Process & Vertical Shadow Control Register

Address Offset: 30h Access: Read/Write
Default Value: 82h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5] | R/W | VST_CHGSEL | 1:Vsync timing change determined by 8*# of XCLK<br>0:Vsync timing change determined by # of hsync (default)<br># can be assigned at Reg 0x3A |
| [4] | R/W | INT_EDGE | Interrupt polarity<br>1: positive<br>0: negative (default) |
| [3] | R/W | LB_SIZE_FIXED | This bit control capture size for Scaler.<br>1: Hsize and Vsize are assigned by 54h ~57h<br>0: sizes assigned by input sources. (default) |
| [2] | R/W | ENQKHS | Reserved for chip teset only, set to 0 for normal operation |
| [1] | R/W | ITLCPRO | Set 1 for interlaced video (default)<br>Set 0 for non-interlaced video |
| [0] | R/W | ADC_Odd_in_HsVs | Set to 1 for enabling detecting Odd flag from HS/VS pins |

### 3.2.2 Source Select Register

Address Offset: 31h Access: Read/Write
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | ITLCFLM | Indicates incoming video signal is interlaced if get 1 |
| [6:4] | R/W | VIP_Sel[2:0] | Select the digital input source (VIP: Video Input):<br>000: A656<br>001: B656<br>010: L601_8bits<br>011: L601_16bits<br>100: Reserved<br>101: RGB565<br>110: RGB666<br>111: RGB888 |
| [3:2] | R/W | InSource_Sel[1:0] | Select the input source:<br>00: Digital VIP input<br>01: select VD input (CVBS, S-Video, YPbPr)<br>10: Select ADC RGB, SOY(YPbPr)<br>11: Reserved |
| [1] | RO | Reserved | |
| [0] | RO | VBI_Field | Current VBI field information |

### 3.2.3 Interrupt Status Register

Address Offset: 32h Access: Read-only / Write-1-to-clear
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO/W1C | INTSTS | Read to get interrupt trigger source, Write 1 to clear it.<br>[7]: IR packet received<br>[6]: VBI packet is valid for processing<br>[5]: Every VSync Leading Edge<br>[4]: Timer time out<br>[3]: HSync Timing Changed<br>[2]: VSync Timing Changed<br>[1]: Lost HSync<br>[0]: Lost VSync |

### 3.2.4 Interrupt Mask Register

Address Offset: 33h Access: Read/Write
Default Value: FFh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | INTMASK | Set to 1 for masking relative interrupt trigger source:<br>[7]: IR packet received<br>[6]: VBI packet is valid for processing<br>[5]: Every VSync Leading Edge<br>[4]: Timer time out<br>[3]: HSync Timing Changed<br>[2]: VSync Timing Changed<br>[1]: Lost HSync<br>[0]: Lost VSync |

### 3.2.5 Interrupt Status/Mask 2 Register

Address Offset: 34h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | R/W | Reserved | |
| [4] | R/W | INTMASK_2 | Set to 1 for masking relative interrupt trigger source:<br>[4]: SAR1_Toggling |
| [3:1] | RO/W1C | Reserved | |
| [0] | RO/W1C | INTSTS_2 | Read to get interrupt trigger source, Write 1 to clear it.<br>[0]: SAR1_Toggling |

### 3.2.6 VD/656 Left Border Crop Register

Address Offset: 3Ch Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:0] | R/W | CROP_LEFTB | Remove noisy pixels appearing on left border.<br>1LSB =1 pixel |

### 3.2.7 VD/656 VSync Offset Register

Address Offset: 3Dh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | VD_VsOfs_Mode | VD/656 VSync Offset mode:<br>0: Crop Top Border<br>1: VSync Offset, delay lines |
| [6] | RO | Reserved | |
| [5:0] | R/W | VD_VsOffset | Remove noisy pixels appearing on top border or re-shape VSync<br>1LSB =1 line, value 0 means disable. |

### 3.2.8 VD/656 Left Border Crop Register

Address Offset: 3Eh Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | En_VD_VsOfs_P1 | Enable VSync Offset add 1 line for even or odd field on VD path |
| [6] | R/W | VD_VsOfs_on_Odd | Set to 1 for selecting VD VSync Offset delay 1 line on Odd field; Set to 0 for Even field. This bit works only when En_VD_VsOfs_P1=1. |
| [5:0] | R/W | VD_VsBP | VD/656 VSync Back Proch (# lines) |

### 3.2.9 Input Sync Signal Detection Register

Address Offset: 3Fh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | HSTLSPVS | 1:use trailing edge of hsync to sample<br>0:use leading edge of hsync to sample |
| [6] | R/W | AUTOVSD6 | When the edges of vsync and hsync are too close, input detection circuit can delay vsync 6 cycle of XCLK to avoid unstable detection<br><br>1:Automatically delay 6 cycles of XCLK if CFSEEDGE is true.<br>0:Dealy 6 cycles of XCLK if FCVSD6 is true |
| [5] | R/W | Reserved | |
| [4] | RO | CFSEEDGE | VS and HS edges are too close. |
| [3] | RO | HS_Polarity | Detected HSync polarity (for Analog RGB raw input) |
| [2] | RO | VS_Polarity | Detected VSync polarity (for Analog RGB raw input) |
| [1:0] | RO | Reserved | |

### 3.2.10 ADC Sync Offset Control Register

Address Offset: 40h Access: Read/Write
Default Value: D0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | En_HsOffset | Set to 1 for enabling ADC HSync Offset. |
| [6] | R/W | En_VsOffset | Set to 1 for enabling ADC VSync Offset. |
| [5] | R/W | En_VsOfs_Evn_P1 | Set to 1 for enabling ADC VSync Offset delay 1 line for even field. |
| [4] | R/W | SOY_Odd_Inv_ | Set to 0 for inverting SOY Odd field flag. |
| [3:2] | RO | Reserved | |
| [1] | R/W | RGB_PowerDown_ | Set to 0 for power down RGB related logic. 1 for enabling RGB path. |
| [0] | R/W | HS_in_SyncSel | Select the sampling edge of HSync pin. |

### 3.2.11 ADC HSync Offset LSB Register

Address Offset: 41h Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HsOffset[7:0] | Delay ADC HSync by # dots. |

### 3.2.12 ADC HSync Offset MSB Register

Address Offset: 42h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | HsOffset[10:8] | Delay ADC HSync by # dots. |

### 3.2.13 ADC VSync Offset LSB Register

Address Offset: 43h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | VsOffset[7:0] | Delay ADC VSync by # lines. |

### 3.2.14 ADC VSync Offset MSB Register

Address Offset: 44h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | VsOffset[9:8] | Delay ADC VSync by # lines. |

### 3.2.15 ADC HSync Offset Pulse Width Register

Address Offset: 45h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HsPulseWidth[7:0] | Pulse width of the regenerated ADC HSync (# dots). |

### 3.2.16 ADC VSync Offset Pulse Width Register

Address Offset: 46h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | RO | Reserved | |
| [3:0] | R/W | VsPulseWidth[3:0] | Pulse width of the regenerated ADC VSync (# lines). |

### 3.2.17 ADC Capture Control Register

Address Offset: 47h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | Mask_H_Left | Set to 1 for mask left portion when wrap. |
| [6] | R/W | Mask_H_Right | Set to 1 for mask right portion when wrap. |
| [5] | R/W | Mask_V_Top | Set to 1 for mask top portion when wrap. |
| [4] | R/W | Mask_V_Bottom | Set to 1 for mask bottom portion when wrap. |
| [3:1] | RO | Reserved | |
| [0] | R/W | Reserved | Reserved for chip test only |

### 3.2.18 ADC Capture HSize LSB Register

Address Offset: 48h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADC_HSize[7:0] | ADC Capture window: Horizontal Size (# dots). |

### 3.2.19 ADC Capture HSize MSB Register

Address Offset: 49h Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | ADC_HSize[10:8] | ADC Capture window: Horizontal Size (# dots). |

### 3.2.20 ADC Capture VSize LSB Register

Address Offset: 4Ah Access: Read/Write
Default Value: E0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADC_VSize[7:0] | ADC Capture window: Vertical Size (# lines). |

### 3.2.21 ADC Capture VSize MSB Register

Address Offset: 4Bh Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | ADC_VSize[9:8] | ADC Capture window: Vertical Size (# lines). |

### 3.2.22 ADC Capture HSync Back Porch LSB Register

Address Offset: 4Ch Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADC_HStart[7:0] | ADC Capture window: HSync Start Point (# dots). |

### 3.2.23 ADC Capture HSync Back Porch MSB Register

Address Offset: 4Dh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | ADC_HStart[10:8] | ADC Capture window: HSync Start Point (# dots). |

### 3.2.24 ADC Capture VSync Back Porch LSB Register

Address Offset: 4Eh Access: Read/Write
Default Value: 05h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ADC_VStart[7:0] | ADC Capture window: VSync Start Point (# linees). |

### 3.2.25 ADC Capture VSync Back Porch MSB Register

Address Offset: 4Fh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | ADC_VStart[9:8] | ADC Capture window: VSync Start Point (# linees). |

## 3.3 Picture Enhancement Register Set

### 3.3.1 DCTI Control Register

Address Offset: 60h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2] | R/W | DCTi_Dist_Sel | DCTI distance selection: 1 for longer distance |
| [1] | RO | Reserved | |
| [0] | R/W | DLTi_Dist_Sel | DLTI distance selection: 1 for longer distance |

### 3.3.2 Peaking Register

Address Offset: 61h Access:
Default Value: 08h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | Peaking_En | Enable Peaking function |
| [6] | R/W | Peaking_LR_Disable | Peaking boundary mode |
| [5:0] | R/W | Peaking_Coring | |

### 3.3.3 Peaking Band-Pass Coefficient Register

Address Offset: 62h Access:
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | Peaking_BP_Coef | |

### 3.3.4 Peaking High-Pass Coefficient Register

Address Offset: 63h Access:
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | Peaking_HP_Coef | |

### 3.3.5 Peaking Low-Pass Coefficient Register

Address Offset: 64h Access:
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [1:0] | R/W | Peaking_LP_Coef | |

### 3.3.6 DCTI_0 Gain and Coring Register

Address Offset: 65h Access: Read/Write
Default Value: 08h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | R/W | DCTI_GAIN_0 | |
| [4:0] | R/W | DCTI_CO_0 | |

### 3.3.7 DCTI_1 Gain and Coring Register

Address Offset: 66h Access: Read/Write
Default Value: 08h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | R/W | DCTI_GAIN_1 | |
| [4:0] | R/W | DCTI_CO_1 | |

### 3.3.8 Cb/Cr Delay control

Address Offset: 67h Access: Read/Write
Default Value: 1Eh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | U_delay | Cb signal delay control.<br>0: no delay (default)<br>1: 1 pixel delay |
| [6:5] | R/W | V_delay | Cr signal delay control.<br>00: no delay (default)<br>01: 1 pixel delay<br>10: 2 pixel delay<br>11: 3 pixel delay |
| [4:0] | R/W | DCTI_Threshold | DCTI performing Threshold Limit |

### 3.3.9 Contrast Adjust Register

Address Offset: 68h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | LumaCON | |

### 3.3.10 Brightness Adjust Register

Address Offset: 69h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | LumaBRI | |

### 3.3.11 Hue Sin Adjust Register

Address Offset: 6Ah Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HueSin | |

### 3.3.12 Hue Cos Adjust Register

Address Offset: 6Bh Access: Read/Write
Default Value: 7Fh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HueCos | |

### 3.3.13 Chroma Saturation Adjust Register

Address Offset: 6Ch Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | ChomSat | |

### 3.3.14 Black Level Expansion Threshold Register

Address Offset: 6Eh Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BLE_TH | |

### 3.3.15 VIP Black level Expansion Gain / Offset Control Register

Address Offset: 6Fh Access: Read/Write
DefaultValue: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | BLE_GAIN | |
| [3:2] | RO | Reserved | |
| [1:0] | R/W | BLE_OFFSET | |

## 3.4 Scaling Register Set

### 3.4.1 Scaling General Control Register

Address Offset: 70h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | Reserved | |
| [5] | R/W | Inv_VideoF | Inv_VideoF: Reverse input odd field control for intra-field scaling, only take action when ITLCPRO set to 1. |
| [4:3] | R/W | Reserved | |
| [2:1] | RO | Reserved | |
| [0] | WO | Coef_Pointer_Reset | Write 1 to reset pointer, must be performed before programming scaling coefficients. |

### 3.4.2 Horizontal Scale Step LSB Register

Address Offset: 72h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | H_Scale_Step [7:0] | |

### 3.4.3 Horizontal Scale Step MSB Register

Address Offset: 73h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | H_Scale_Step [15:8] | |

### 3.4.4 Vertical Scale Step LSB Register

Address Offset: 74h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | V_Scale_Step [7:0] | |

### 3.4.5 Vertical Scale Step MSB Register

Address Offset: 75h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | V_Scale_Step [15:8] | |

### 3.4.6 Horizontal Aspect Ratio LSB Register

Address Offset: 76h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | H_Aspect[7:0] | Horizontal Aspect Ratio [7:0] |

### 3.4.7 Horizontal Aspect Ratio MSB Register

Address Offset: 77h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | H_Aspect_En | Horizontal Aspect Ratio Enable |
| [6] | R/W | HASP_Center_Enlarge | Horizontal Aspect adjusting effect:<br>0: Center portion shrink<br>1: Center portion enlarge |
| [5:4] | RO | Reserved | |
| [3:0] | R/W | H_Aspect[11:8] | Horizontal Aspect Ratio [11:8] |

### 3.4.8 Low Pass Filter Register

Address Offset: 78h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | En_Half_input | Enable Low pass |
| [6] | RO | Reserved | |
| [5:4] | R/W | LP_Average[1:0] | Shift average level in Low Pass enabled |
| [3] | R/W | LP_Boundary_Dup | Duplicate the first dot or not |
| [2] | RO | Reserved | |
| [1:0] | R/W | LP_ShiftDot[1:0] | Shift dot count during Low Pass enabled |

### 3.4.9 Frame Color (Luma-Y) in Scaler Register

Address Offset: 7Dh Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Scale_Frame_Y[7:0] | Background (Frame) Y Color of Scaler. |

### 3.4.10 Frame Color (Chroma-U) in Scaler Register

Address Offset: 7Eh Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Scale_Frame_U[7:0] | Background (Frame) U Color of Scaler. |

### 3.4.11 Frame Color (Chroma-V) in Scaler Register

Address Offset: 7Fh Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Scale_Frame_V[7:0] | Background (Frame) V Color of Scaler. |

### 3.4.12 Line Buffer Configuration LSB Register

Address Offset: 84h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | LBPRFL[7:0] | LBPRFL can cause a time dealy in XCLK count between the leading edge of input Vsync and leading edge of output Vsync. |

### 3.4.13 Line Buffer Configuration MSB Register

Address Offset: 85h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | LBPRFL[15:8] | |

### 3.4.14 Left Display Border Configuration LSB Register

Address Offset: 88h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HLDSPLB[7:0] | When Output pixel's index is less than HRDSPLB, output pixel value is assigned as left display border with Frame color: {FMCLRRED, FMCLRGRN , FMCLRBLU} |

### 3.4.15 Left Display Border Configuration MSB Register

Address Offset: 89h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | HDSPLB_INV | Horizontal border is on if HDSPLB_INV is set as follows<br>1: HLDSPLB < Horizontal border < HRDSPLB<br>0: Horizontal border < HLDSPLB or it > HRDSPLB |
| [6] | R/w | VDSPLB_INV | Vertical border is on if VDSPLB_INV is set as follows<br>1: VTDSPLB < < VBDSPLB<br>0: Vertical border < VTDSPLB or it > VBDSPLB |
| [5] | R/W | HDSPLB_STY | Horizontal Border style<br>1: mesh<br>0: solid |
| [4] | R/W | VDSPLB_STY | Vertical Border style<br>1: mesh<br>0: solid |
| [3] | RO | Reserved | |
| [2:0] | R/W | HLDSPLB[10:8] | |

### 3.4.16 Right Display Border Configuration LSB Register

Address Offset: 8Ah Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HRDSPLB[7:0] | When Output pixel's index is greater than HRDSPLB, output pixel value is assigned as right display border with Frame color |

### 3.4.17 Right Display Border Configuration MSB Register

Address Offset: 8Bh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | HRDSPLB[10:8] | |

### 3.4.18 Top Display Border Configuration LSB Register

Address Offset: 8Ch Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | VTDSPLB[7:0] | |

### 3.4.19 Top Display Border Configuration MSB Register

Address Offset: 8Dh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | HDSPLB_GRID[1:0] | H grip precision,<br>00b: 1 pixel<br>01b: 4 pixels<br>10b: 16 pixels<br>11b: 32 pixels |
| [5:4] | R/W | VDSPLB_GRID[1:0] | V grip precision<br>00b: 1 line<br>01b: 4 lines<br>10b: 16 lines<br>11b: 32 lines |
| [3:2] | RO | Reserved | |
| [1:0] | R/W | VTDSPLB[9:8] | |

### 3.4.20 Bottom Display Border Configuration LSB Register

Address Offset: 8Eh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | VBDSPLB[7:0] | |

### 3.4.21 Bottom Display Border Configuration MSB Register

Address Offset: 8Fh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | VBDSPLB[9:8] | |

## 3.5 Gamma and Pattern Gen. Register Set

### 3.5.1 Image Function Control Register

Address Offset: 90h Access: Read/Write
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | GATS[1:0] | Gamma Table Select. Default=2'b00.<br>00b: All R/G/B Gamma tables<br>01b: B Gamma table<br>10b: G Gamma table<br>11b: R Gamma table |
| [5] | R/W | Gamma_BIST_En | Enable Gamma RAM BIST. |
| [4:2] | R/W | Reserved | |
| [1] | R/W | EN_GAMMA | Enable Gamma. |
| [0] | R/W | EN_DITHER | Enable Dithering:<br>0: Disable Dithering, output full 8 bit<br>1: 6 bits Dithering |

### 3.5.2 Built-in Pattern Generator Control Register

Address Offset: 91h Access: Read/Write
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | EFMCLR | Enable Frame background color<br>Turn on this bit may disable Scaler's color and show user-defined color on LCD panel.<br>See 0x9D, 0x9E and 0x9F for user-defined frame color. |
| [6] | R/W | ESLDSW | This bit may enable pattern generator shows 9 patterns sequentially.<br>EFMCLR, ESLDSW — Output<br>2'b0X — Normal Color<br>2'b10 — Still pattern<br>2'b11 — Motion patterns |
| [5] | R/W | EVBAR | Enable Vertical Bar Patterns |
| [4] | R/W | PLBIT | 1: indicate 8-bit patterns<br>0:indicate 6-bit patterns |
| [3:0] | R/W | PTN | Show nth pattern on LCD panel when EFMCLR is enabled<br>When Both EFMCLR and ESLDSW are enabled, pattern generator may show 0, 1 ,2 ...up to PTNth. |

### 3.5.3 GAMMA RAM BIST Result Register

Address Offset: 92h Access: Read/Write
Default Value: X0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Gamma_BIST_Done | When Gamma RAM BIST finish, this bit will be set to 1, then the other P0_92<6:4> bits are valid. |
| [6:4] | RO | Gamma_R/G/B_Fail | When Gamma RAM (R/G/B RAMs) BIST result: 0=pass, 1=fail. |
| [3:0] | RO | Reserved | |

### 3.5.4 GAMMA Table Address Port Register

Address Offset: 93h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | GAMMA_ADR | Gamma coefficient table address. The Index range is 00h~FFh |

### 3.5.5 GAMMA Table Write Data Port Register

Address Offset: 94h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | GAMMA_WR_D | Gamma coefficient write data port. |

### 3.5.6 Pattern Bar Width Register

Address Offset: 96h Access: Read/Write
Default Value: 3Ch Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | Pattern_Bar_Width | This is for generated pattern vertical bar width (for patterns: Color Bar or Gray ramp) |

### 3.5.7 Pattern Color Gradient & Dithering Mode Register

Address Offset: 9Ch Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | CLRGRDT[3:0] | When EFMCLR are enabled, CLRGRDT may set color gradient at pattern 2, 3 ,4, 5 |
| [3:0] | R/W | Reserved | |

### 3.5.8 Frame Color Red Configuration Register

Address Offset: 9Dh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | FMCLRRED | 8 bits of red color depth for frame color. |

### 3.5.9 Frame Color Green Configuration Register

Address Offset: 9Eh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | FMCLRGRN | 8 bits of green color depth for frame color. |

### 3.5.10 Frame Color Blue Configuration Register

Address Offset: 9Fh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | FMCLRBLU | 8 bits of blue color depth for frame color. |

## 3.6 OSD1 Register Set

(For detail OSD1 description, please refer to section 2.6 **OSD**.)

### 3.6.1 OSD1 Configuration Index Port Register

Address Offset: A0h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | W | OSD1_CFG_INDEX | OSD1 Configuration Address Port |

### 3.6.2 OSD1 Configuration Data Port Register

Address Offset: A1h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1_CFG_DATA | OSD1 Configuration Data Port |

### 3.6.3 OSD1 RAM Address Port Register

Address Offset: A2h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | OSD1_RAM_A | OSD1 RAM Address Port, LSB first, then MSB |
| [1] | RO | OSD1_RAM_Ready | OSD1 RAM is ready for next programming |
| [0] | RO | OSD1_Cfg_Ready | OSD1 configuration is ready for next programming |

### 3.6.4 OSD1 RAM Data Port Register

Address Offset: A3h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1_RAM_D | OSD1 RAM Data Port |

### 3.6.5 OSD1 Pattern Fill Configuration Index Port Register

Address Offset: A8h Access: Write Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | WO | OSD1PF_CFG_INDEX | OSD1 Pattern Fill Configuration Address Port |

### 3.6.6 OSD1 Pattern Fill Configuration Data Port Register

Address Offset: A9h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OSD1PF_CFG_DATA | OSD1 Pattern Fill Configuration Data Port |

## 3.7 LCD Output Control Register Set

### 3.7.1 Display Window Horizontal Start Register

Address Offset: B0h Access: Read/Write
Default Value: 20h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | DWHS_L[7:0] | Horizontal back porch. |

### 3.7.2 Display Window Vertical Start Register

Address Offset: B2h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | DWVS[7:0] | Vertical back porch |

### 3.7.3 Display Window Horizontal Width LSB Register

Address Offset: B4h Access: Read/Write
Default Value: E0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | DWHSZ[7:0] | Horizontal Active. |

### 3.7.4 Display Window Horizontal Width MSB Register

Address Offset: B5h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | DWHSZ[10:8] | Horizontal Active. |

### 3.7.5 Display Window Vertical Width LSB Register

Address Offset: B6h Access: Read/Write
Default Value: EAh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | DWVSZ[7:0] | Vertical Active. |

### 3.7.6 Display Window Vertical Width MSB Register

Address Offset: B7h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | DWVSZ[9:8] | |

### 3.7.7 Display Panel Horizontal Total Dots per Scan Line LSB Register

Address Offset: B8h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | PH_TOT[7:0] | Output horizontal total dots |

### 3.7.8 Display Panel Horizontal Total Dots per Scan Line MSB Register

Address Offset: B9h Access: Read/Write
Default Value: 03h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | PH_TOT[10:8] | |

### 3.7.9 Display Panel Vertical Total Lines per Frame LSB Register

Address Offset: BAh Access: Read/Write
Default Value: 58h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | PV_TOT[7:0] | Output vertical total lines |

### 3.7.10 Display Panel Vertical Total Lines per Frame MSB Register

Address Offset: BBh Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | PV_TOT[9:8] | |

### 3.7.11 Display Panel HSYNC Width Register

Address Offset: BCh Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | PH_PW[7:0] | |

### 3.7.12 Display Panel VSYNC Width Register

Address Offset: BEh Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | PV_PW[4:0] | |

### 3.7.13 Panel Output Signal Control 1 Register

Address Offset: C0h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | Reserved | |
| [6] | RO | Reserved | |
| [5] | R/W | En_sPanel | Enable Serial RGB (sPanel) output.<br>0: for Analog panel (DAC output with TCON)<br>1: for Serial RGB panel (sD[7:0] + DCLKO + HS/VS/HDE) |
| [4] | R/W | Reserved | |
| [3] | R/W | Data_Neg | Reverse RGB output.<br>0: No reverse<br>1: RGB reverse. |
| [2] | R/W | PHSync_Polarity | PHSYNC Polarity. Default=0.<br>0: Active Low<br>1: Active High |
| [1] | R/W | PVSync_Polarity | PVSYNC Polarity. Default=0.<br>0: Active Low<br>1: Active High |
| [0] | R/W | PHDE_Polarity | PDE polarity. Default=1.<br>0: Active Low<br>1: Active High |

### 3.7.14 Panel Output Signal Control 3 Register

Address Offset: C1h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | Reserved | |
| [3] | R/W | DCLK_INV | CLKO Polarity. Default=0.<br>0: Non-Invert, CLKO rising aligns to Data transition<br>1: Inverted, CLKO falling aligns to Data transition |
| [2:1] | RO | Reserved | |
| [0] | R/W | Half_CPHn | Half CPHn frequency when set to 1. |

### 3.7.15 Panel VSYNC Frame Delay Control Register

Address Offset: C2h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6:5] | R/W | Reserved | |
| [4] | R/W | PSYNC_STR | For Frame lock, input VSync (if exist) will trigger output VSync<br>0: Allow input vsync to trigger output vsync<br>1: Block input vsync triggering on output vsync |
| [3] | R/W | Reserved | |
| [2] | RO | Reserved | |
| [1] | R/W | IGNORE_VSYNC | Ignore the input VSYNC. This can be used for output free run when input VSYN is not available |
| [0] | WO | Reserved | For Chip Test only |

### 3.7.16 Serial RGB HSync Delay Register

Address Offset: C5h Access: Read/Write
Default Value: 60h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | sPanel_HS_Delay[7:0] | Delay output HSync for sPanel. (count in 3x panel clock) Value must >= 02h. This register is used to shift sPanel_HS, and align correct RGB color in sequence, for some sPanel do not have HDE input. |

### 3.7.17 Output RGB Reordering Register

Address Offset: C7h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6:4] | R/W | Reserved | |
| [3] | R/W | BIGENDIANE | Reverse bit [7:0] of RGB:<br>0: Non-Inverted, Little Endian.<br>1: Inverted, Big Endian. |
| [2:0] | R/W | RGBSWAPE | RGB Channel Swapping |

### 3.7.18 Output PLL Divider 1 Register

Address Offset: C8h Access: Read/Write
Default Value: 15h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6:0] | R/W | PLLDIV_F | PLL feedback divider. |

### 3.7.19 Output PLL Divider 2 Register

Address Offset: C9h Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | SS_Clock_En | Enable Spread Spectrum clock output |
| [6:5] | R/W | SS_Clock_Deviation[1:0] | Spread Spectrum clock deviation selection |
| [4:0] | R/W | PLLDIV_I | PLL Input Divider. |

### 3.7.20 Output PLL Divider 3 Register

Address Offset: CAh Access: Read/Write
Default Value: 03h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | PLLMX | PLL MUX Function Select<br>PLLMX: Mode<br>2'b00: PLLCLK<br>2'b01: Keep High<br>2'b10: Bypass PLL<br>2'b11: Bypass PLL |
| [5] | R/W | PLLPD | Display PLL power down Control:<br>0: Display PLL power on<br>1: Display PLL power down |
| [4] | R/W | PLL_Div2 | Display PLL analog divider, set 1 to half frequency output |

| | | | |
|---|---|---|---|
| [3:2] | R/W | PLL_OUT_SEL | PLL additional divider<br>0: no divider<br>1: divided by 2<br>2: divided by 4<br>3: divided by 8 |
| [1:0] | R/W | PLLDIV_O | PLL Output Divider. Default=1.<br>output_freq = 27Mhz * (F + 2) / (I+2) / (2^(O+1) ) |

### 3.7.21 LLCKn Clock Register

Address Offset: CBh Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | LLCK1_Phase[3:0] | CPH1 (LLCK1) phase, 1<= value <= LLCK_DivideN[3:0] |
| [3:0] | R/W | LLCK_DivideN[3:0] | LLCK pre-divider. 0/1 for no divide; |

### 3.7.22 Output LLCK Control 2 Register

Address Offset: CCh Access: Read/Write
Default Value: 32h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | LLCK3_Phase[3:0] | CPH3 (LLCK3) phase, 1<= value <= LLCK_DivideN[3:0] |
| [3:0] | R/W | LLCK2_Phase[3:0] | CPH2 (LLCK2) phase, 1<= value <= LLCK_DivideN[3:0] |

### 3.7.23 Display Window Horizontal Start Register

Address Offset: D8h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HMDISP_STR[7:0] | |

### 3.7.24 Display Window Vertical Start Register

Address Offset: DAh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | VMDISP_STR | |

### 3.7.25 Display Window Horizontal Size LSB Register

Address Offset: DCh Access: Read/Write
Default Value: E0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HMDISP_SIZE[7:0] | |

### 3.7.26 Display Window Horizontal Size MSB Register

Address Offset: DDh Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | HMDISP_SIZE[10:8] | |

### 3.7.27 Display Window Vertical Size LSB Register

Address Offset: DEh Access: Read/Write
Default Value: EAh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | VMDISP_SIZE[7:0] | |

### 3.7.28 Display Window Vertical Size MSB Register

Address Offset: DFh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | VMDISP_SIZE[9:8] | |

## 3.8 Global Control Register Set

### 3.8.1 Power Management Control Register

Address Offset: E0h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | PD_TotalPad_ | Set to 0 for Power Down all I/O pads, except $I^2C$ I/F. |
| [6] | R/W | PD_ADCD_ | Set to 0 for Power Down ADC digital portion. |
| [5] | R/W | PD_VIP_ | Power down ITU-R656, L601 interface, active low |
| [4] | R/W | PD_VD_ | Set to 0 for Power Down Comb Video Decoder block. |
| [3] | R/W | LLCK1_EN | LLCK1 enable |
| [2] | R/W | LLCK2_EN | LLCK2 enable |
| [1] | R/W | LLCK3_EN | LLCK3 enable |
| [0] | R/W | PD_TC_ | Set to 0 for Power down TC interface. |

### 3.8.2 Output Pin Configuration

Address Offset: E1h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | RowSTV_Sel | RowSTV_Sel: Mode<br>2'b00: Output both<br>2'b01: Output both<br>2'b10: Output STV1<br>2'b11: Output STV2 |
| [5:4] | R/W | ColSTH_Sel | ColSTH_Sel: Mode<br>2'b00: Output both<br>2'b01: Output both<br>2'b10: Output STH1<br>2'b11: Output STH2 |
| [3] | R/W | UD_Sel | Set UD output value |
| [2] | R/W | RL_Sel | Set RL output value |
| [1:0] | RO | Reserved | |

### 3.8.3 Shadow Control Configuration

Address Offset: E2h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4] | R/W | Shadow_Enable | 1: Enable registers shadow control |
| [3:1] | RO | Reserved | |
| [0] | WO | Shadow_Sync | Write 1 to sync all shadowed registers |

### 3.8.4 DAC Power Management

Address Offset: E3h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | PDn_Bias | 1: power down Bias circuit<br>0: power on Bias circuit |
| [6] | R/W | PDn_VCOM | 1: power down Analog VCOM Amp circuit<br>0: power on Analog VCOM Amp circuit |
| [5] | R/W | PDn_Regulator | 1: power down Regulator circuit<br>0: power on Regulator circuit |
| [4] | R/W | PDn_DC2DC | 1: power on DC to DC circuit<br>0: power down DC to DC circuit |
| [3] | R/W | SL | 1: power down 3 channels<br>0: power on 3 channels |
| [2] | R/W | SLR | 1: power down R channel<br>0: power on R channel |
| [1] | R/W | SLG | 1: power down G channel<br>0: power on G channel |
| [0] | R/W | SLB | 1: power down B channel<br>0: power on B channel |

### 3.8.5 Analog Output Current 1 Register

Address Offset: E4h Access: Read/Write
Default Value: 0Fh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | R/W | VCOM_DC[2:0] | LSB of VCOM DC setting |
| [4:0] | R/W | DAC_Amp[4:0] | DAC Amp setting |

### 3.8.6 Analog Output Current 2 Register

Address Offset: E5h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | VCOM_VoltagePeak | VCOM voltage peak setting |
| [6:5] | R/W | VCOM_DC[4:3] | MSB of VCOM DC setting |
| [4:0] | R/W | VCOM_Amp[4:0] | VCOM Amp setting |

### 3.8.7 Power Down Register

Address Offset: E6h Access: Read/Write
Default Value: 3Ch Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | PD_CombLB | 1: power down Video Decoder Comb Line Buffers<br>0: power on Video Decoder Comb Line Buffers |
| [6] | R/W | PD_XCLK2MC | 1: Tri-state XCLK2MC output<br>0: Allow XCLK2MC output |
| [5] | R/W | PDn_LED | 1: power on LED circuit<br>0: power down LED circuit |
| [4] | R/W | PDn_Inverter | 1: power on Inverter circuit<br>0: power down Inverter circuit |
| [3] | R/W | OpnLmpPrtct_En | 1 for Open Lamp Protection Enabled; else disabled |
| [2:0] | R/W | BackLight_Dim [2:0] | Back Light Dim level control. |

### 3.8.8 CCFL/LED Control Register

Address Offset: E7h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | DIM_Source_Sel | DIM PWM source select:<br>0: analog PWM<br>1: digital PWM |
| [6] | R/W | DeadTimeControl | Dead Timer Control |
| [5:4] | R/W | OpnLmp_Current[1:0] | Open Lamp Current setting |
| [3:0] | R/W | Inverter_Freq_Sel[1:0] | Inverter frequency selection |

### 3.8.9 PWM_1 General Control Register

Address Offset: E8h Access: Read/Write
Default Value: 07h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | R/W | PWM1_Low[4:3] | |
| [5] | R/W | PWM1_Alt_Mode | 1: Alternative PWM1 mode; 0: Legacy {PWM1_High/256} mode |
| [4] | R/W | PWM1_En | Enable PWM_1 |
| [3] | RO | Reserved | |
| [2:0] | R/W | PWM1_Freq_Sel | This register set the PWM1 counter base clock = XCLK / 2^N, N=0, 1, 2, 3, 5, 7, 9, 11. That is, the PWM1 freq = PWM1 base clock freq / 256. |

### 3.8.10 PWM_1 Active High Time Counter Register

Address Offset: E9h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | R/W | PWM1_High[7:5] / PWM1_Low[2:0] | InPWM1 legacy mode, this register set PWM1 high time (PWM1_High[7:0]/256) counted by PWM1 base clock.<br>In PWM1 Alternative mode, the PWM1 output: PWM1_High[4:0] / ( PWM1_Low[4:0] + PWM1_High[4:0]), based clock is divide from XCLK , see P0_E8<2:0> |
| [4:0] | R/W | PWM1_High[4:0] | This register set PWM1 high time counted by PWM1 base clock. The based clock is divide from XCLK , see P0_E8<2:0> |

### 3.8.11 PWM_2 General Control Register

Address Offset: EAh Access: Read/Write
Default Value: 27h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | PWM2_Fine_Freq_Mode | Select PWM_2 operating clock mode:<br>0: original XCLK/2^n mode, same as PWM1<br>1: fine frequency mode, XCLK/PWM2_Fine_Freq[10:0] |
| [6] | R/W | PWM2_Cfg_FineFreq | Select which setting for programming<br>1: allow configuring clock divider: PWM2_Fine_Freq[10:0];<br>0: configure original PWM2_Freq_Sel[2:0] and PWM2_High[7:0] |
| [5] | R/W | CCFL_PWM_Sel | Select digital PWM output to CCFL:<br>0: PWM1 output<br>1: PWM2 output |
| [4] | R/W | PWM2_En | Enable PWM_2 |
| [3] | RO | Reserved | |

| | | | |
|---|---|---|---|
| [2:0] | R/W | PWM2_Freq_Sel[3:0]<br>or<br>PWM2_Fine_Freq[10:8] | When PWM2_Cfg_FineFreq=0, these bits select PWM2 counter base clock = XCLK / 2^(2*n+3), That is, the PWM2 freq = PWM2 base clock freq / 256.<br>When PWM2_Cfg_FineFreq=1, these bits as MSB for PWM2 clock divider. |

### 3.8.12 PWM_2 Active High Time Counter Register

Address Offset: EBh Access: Read/Write
Default Value: 80h/D1h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | PWM2_High[7:0]<br>or<br>PWM2_Fine_Freq[7:0] | When PWM2_Cfg_FineFreq=0, this register sets PWM2 high time counted by PWM2 base clock. Default value is 80h. The based clock is divide from XCLK , see P0_EA<2:0>.<br>When PWM2_Cfg_FineFreq=1, this register as LSB for PWM2 clock divider. Default value is D1h. |

### 3.8.13 DAC Offset Control Register

Address Offset: EDh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | DAC_Offset[4:0] | DAC Offset setting |

### 3.8.14 Serial Bus Control Register

Address Offset: F1h Access: Read/Write
Default Value: C4h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | SCL_Out | SCL output value, when i8051 enabled and acts as an I2C master |
| [6] | RO | SCL_In | SCL input status |
| [5] | R/W | SDA_Out | SDA output value, when i8051 enabled and acts as an I2C master |
| [4] | RO | SDA_In | SDA input status |
| [3] | R/W | XBus_En | Reserved for chip testing |
| [2] | R/W | I2CATINCADR | Set to 1 for enabling 2-wire serial bus automatic address increment in multiple R/W Access mode. Default=1'b1. |
| [1:0] | RO | Reserved | |

### 3.8.15 Vendor ID 1 Register

Address Offset: F3h Access: Read Only
Default Value: 54h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | VID_L | Reading this register obtains ASCII code "T". |

### 3.8.16 Vendor ID 2 Register

Address Offset: F4h Access: Read Only
Default Value: 57h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | VID_H | Reading this register obtains ASCII code "W". |

### 3.8.17 Device ID Register

Address Offset: F5h Access: Read Only
Default Value: C8h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | DID | This field puts a part number in Hex “C8” as T108 |

### 3.8.18 Revision ID Register

Address Offset: F6h Access: Read Only
Default Value: A4h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | RO | RID | This field puts a revision number in Hex “A3”. |

### 3.8.19 SRAM BIST Enable Register

Address Offset: F8h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | Reserved | |
| [6:5] | RO | Reserved | |
| [4] | R/W | En_8051RAM_BIST | Enable Cache RAM, iRAM, xRAM BIST, if set to 1. |
| [3] | R/W | En_VBI_BIST | Enable VBI RAM BIST, if set to 1. |
| [2] | R/W | En_OSD_BIST | Enable OSD1 RAM/ROM BIST, if set to 1. |
| [1] | R/W | En_Comb_BIST | Enable VD Comb RAM BIST, if set to 1. |
| [0] | R/W | En_SM_BIST | Enable Scaler Machine LB RAM BIST, if set to 1. |

### 3.8.20 SRAM BIST Finish Register

Address Offset: F9h Access: Read Only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5] | RO | Done_VHalf_BIST | V_Half Line Buffer BIST finish if get 1. |
| [4] | RO | Done_8051RAM_BIST | Cache RAM, iRAM, xRAM BIST finish if get 1. |
| [3] | RO | Done_VBI_BIST | VBI RAM BIST finish if get 1. |
| [2] | RO | Done_OSD_BIST | OSD1 RAM/ROM BIST finish if get 1. |
| [1] | RO | Done_Comb_BIST | VD Comb RAM BIST finish if get 1. |
| [0] | RO | Done_SM_BIST | Scaler Machine LB RAM BIST finish if get 1. |

### 3.8.21 SRAM BIST Result Register 1

Address Offset: FAh Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | VBI_RAM_Fail | VBI RAM BIST fail if get 1. |
| [6] | RO | OSD1_BDSRAM_Fail | OSD1 BDSRAM BIST fail if get 1. |
| [5] | RO | OSD1_ORAM_Fail | OSD1 ORAM BIST fail if get 1. |
| [4] | RO | Comb_BIST_fail | VD Comb RAM BIST fail if get 1. |
| [3:0] | RO | SM[3:0]_BIST | Scaler Machine LB[3:0] BIST fail if get 1. |

### 3.8.22 SRAM BIST Result Register 2

Address Offset: FBh Access: Read Only
Default Value: XXh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | RO | Reserved | |
| [5] | RO | VHalf_Buffer_Fail | V_Half buffer fail if get 1. |
| [4] | RO | CacheH_Fail | 8051 Cache high 8KB RAM BIST fail if get 1. |
| [3] | RO | CacheL_Fail | 8051 Cache low 8KB RAM BIST fail if get 1. |
| [2] | RO | xRAM_Fail | 8051 external RAM BIST fail if get 1. |
| [1] | RO | iRAM_fail | 8051 internal RAM BIST fail if get 1. |
| [0] | RO | Reserved | |

### 3.8.23 Pin Function Select Register

Address Offset: FEh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | :Description |
|---|---|---|---|
| [7] | R/W | GPOA54_as_UDRL | GPOA[5:4] act as:<br>0: GPOA[5:4] (controlled by P1_51<5:4>);<br>1: UD and RL (controlled by P0_E1<3:2>) |
| [6] | R/W | GPOA321_as_TCON | GPOA[3:1] act as:<br>0: GPOA[3:1] (controlled by P1_51<3:1>);<br>1: TCON: STB/CKVB (inverted of some TCON signals) |
| [5] | R/W | GPIC_from_LVY | GPIC[7:0] input from:<br>0: GPIC[7:0] mux-ed pins;<br>1: LVY[7:0] pins |
| [4:2] | R/W | Reserved | |
| [1] | R/W | BYPS_DAC | For chip testing DAC block |
| [0] | R/W | BYPS_ADC | For chip testing ADC block |

### 3.8.24 Page Select Register

Address Offset: FFh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W | PAGE[1:0] | |

# Serial Bus Register Set Page 1

## 3.9 TCON Register Set

### 3.9.1 Timing Controller (TCON) Control Register

Address Offset: 20h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | GScanInt | Enable interlaced scanning<br>Mode 0: Type Processive<br>Mode 1: Type Interlacing |
| [6] | R/W | DDR_GDRV | Enable DDR gate driver<br>Mode 0: Type 1 line/GCLK<br>Mode 1: Type 2 lines/GLK |
| [5] | R/W | GTOE | Enable gate driver output<br>Mode 0: Type Shutdown output<br>Mode 1: Type Enable |
| [4] | R/W | DbScan_Edge | Clock edge of STV<br>When DbScan_STV_1p is enabled, DbScan_Edge can control STV alignment with the falling edge o rising edge of GCLK<br>Mode 0: Type Falling edge of GCLK<br>Mode 1: Type Rising edge of GCLK |
| [3] | R/W | DbScan_STV_1p5 | STV 1.5 lines wide<br>Mode 0: Type 1 line wide<br>Mode 1: Type 1.5 lines wide |
| [2] | R/W | DbScan_En | Gate driver Scanning control<br>Mode 0: Type 1 GCLK/line<br>Mode 1: Type 2 GCLKs/line |
| [1] | R/W | Q1HPL | Q1H polarity<br>Mode 0: Type Negative<br>Mode 1: Type Positive |
| [0] | R/W | PNINV | Enable line-inverted function. |

### 3.9.2 Timing Protocol & Polarity Control Register

Address Offset: 21h Access: Read/Write
Default Value: FFh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RW | DRVRSTPL | This bit may control Source Drive Reset polarity<br>When P0_E1h<7:6> is not 11b, pin STV2 becomes the rese of source driver. |
| [6] | R/W | GTOEPL | This bit may control GOE polarity<br>Mode Type<br>0 Low-active<br>1 Highactive |
| [5] | R/W | STVPL | Row Driver start pulse polarity<br>Mode Type<br>0 Negative<br>1 Positive |
| [4] | R/W | CLKVPL | Data Inversion Polarity<br>Mode Type<br>0 Negative<br>1 Positive |
| [3] | R/W | FLD1PL | Video Field Polarity<br>Mode Type<br>0 Inverted field flag<br>1 Non-inverted field flag |
| [2] | R/W | POLPL | Column Driver POL inversion polarity<br>Mode Type<br>0 Negative<br>1 Positive |
| [1] | R/W | LPPL | Column Driver Latch Pulse polarity<br>Mode Type<br>0 Negative<br>1 Positive |
| [0] | R/W | STHPL | Column Driver Start Pulse polarity<br>Mode Type<br>0 Negative<br>1 Positive |

## 3.10 Infra-Red Register Set

### 3.10.1 IR Sampling Tick LSB Register

Address Offset: 40h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | IR_Tick[7:0] | Sampling Tick LSB byte (Unit: XCLK is 27MHz):<br>NEC mode: 560μs (3B10h);<br>Philips RC5 mode: 900μs (5EECh) |

### 3.10.2 IR Sampling Tick MSB Register

Address Offset: 41h Access: Read/Write
Default Value: 3Bh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | IR_Tick[15:8] | Sampling Tick MSB byte. |

### 3.10.3 IR Stream 1~4 Register (when IR_Counter_Mode=0)

Address Offset: 42h~45h Access: Read Only
Default Value: --h Size: 32 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0]<br>x4 | RO | IR_Stream[0..31] | Decoded IR stream (packet) stored in P1_42h~45h<br>The first received bit is IR_Stream[0], then the next IR_Stream[1], …. and the last available bit is IR_Stream[31] if packet that long.<br>IR_Stream[7:0] in P1_42, IR_Stream[15:8] in P1_43,<br>IR_Stream[23:16] in P1_44, IR_Stream[31:24] in P1_45; |

### 3.10.4 IR Duration 1~3 Register (when IR_Counter_Mode=1)

Address Offset: 42h~44h Access: Read Only
Default Value: --h Size: 24 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0]<br>x3 | RO | IR_Duration[0..21]<br>(P1_44<7:6> are 00b) | The duration (count in XCLK) of input IR. When IR protocol is not supported, F/W can use this counter result and IR interrupt to decode. |

### 3.10.5 IR Stream 1 Register

Address Offset: 47h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | IR_En | Enable IR Decoder. |
| [6] | R/W | IR_Counter_Mode | Set to 0 for supported IR protocols;<br>Set to 1 for monitoring IR transition duration (count in XCLK) |
| [5:4] | R/W | IR_Mode[1:0] | IR Decoder Mode:<br>00: NEC mode; 01: Philips RC5 mode; 1X: Sony mode |
| [3] | R/W | IR_Invert | Invert IR1 input to IR Decoder. |
| [2] | RO | IR_Value | Current IR value (high or low) |
| [1] | RO | IR_Overflow | IR duration counter overflow if get 1, then the |
| [0] | RO | IR_Repeat | Getting 1 indicates the current IR packet is Repeat. |

## 3.11 ITU - 656 Decoder Register Set

### 3.11.1 ITU-656 Decoder HS Delay Register

Address Offset: D0h Access: Read/Write
Default Value: 30h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HS_DELAY656[7:0] | Unit: Cycles of Half VCLK |

### 3.11.2 ITU-656 Decoder HS Pulse Width Register

Address Offset: D2h Access: Read/Write
Default Value: 10h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:3] | R/W | HS_WIDTH656[5:3] | Unit: Cycles of Half VCLK, HS_WIDTH656[2:0] = 000b |
| [2:0] | RO | Reserved | |

### 3.11.3 ITU-656 Decoder VS Delay Register

Address Offset: D3h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | Reserved | |
| [4:0] | R/W | VS_DELAY656[4:0] | Unit: HS |

### 3.11.4 ITU-656 Decoder VS Pulse Width Register

Address Offset: D4h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | VS_in_LineCnt | 0: VSync Delay/Width in VCLK count (for those digital video inputs which have no HREF or its codeword during vertical blank)<br>1: VSync Delay/Width in Line count (for those digital video inputs which keeps sending HREF or its codeword during Vertical Blank) |
| [6] | R/W | VS_Ex1_Odd | Set to 1 for extra 1 line VSync Offset for Odd field |
| [5] | R/W | VS_Ex1_Evn | Set to 1 for extra 1 line VSync Offset for Even field |
| [4:2] | RO | Reserved | |
| [1:0] | R/W | VS_WIDTH656[1:0] | Unit: HS |

### 3.11.5 ITU-656 Decoder HDE Start Register

Address Offset: D5h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HSTART656[7:0] | Unit: Pixel |

### 3.11.6 ITU-656 Decoder HDE Size LSB Register

Address Offset: D7h Access: Read/Write
Default Value: D0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W or RO | HSIZE656[7:0] | Unit: Pixel, RO if SIZE_DET=1; else R/W |

### 3.11.7 ITU-656 Decoder HDE Size MSB Register

Address Offset: D8h Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W or RO | HSIZE656[10:8] | Unit: Pixel |

### 3.11.8 ITU-656 Decoder Odd Field VDE Start Register

Address Offset: D9h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | OVSTART656[7:0] | Odd Filed VDE Start, Unit: HS |

### 3.11.9 ITU-656 Decoder Odd/Even Field VDE Start Register

Address Offset: DAh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | EVPluse1 | Even Filed VDE Start<br>1: EVSTART656=OVSTART + 1<br>0: EVSTART656=OVSTART |
| [6:0] | RO | Reserved | |

### 3.11.10 ITU-656 Decoder VDE Size LSB Register

Address Offset: DBh Access: Read/Write
Default Value: F0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W or RO | VSIZE656[7:0] | Unit: HS, RO if SIZE_DET=1; else R/W |

### 3.11.11 ITU-656 Decoder VDE Size MSB Register

Address Offset: DCh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:2] | RO | Reserved | |
| [1:0] | R/W or RO | VSIZE656[9:8] | Unit: HS |

### 3.11.12 ITU-656 Decoder VCLK Tuning Register

Address Offset: DEh Access: Read/Write
Default Value: 02h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6] | R/W | LHDE_Yes | Enable LHDE input for digital RGB input:<br>0: Ignore LHDE, then requiring setting capture window<br>1: Use LHDE to capture active window |
| [5] | R/W | LODD_INV | Set to 1 for invert LODD/LVSYNC pin |
| [4] | R/W | LODD_is_VSYNC | Set to 1 if LODD pin acts as VSYNC input |
| [3] | R/W | LHREF_INV | to 1 for invert LHREF/LHSYNC pin |
| [2] | R/W | LFIEDLD_in_LHREF | Set to 1 for enabling extract Odd flag from LHREF pin |
| [1] | R/W | VCLK_INV | VCLK skew: invert |
| [0] | R/W | VCLK_DLY | VCLK skew: delay |

### 3.11.13 ITU-656 Decoder Format Control Register

Address Offset: DFh Access: Read/Write
Default Value: 40h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6] | R/W | ODDF_INV | Filed flag indicator<br>0: 1st field =0, 2nd field=1<br>1: 1st filed =1, 2nd field=0 |
| [5] | R/W | ReSync_OddF | Set to 1 for re-synchronizing Odd Flag |
| [4] | R/W | RGB_for_HDTV | Option different color space convert coefficient set |
| [3] | R/W | A656_V_Align | Chroma_V pixel alignment |
| [2] | R/W | A656_UV_Intrplt | Interpolate UV pixel values when 422 => 444 converting |
| [1] | R/W | SIZE_DET | Read back Size of HDE and VDE<br>0:Disable<br>1:Enable |
| [0] | R/W | Detect_Update_ | Size detect result update allow, depends on:<br>0:Update current detection<br>1:Keep previous detection |

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## 3.12 Y/C Separation and Chroma Decoder Register Set

### 3.12.1 Video Source Selection of Comb Filter Register

Address Offset: 00h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5] | R/W | PIXEL_CNT | Pixel per scan line.<br>0: 858 pixels (default)<br>1: 864 pixels |
| [4] | R/W | LINE_CNT | Scan lines per frame.<br>0 = 525 (default)<br>1 = 625 |
| [3:1] | R/W | TV_MODE | Video standard.<br>000 = NTSC (default)<br>001 = PAL (I,B,G,H,D,N)<br>010 = PAL (M)<br>011 = PAL (CN)<br>100 = SECAM |
| [0] | R/W | INPUT_MODE | Video format.<br>0 = composite (default)<br>1 = S-Video (separated Y/C) |

### 3.12.2 Bandwidth Control Register

Address Offset: 01h Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | LUMA_FILTER | Luma notch filter bandwidth<br>00 = none (default)<br>01 = narrow<br>10 = medium<br>11 = wide |
| [3:2] | R/W | CHROMA_FILTER | Chroma low pass filter bandwidth<br>0 = narrow (default)<br>1 = wide<br>2 = extra wide<br>3 = extra wide |
| [1] | R/W | BURST_NUMBER | Burst gate width<br>0 = 5 subcarrier clock cycles (default)<br>1 = 10 subcarrier clock cycles |
| [0] | R/W | PED_ENABLE | Blank-to-black pedestal enable<br>0 = no pedestal subtraction<br>1 = pedestal subtraction (default) |

### 3.12.3 Comb Filtering Mode Register

Address Offset: 03h Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:3] | RO | Reserved | |
| [2:0] | R/W | COMB_MODE | 000 = fully adaptive comb (2-D adaptive comb) (default)<br>010 = 5-tap adaptive comb filter (PAL mode only)<br>011 = must be used for S-Video<br>110 = 5-tap hybrid adaptive comb filter (PAL mode only)<br>others = reserved. |

### 3.12.4 Luma AGC Target Value Register

Address Offset: 04h Access: Read/Write
Default Value: DDh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | AGC_LEVEL | Luma AGC target value.<br>Standard / Programming Value<br>NTSC M: DDh (221d) (default)<br>NTSC J: CDh (205d)<br>PAL B,D,G,H,I, COMB N, SECAM: DCh (220d)<br>PAL M,N: DDh (221d) |

### 3.12.5 Y/C Output Control Register

Address Offset: 07h Access: Read/Write
Default Value: 20h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | BLUE_SCREEN | This bit controls the blue screen mode.<br>00 = Disabled<br>01 = Enabled<br>10 = Auto (Default)<br>11 = reserved |
| [3:0] | R/W | YC_DELAY | The range is [-5,7]. Default = 0. |

### 3.12.6 Luma Contrast Register

Address Offset: 08h Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | CONTRAST | *Luma_out* = *Luma_in* * CONTRAST<br>where CONTRAST is a 1.7-bit fixed point value. |

### 3.12.7 Luma Brightness Register

Address Offset: 09h Access: Read/Write
Default Value: 20h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | BRIGHTNESS | *Luma_out* = *Luma_in* + BRIGHTNESS - 32 |

### 3.12.8 Chroma Saturation Register

Address Offset: 0Ah Access: Read/Write
Default Value: 80h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | SATURATION | *Chroma_out* = *Chroma_in* * SATURATION<br>where SATURATION is a 1.7-bit fixed point value |

### 3.12.9 Chroma Hue Phase Register

Address Offset: 0Bh Access: Read/Write
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | HUE | *U_out = U_in*cos(*HUE*/256*360) + V_in * sin(*HUE*/256*360)*<br>*V_out = V_in*cos(*HUE*/256*360) - U_in * sin(*HUE*/256*360)* |

### 3.12.10 Chroma AGC Register

Address Offset: 0Ch Access: Read/Write
Default Value: 8ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | CHROMA_AGC | Chroma AGC target. Default = 138. |

### 3.12.11 AGC Peak Nominal Register

Address Offset: 10h Access: Read/Write
Default Value: 0ah Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6:0] | R/W | AGC_PEAK | Luma peak value. Default = 10. |

### 3.12.12 Chroma DTO Incremental 0 Register

Address Offset: 18h Access: Read/Write
Default Value: 21h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | R/W | CHROMA_FREQ_FIX | Fix chroma frequency.<br>0: disable (default).<br>1: enable. |
| [6] | RO | Reserved | |
| [5:0] | R/W | C_FREQ[29:24] | Bits 29:24 of the 30-bit-wide chroma frequency increment. |

### 3.12.13 Chroma DTO Incremental 1 Register

Address Offset: 19h Access: Read/Write
Default Value: F0h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | C_FREQ[23:16] | Bits 23:16 of the 30-bit-wide chroma frequency increment. |

### 3.12.14 Chroma DTO Incremental 2 Register

Address Offset: 1Ah Access: Read/Write
Default Value: 7Ch Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | C_FREQ[15:8] | Bits 15:8 of the 30-bit-wide chroma frequency increment. |

### 3.12.15 Chroma DTO Incremental 3 Register

Address Offset: 1Bh Access: Read/Write
Default Value: 0Fh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | C_FREQ[7:0] | Bits 7:0 of the 30-bit-wide chroma frequency increment. |

### 3.12.16 Active Video Horizontal Start Time Register

Address Offset: 2Eh Access: Read/Write
Default Value: 82h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | H_START | Active video horizontal start position. Default = 130. |

### 3.12.17 Active Video Horizontal Width Register

Address Offset: 2Fh Access: Read/Write
Default Value: 50h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | H_WIDTH | Active video horizontal pixel counts.<br>Default = 80 → 640+80 = 720 |

### 3.12.18 Active Video Vertical Start Register

Address Offset: 30h Access: Read/Write
Default Value: 22h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | V_START | Active video vertical line start position. Default = 34. |

### 3.12.19 Active Video Vertical Height Register

Address Offset: 31h Access: Read/Write
Default Value: 61h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:0] | R/W | V_WIDTH | Active video vertical line counts.<br>Default = 97 ( 384+97 = 481 half lines |

### 3.12.20 Comb Video Status Register 1

Address Offset: 3Ah Access: Read only
Default Value: 00h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:5] | RO | mv_colourstripes | Macrovision color stripes detected. The number indicates the number of color stripe lines in each group |
| [4] | RO | mv_vbi_detected | MacroVision VBI pseudo-sync pulses detection<br>1 = Detected<br>0 = Undetected |
| [3] | RO | chromalock | Chroma PLL locked to color burst<br>1 = Locked<br>0 = Unlocked |
| [2] | RO | vlock | Vertical lock<br>1 = Locked<br>0 = Unlocked |
| [1] | RO | hlock | Horizontal line locked<br>1 = Locked<br>0 = Unlocked |
| [0] | RO | no_signal | No signal detection<br>1 = No Signal Detected<br>0 = Signal Detected |

### 3.12.21 Soft Reset Register

Address Offset: 3Fh Access: Read/Write
Default Value: 01h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:1] | RO | Reserved | |
| [0] | R/W | RESET | Soft Reset: Write 1 to reset initial values for comb filter |

### 3.12.22 Luminance Peaking Control Register

Address Offset: 80h Access: Read/Write
Default Value: 04h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:6] | RO | Reserved | |
| [5:4] | R/W | Reserved | |
| [3:1] | R/W | PEAK_GAIN | peak_gain. Default = 2. |
| [0] | R/W | PEAK_EN | Luma horizontal peaking control enable.<br>0 = Disabled (default)<br>1 = Enabled |

### 3.12.23 Comb Filter Configuration Register

Address Offset: 82h Access: Read/Write
Default Value: 42h Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7] | RO | Reserved | |
| [6] | R/W | PAL_ERR | PAL error reduced.<br>0: disable.<br>1: enable. |
| [5] | R/W | PAL_AUTO_EN | PAL error detect enable<br>0: disable.<br>1: enable. |
| [4] | R/W | COMB_PAL | PAL comb filter enable.<br>0: disable.<br>1: enable. |
| [3:2] | RO | Reserved | |
| [1:0] | R/W | PAL_SW_LEVEL | PAL switch level.<br>Default = 2. |

### 3.12.24 Comb Lock Configuration Register

Address Offset: 83h Access: Read/Write
Default Value: 6Fh Size: 8 bits

| Bit | Access | Symbol | Description |
|---|---|---|---|
| [7:4] | R/W | lose_chromalock_count | This register is used to tune the chromakill, higher values are more sensitive to losing lock<br>Default = 6. |
| [3:1] | R/W | lose_chromalock_level | Set the level for chromakill.<br>Default = 7. |
| [0] | R/W | lose_chromalock_ckill | When set, chroma is killed whenever chromlock is lost.<br>Default = 1. |

# 4 Electrical Characteristics

## 4.1 Digital I/O Pad Operation Condition

**Table 4-1 Operation Condition**

| | Parameter | Min | Typ | Max |
|---|---|---|---|---|
| VDD18 | Digital Core Power Supply | 1.62V | 1.8V | 1.98V |
| VD33 | Digital I/O Power Supply | 3.0V | 3.3V | 3.6V |
| $V_{IL}$ | Input Low Voltage | -0.3V | | 0.8V |
| $V_{IH}$ | Input High Voltage | 2.0V | | 5.0V |
| $V_{T+}$ | Schmitt Trigger Low-to-High Threshold | 1.44V | 1.58V | 1.71V |
| $V_{T+}$ | Schmitt Trigger High-to-Low Threshold | 1.09V | 1.19V | 1.31V |
| $I_I$ | Input Leakage Current@ $V_I$=3.3V or 0V | | | ±1μA |
| $I_{OZ}$ | Tri-state Output Leakage Current@ $V_O$=3.3V or 0V | | | ±1μA |
| $I_{OL}$ | Low level Output Current@ $V_{OL}$=0.4V | | | |
| | 2mA | 2.1mA | 3.4mA | 4.2mA |
| | 4mA | 4.2mA | 6.9mA | 8.6mA |
| | 8mA | 8.4mA | 13.9mA | 17.2mA |
| | 12mA | 12.5mA | 20.8mA | 25.8mA |
| $I_{OH}$ | High level Output Current@ $V_{OH}$=2.4V | | | |
| | 2mA | 3.0mA | 6.2mA | 10.0mA |
| | 4mA | 5.7mA | 11.6mA | 18.6mA |
| | 8mA | 9.5mA | 19.4mA | 30.9mA |
| | 12mA | 13.3mA | 27.1mA | 43.3mA |
| $R_{PU}$ | Pull-up resistor | 74KΩ | 104KΩ | 177KΩ |
| $R_{PD}$ | Pull-down resistor | 62KΩ | 90KΩ | 176KΩ |

Note: $R_{PU}$ and $R_{PD}$ are always present no matter normal operation or power down mode is enabled. A typical 30~40μA false leakage current is resulted from $R_{PU}$ and $R_{PD}$ when a tester forces I/O to 3.3V or 0.0 V.

## 4.2 DC Characteristics

( VDD25=2.5V; VD33=3.3V; AVDDR=AVDDG=AVDDB=AVDDP=AVDDAC=3.3V; VREF=1.235V; RL=37.5ohm, CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted )

**Table 4-2 DC Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating voltage range | AVDDR AVDDG AVDDB AVDDP AVDDAC VD33 | 3.0 | 3.3 | 3.6 | V | |
| Operating voltage range | VDD18 | 1.62 | 1.8 | 1.98 | V | |
| AVDDR supply current | IAVDDR | -- | 35 | -- | mA | SL=0, SLR=0 |
| AVDDG supply current | IAVDDG | -- | 35 | -- | mA | SL=0, SLG=0 |
| AVDDB supply current | IAVDDB | -- | 35 | -- | mA | SL=0, SLB=0 |
| VD33 supply current | IVD33 | -- | 1 | -- | mA | SL=0 |
| VDD25 supply current | IVDD25 | -- | TBD | -- | mA | |
| Full scale current | IOFS | 2.00 | 34.08 | -- | mA | Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. RSET(ohm)=VREFIN(V)*10.66/IOFS(A) ,where IOFS is full-scale output current. |
| Output voltage range | V(IO) | -- | 1.28 | -- | V | . |
| DAC resolution | -- | -- | 10 | -- | bits | . |
| Integral non-linearity error | INL | -- | 0.5 | +-2 | LSB | . |
| Differential non-linearity error | DNL | -- | 0.5 | +-1 | LSB | . |
| Gain error | -- | -- | -- | TBD | % | . |
| DAC to DAC matching | -- | -- | TBD | TBD | % | . |

## 4.3 AC Characteristics

(VDD25=2.5V; VD33=3.3V; AVDDR=AVDDG=AVDDB=AVDDP=AVDDAC =3.3V; VREF=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

**Table 4-3 AC Characteristics**

| Parameter | Sym | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| CK period | Tck | 5 | -- | -- | Ns | |
| CK to valid output | Tdelay | -- | -- | 0.5*Tck+2 | Ns | |
| Output rise time | Tr | -- | -- | 4 | Ns | 10% to 90% IOFS; assume no package inductance. |
| Output fall time | Tf | -- | -- | 4 | Ns | 90% to 10% IOFS; assume no package inductance. |
| Output settling time | Tsettle | -- | -- | TBD | Ns | assume no package inductance |
| Glitch energy | -- | -- | -- | -- | pvs | assume no package inductance |
| DAC to DAC crosstalk | -- | -- | TBD | -- | Db | . |

## 4.4 Analog Processing and A/D Converters

**Table 4-4 Analog Characteristics**

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Zi | Input impedance, analog video inputs | By design | 500 | | | kΩ |
| Ci | Input capacitance, analog video inputs | By design | | 10 | | pF |
| Vi(pp) | Input voltage range† | Ccoupling = 0.1µF | 0 | | 0.75 | V |
| △G | Gain control range | | 0 | | 12 | dB |
| DNL | DC differential nonlinearity | A/D only | | ±0.5 | | LSB |
| INL | DC integral nonlinearity | A/D only | | ±1 | | LSB |
| Fr | Frequency response | 6 MHz | −0.9 | | −3 | dB |
| SNR | Signal-to-noise ratio | 6 MHz, 1.0 Vp-p | | 50 | | dB |
| NS | Noise spectrum | 50% flat field | | 50 | | dB |
| DP | Differential phase | | 1.5 | | | |
| DG | Differential gain | | | 0.5% | | |

## 4.5 I²C Host Interface Timing

**Table 4-5 I²C Host Interface Timing**

| | Parameter | Min | Typ | Max |
|---|---|---|---|---|
| t1 | Bus free time between a Stop and Start condition | 4.7us | | |
| t2 | Hold time (repeated) Start condition | 4.0us | | |
| t3 | Rise time of both SDA and SCL | | | 1000ns |
| t4 | Data hold time | 5.0us | | |
| t5 | Data setup time | 250ns | | |
| t6 | Fall time of both SDA and SCL | | | 300ns |
| t7 | Setup time for a repeated Start condition | 4.7us | | |
| t8 | Setup time for Stop condition | 4.0us | | |
| tLow | Low period of the SCL | 4.7us | | |
| tHigh | High period of the SCL | 4.0us | | |
| fSCL | SCL clock frequency | | | 1Mhz |
| Cb | Capacitive load for each bus line | | | 400pF |

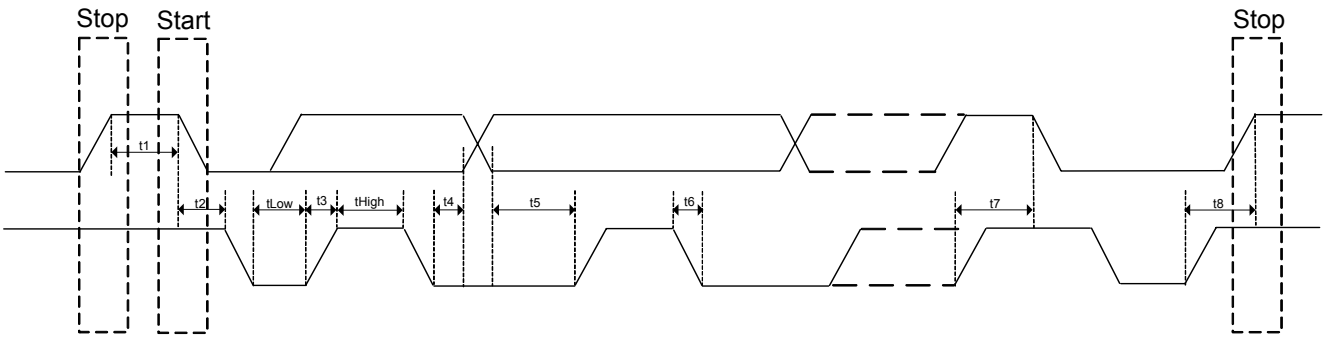
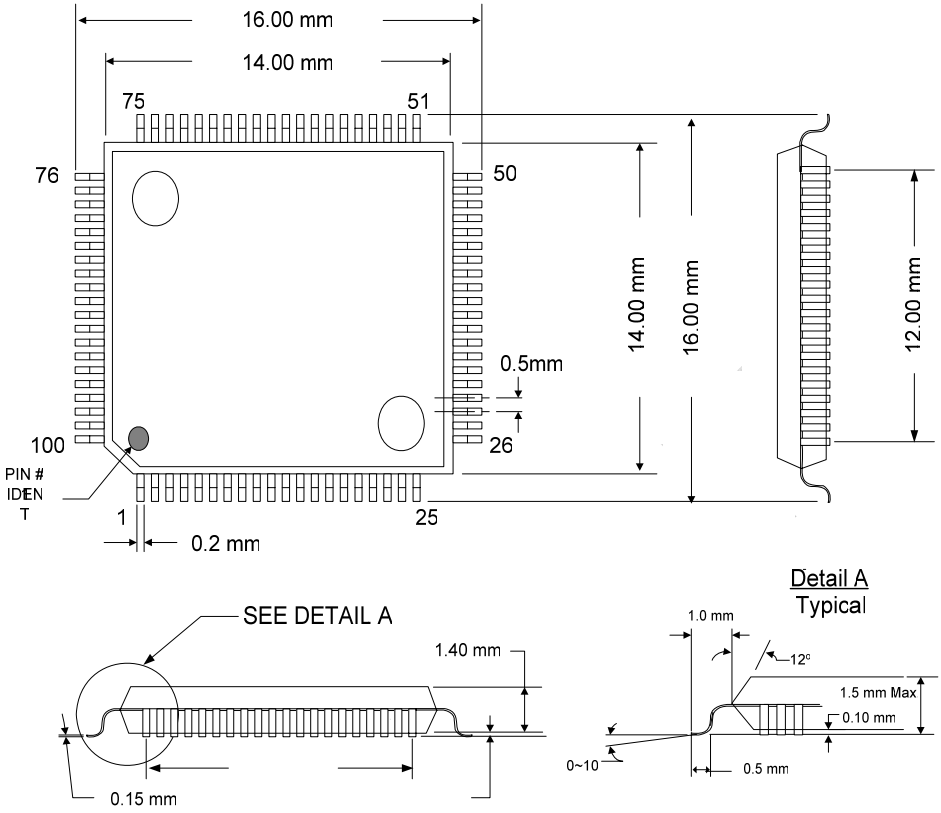



**Figure 4-1 I²C Timing**

# 5 Package Dimensions




[ 100 LQFP 14 X 14 X 1.4 mm ]

# 6 Ordering Information

**Table 6-1 Ordering Information**

| Part No. | Package |
|---|---|
| T108 | 100 LQFP |

# 7 Revisions Note

**Table 7-1 Revision Note**

| Revisions | Description of changes | Date | Note |
|---|---|---|---|
| 0.1 | First draft | May 25, 2005 | |
| 0.2 | Add P0_C1h[6:4] and P0_CBh[7:0] register description | August 3, 2005 | |
| 0.3, 0.4 | Skipped for minor modification of T108 2nd cut | November 15, 2005 | |
| 0.7 | Update TCON registers | October 19, 2006 | |
| 0.8 | Chip Change PinOut | March 22, 2007 | |

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