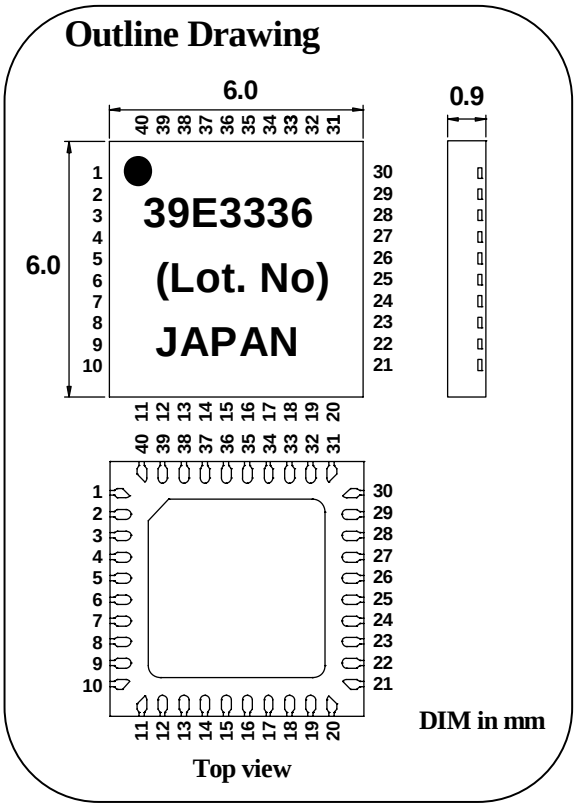
DESCRIPTION

MGFS39E3336 is a 4-stage GaAs RF amplifier Designed for WiMAX CPE.

FEATURES

- InGaP HBT Device
- 6V Operation
- 30dBm Linear Output Power (64QAM, EVM=2.5%)
- 40dB Linear Gain
- Integrated Output Power Detector
- Integrated 1-bit 20dB Step Attenuator
- Surface Mount Package
- RoHS Compliant Package

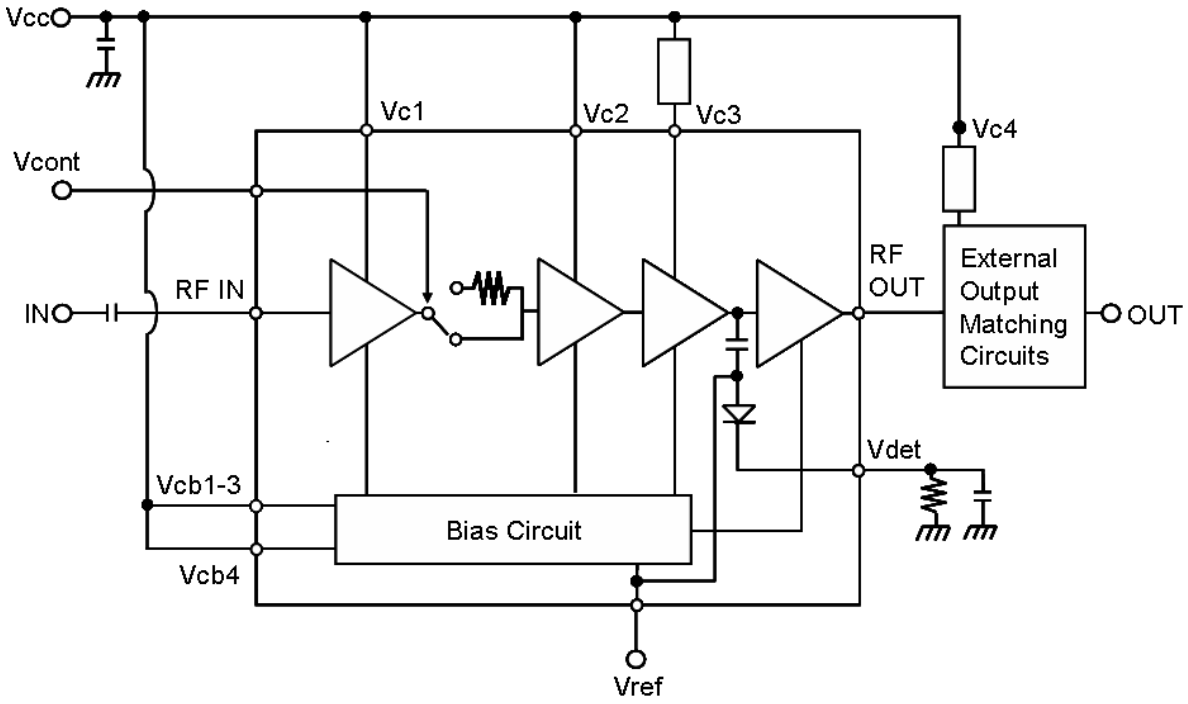
Outline Drawing



APPLICATION

IEEE802.16-2004

FUNCTIONAL BLOCK DIAGRAM



Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i)placement of substitutive, auxiliary, circuits, (ii)use of non-flammable material or (iii)prevention against any malfunction or mishap.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Value	Unit
Vc1,Vc2,Vc3,Vc4 Vcb1-3,Vcb4	Supply Voltage	-	8	V
Vref	Reference Voltage	-	3	V
Vcont	ATT Control Voltage	-	3.5	V
Ic1	Operation current	-	80	mA
Ic2			300	mA
Ic3			300	mA
Ic4			2000	mA
Pin	Input Power	-	-3	dBm
Tj	Junction Temperature		160	deg. C
Tc(op)	Operation Temperature	Pout<=30dBm Duty<=50%	-40 to +85	deg.C
Tstg	Storage Temperature	-	-40 to +125	deg.C

NOTE :
Each maximum rating is guaranteed independently.
Please take care that MGFS39E3336 is operated under these conditions at the worst case on your terminal.
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ELECTRICAL CHARACTERISTICS(Ta=25°C)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
f	Frequency		3.3		3.6	GHz
Gp	Gain	Vcc=6V, Vref=2.85V		43		dB
Ict	Total Collector Current	Pout=30dBm		1.2		A
EVM	EVM	64QAM OFDM Modulation		2.5		%
RLin	Input Return Loss	Duty Cycle <= 50%		10		dB
Vdet	Power Detector Voltage			1.7		V
ATT	Control Gain Step			26		dB

NOTE : Zin=50 Ohm, Zout : Measured with application circuit

ESD RATING : Class 2 (HBM)

MOISTURE SENSITIVITY LEVEL : Level 3

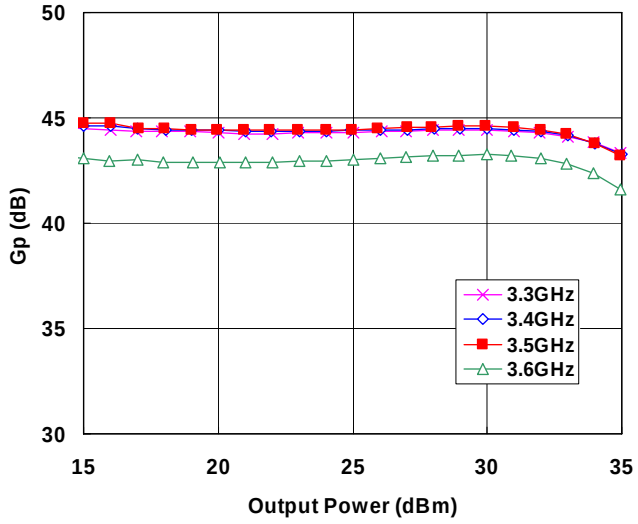
THERMAL RESISTANCE : 4 deg.C/W

(The thermal resistance of the 4th stage is calculated as 5.5 deg.C/W)

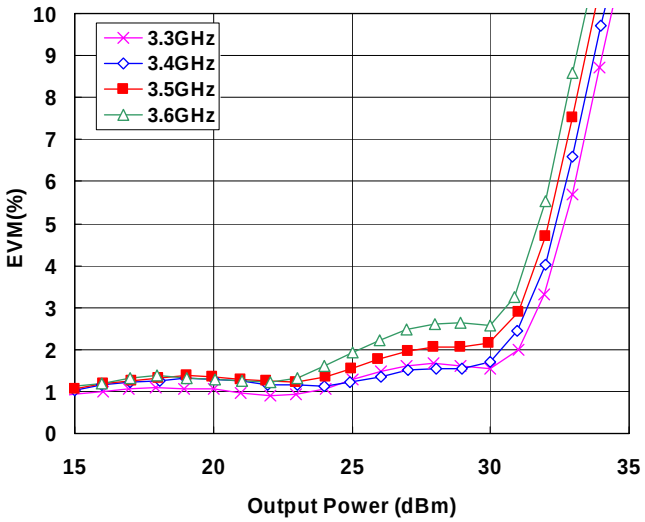
PERFORMANCE DATA

WiMAX OFDM 64QAM BW=10MHz signal input. Vcc=6V, Vref=2.85V, Vcont=0V, Duty 50%, Ta=25deg.C

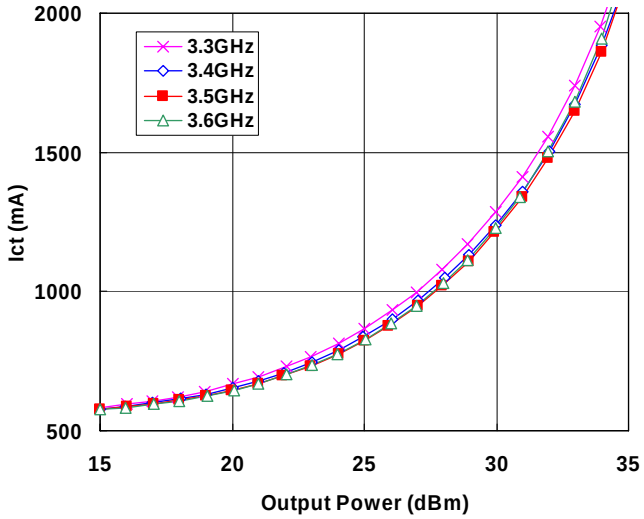
Power Gain vs. Output Power



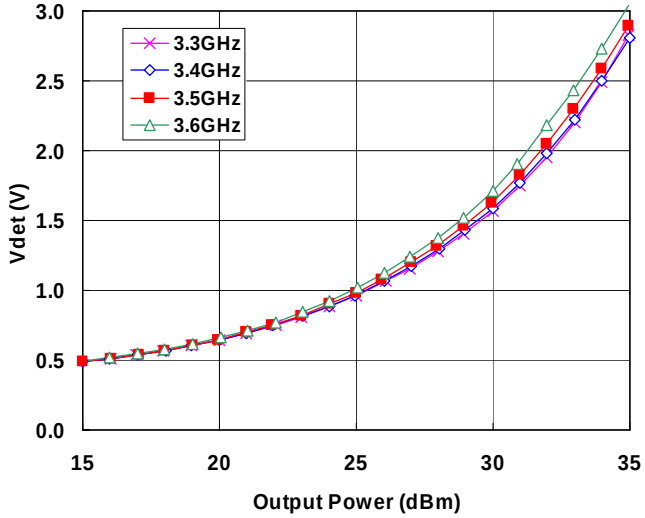
EVM vs. Output Power



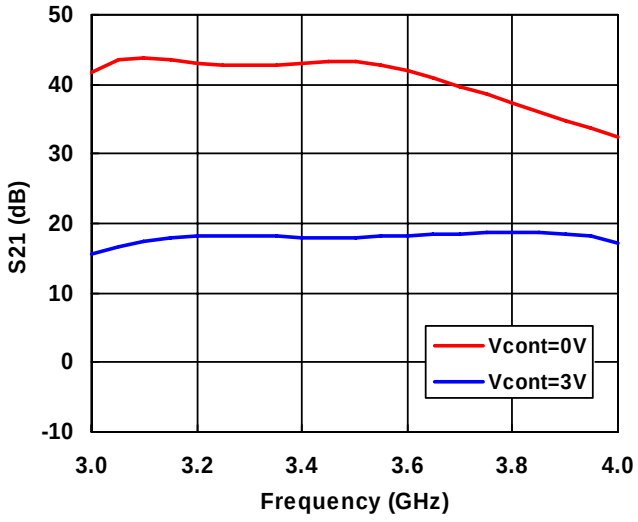
Collector Current vs. Output Power



Detector Voltage vs. Output Power

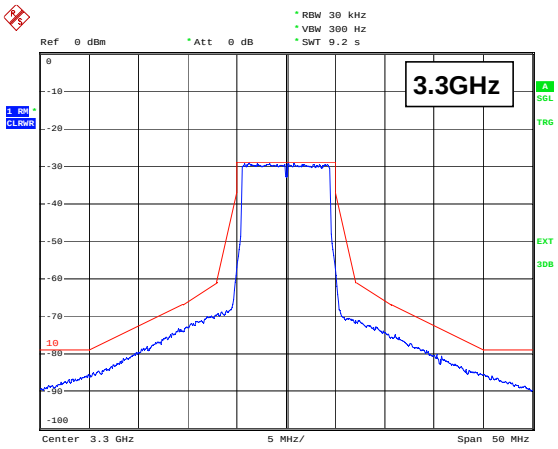


Attenuator Performance



Spectrum Emission Mask

WiMAX OFDM 64QAM BW=10MHz signal input. Vcc=6V, Vref=2.85V, Vcont=0V, Duty=50%, Ta=25deg.C
Po=30dBm, ETSI Mask: EqC-EMO=6 (Type G)



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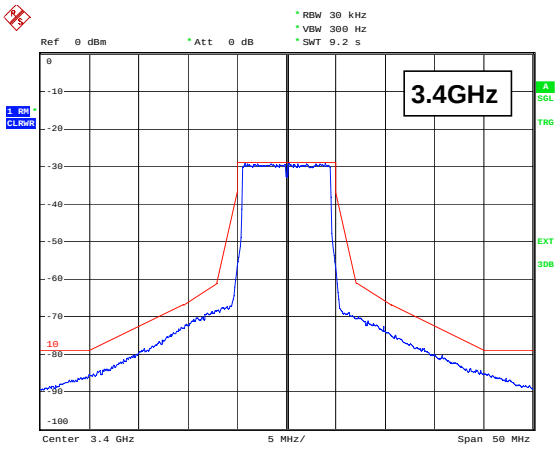

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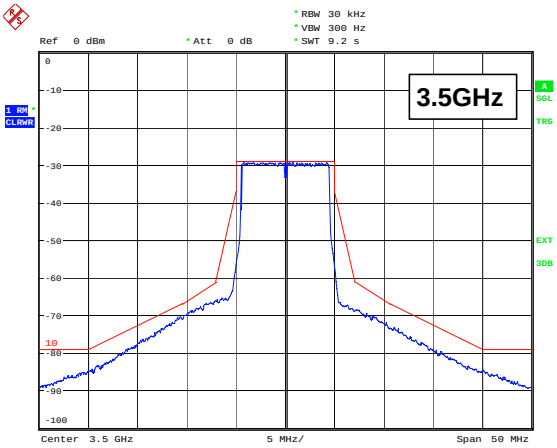

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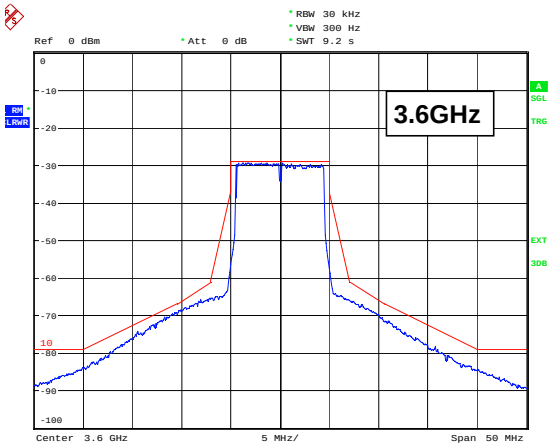

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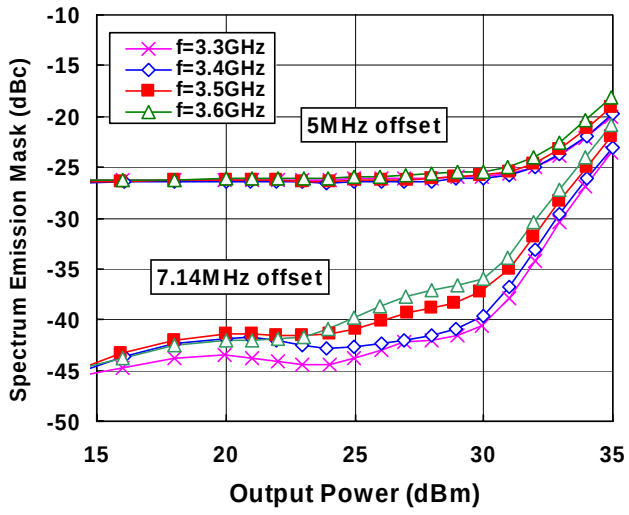
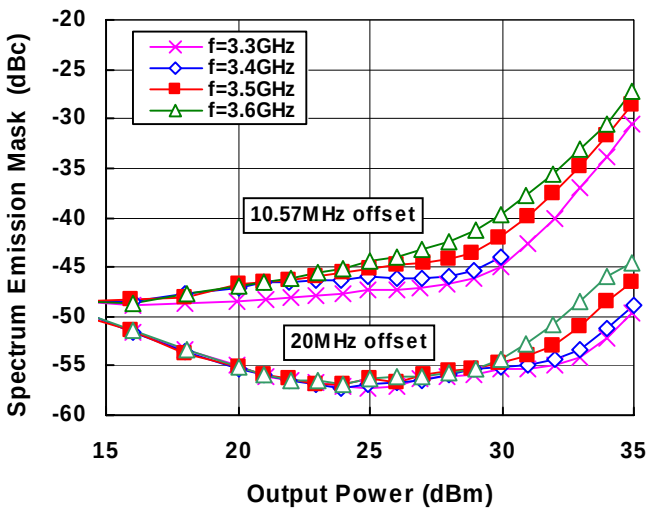
SEM

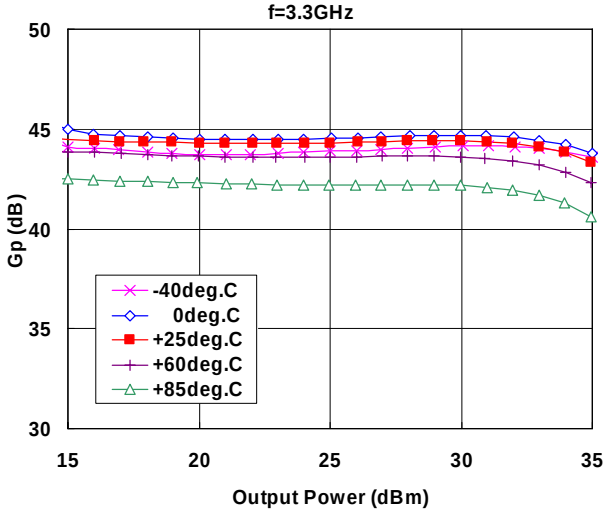


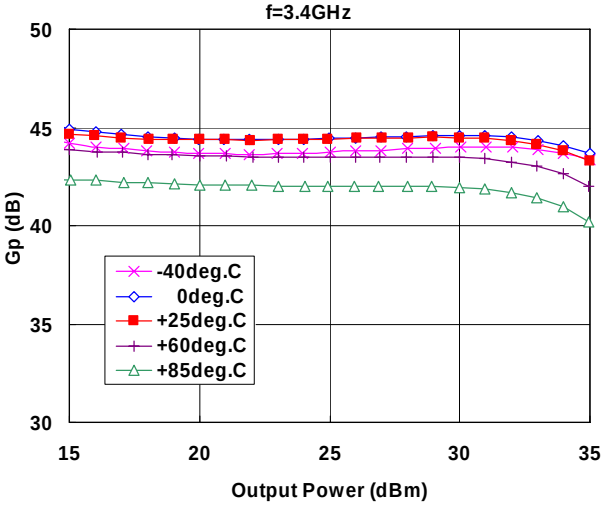


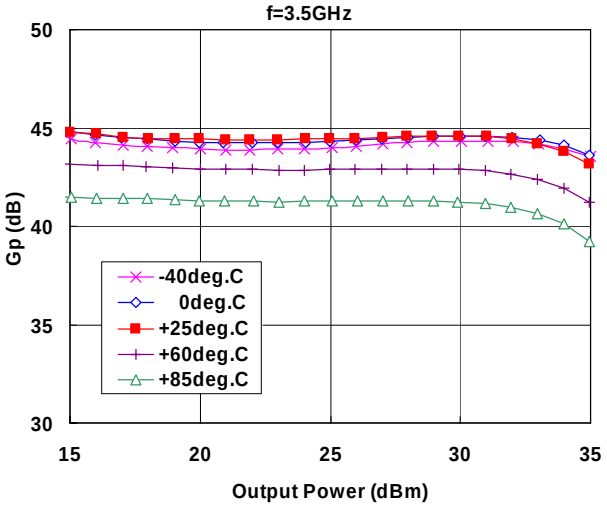
Temperature Dependence

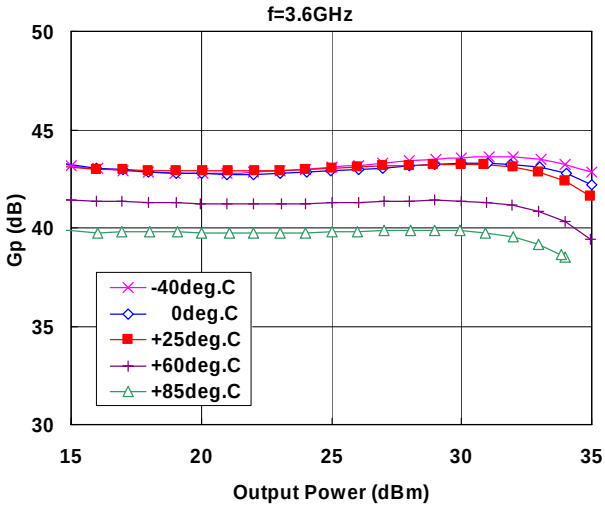
WiMAX OFDM 64QAM BW=10MHz signal input. Vcc=6V, Vref=2.85V, Vcont=0V, Duty 50%, f=3.5GHz

Power Gain vs. Output Power

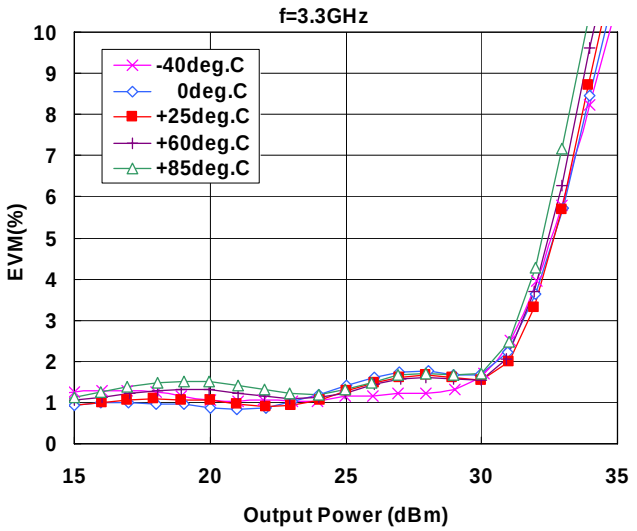


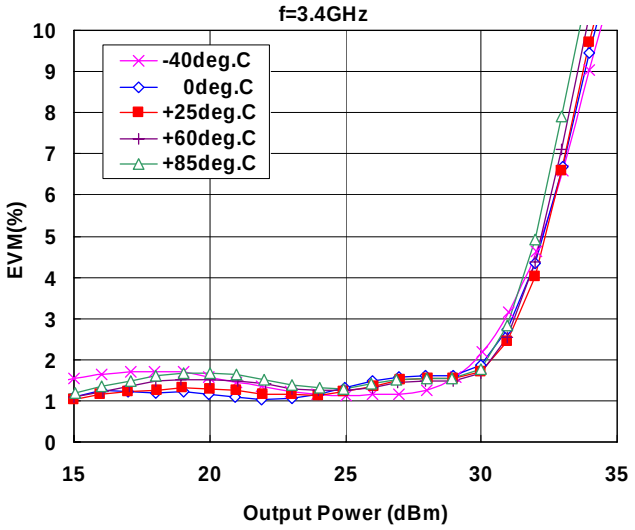


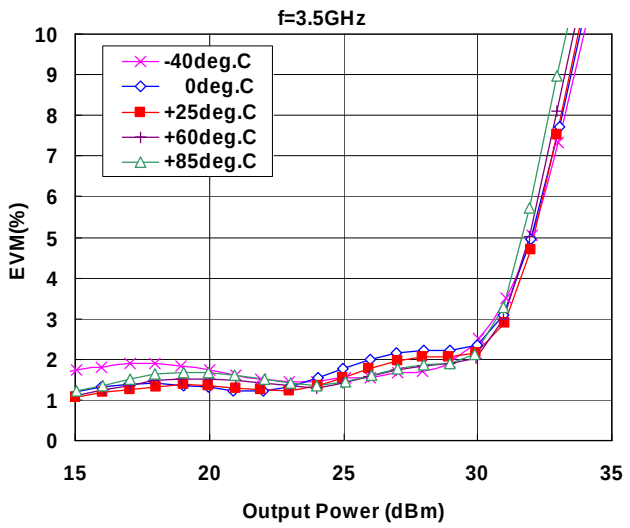


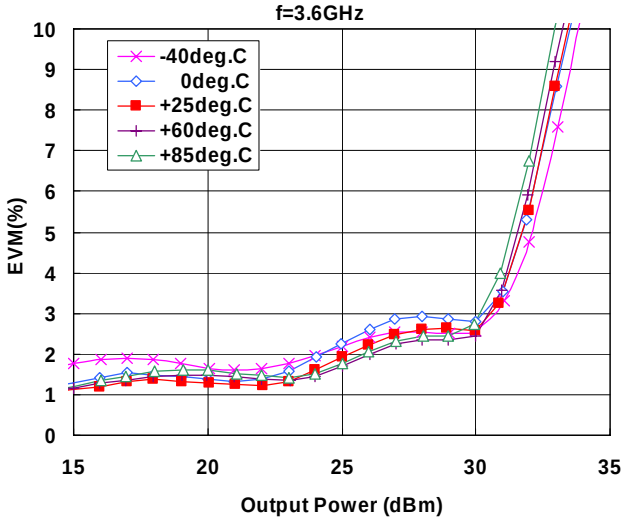


EVM vs. Output Power

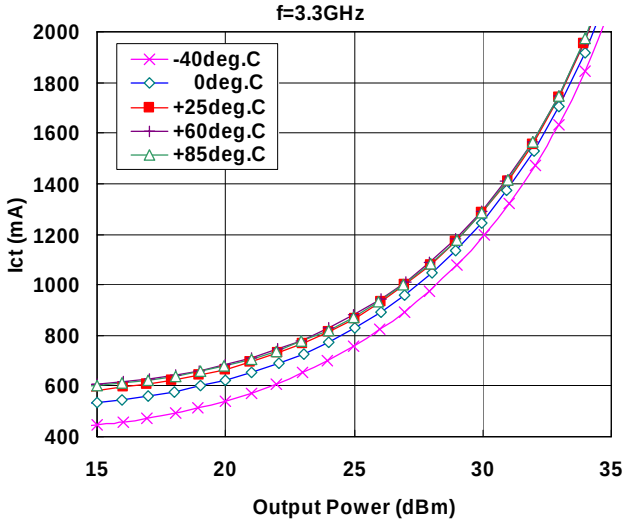


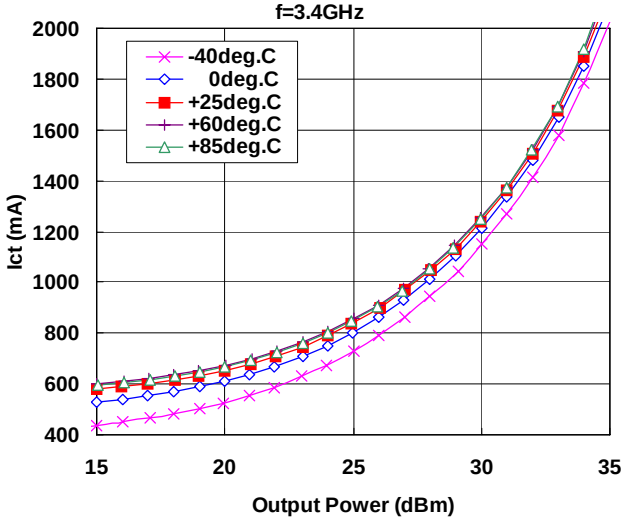


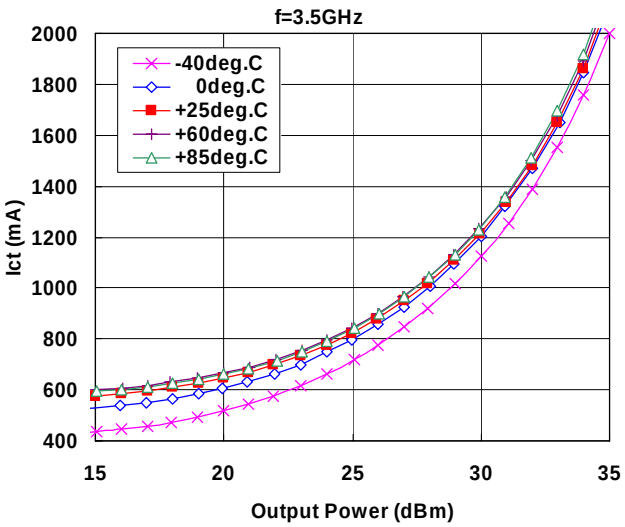


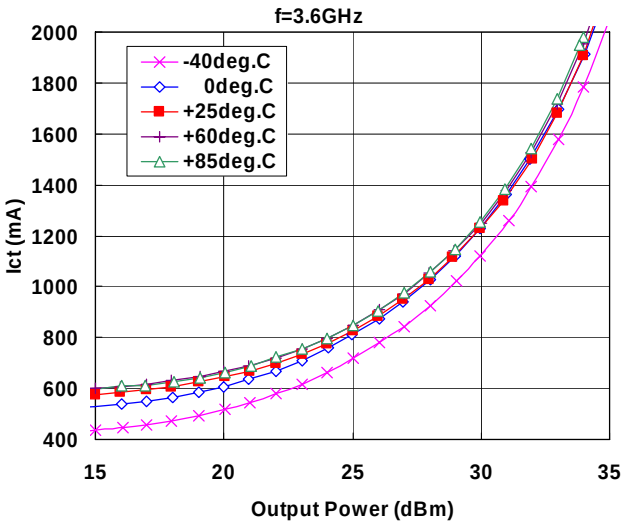


Collector Current vs. Output Power

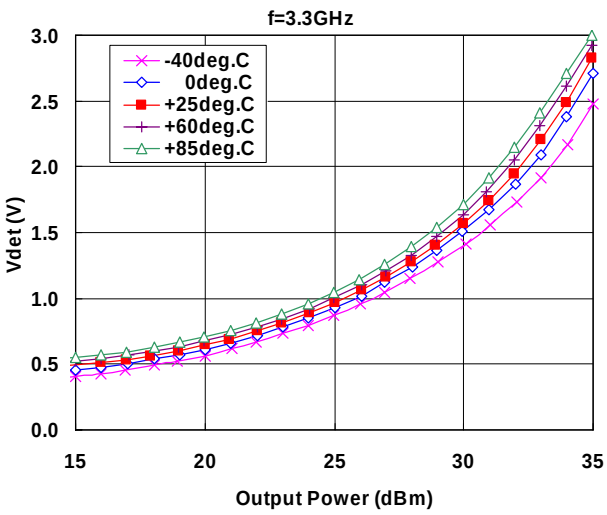


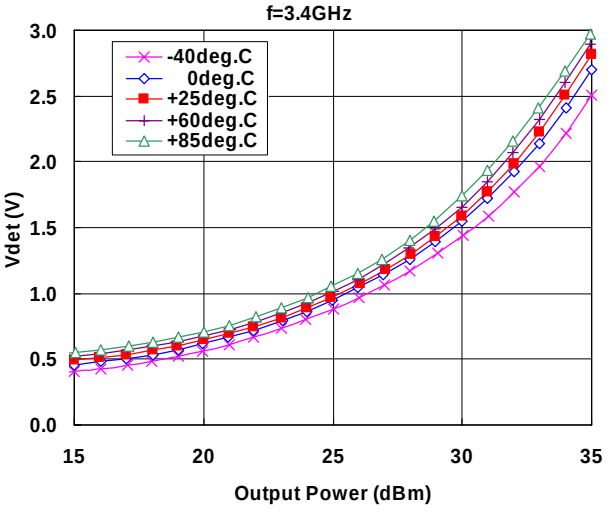


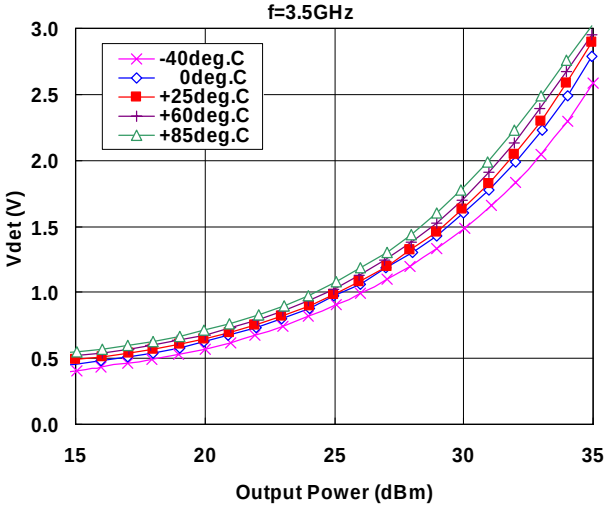


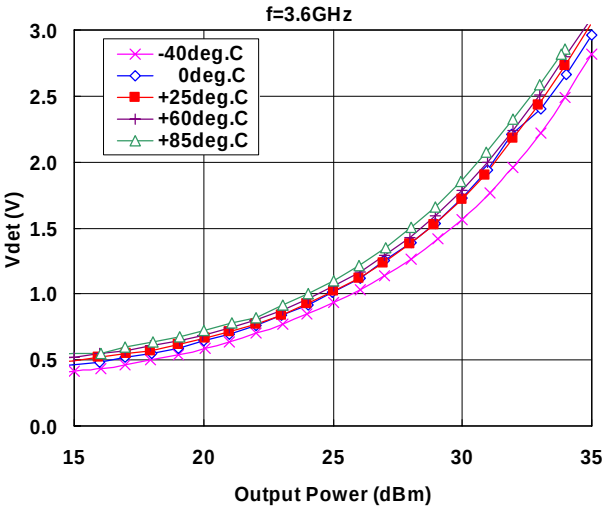


Detector Voltage vs. Output Power

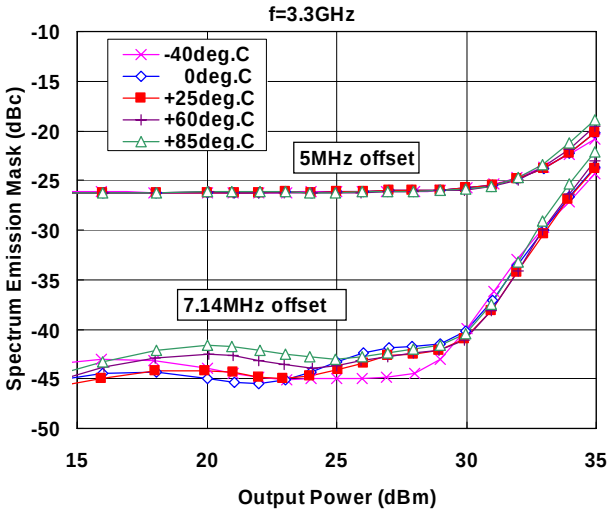


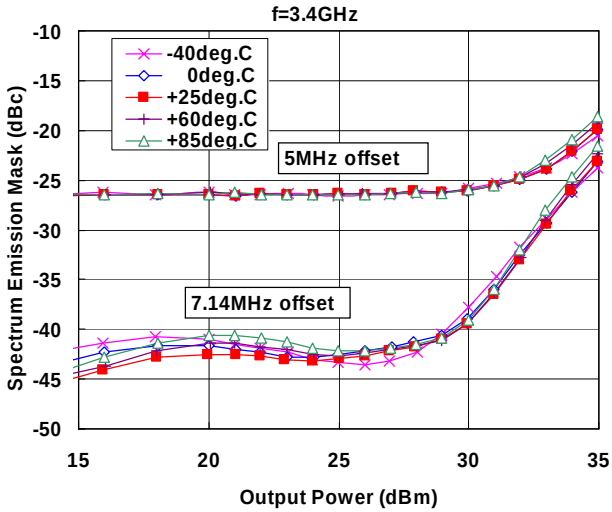


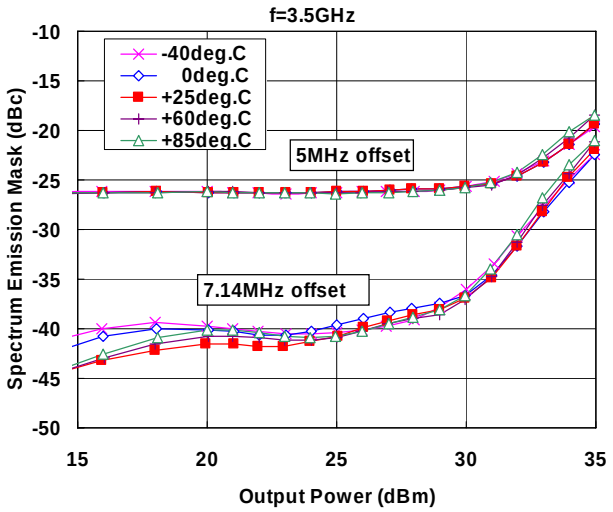


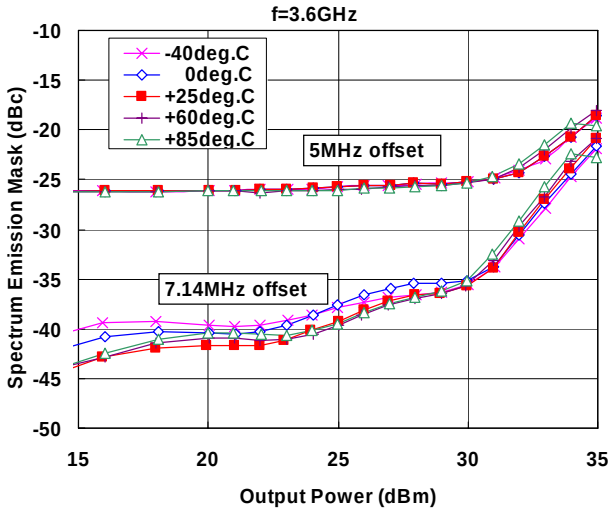


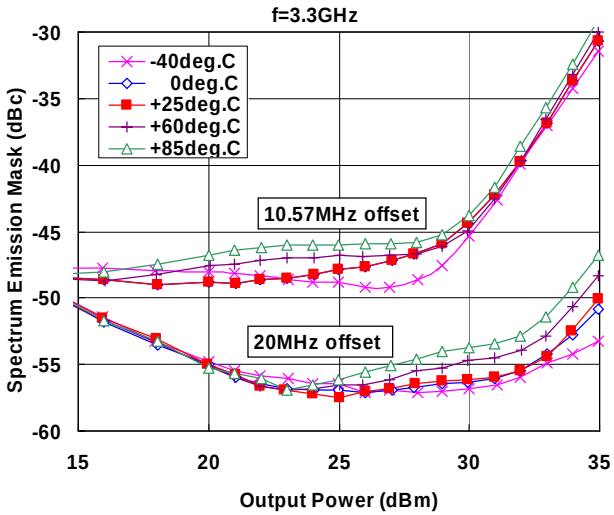
SEI

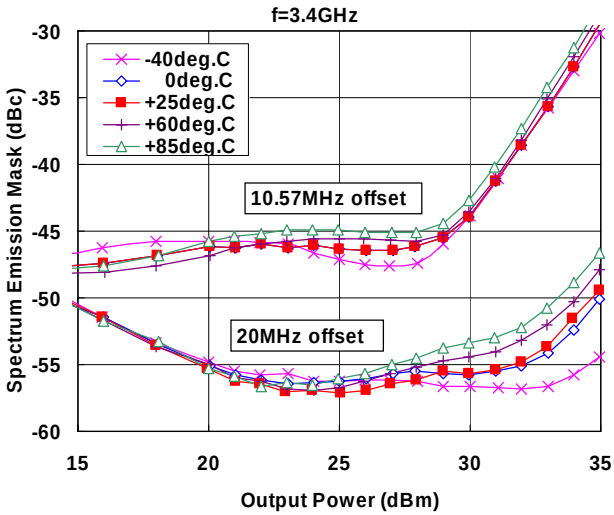


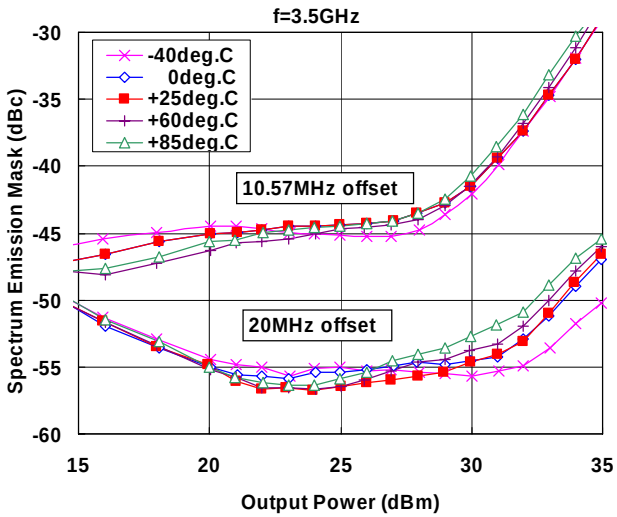


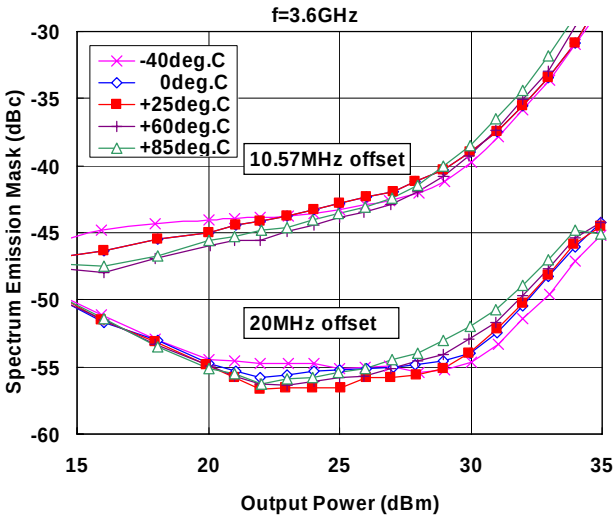

f=3.5GHz
-40deg.C
0deg.C
+25deg.C
+60deg.C
+85deg.C
5MHz offset
7.14MHz offset
Spectrum Emission Mask (dBc)
Output Power (dBm)


f=3.6GHz
-40deg.C
0deg.C
+25deg.C
+60deg.C
+85deg.C
5MHz offset
7.14MHz offset
Spectrum Emission Mask (dBc)
Output Power (dBm)

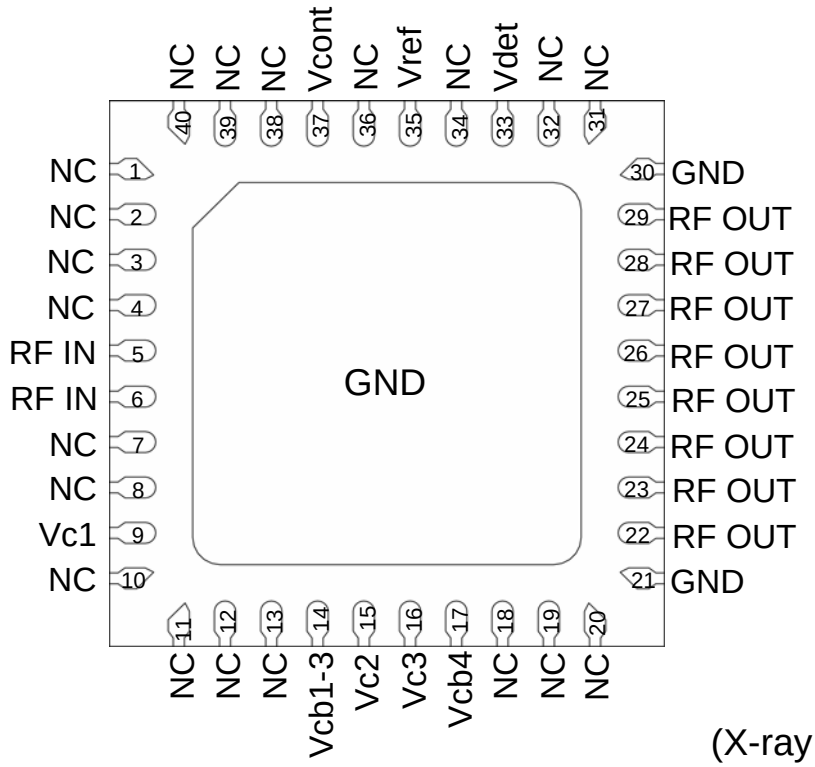

f=3.3GHz
-40deg.C
0deg.C
+25deg.C
+60deg.C
+85deg.C
10.57MHz offset
20MHz offset
Spectrum Emission Mask (dBc)
Output Power (dBm)


f=3.4GHz
-40deg.C
0deg.C
+25deg.C
+60deg.C
+85deg.C
10.57MHz offset
20MHz offset
Spectrum Emission Mask (dBc)
Output Power (dBm)


f=3.5GHz
-40deg.C
0deg.C
+25deg.C
+60deg.C
+85deg.C
10.57MHz offset
20MHz offset
Spectrum Emission Mask (dBc)
Output Power (dBm)


f=3.6GHz
-40deg.C
0deg.C
+25deg.C
+60deg.C
+85deg.C
10.57MHz offset
20MHz offset
Spectrum Emission Mask (dBc)
Output Power (dBm)

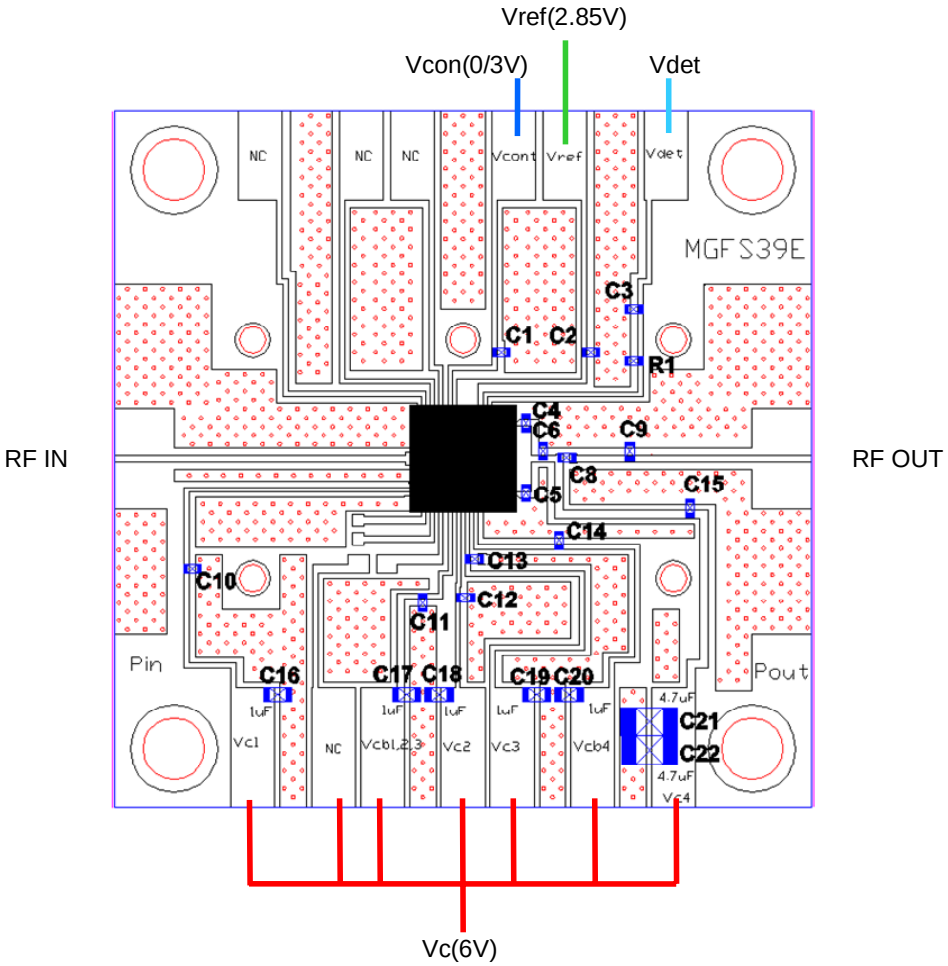
Pinout Description



(X-ray Top View)

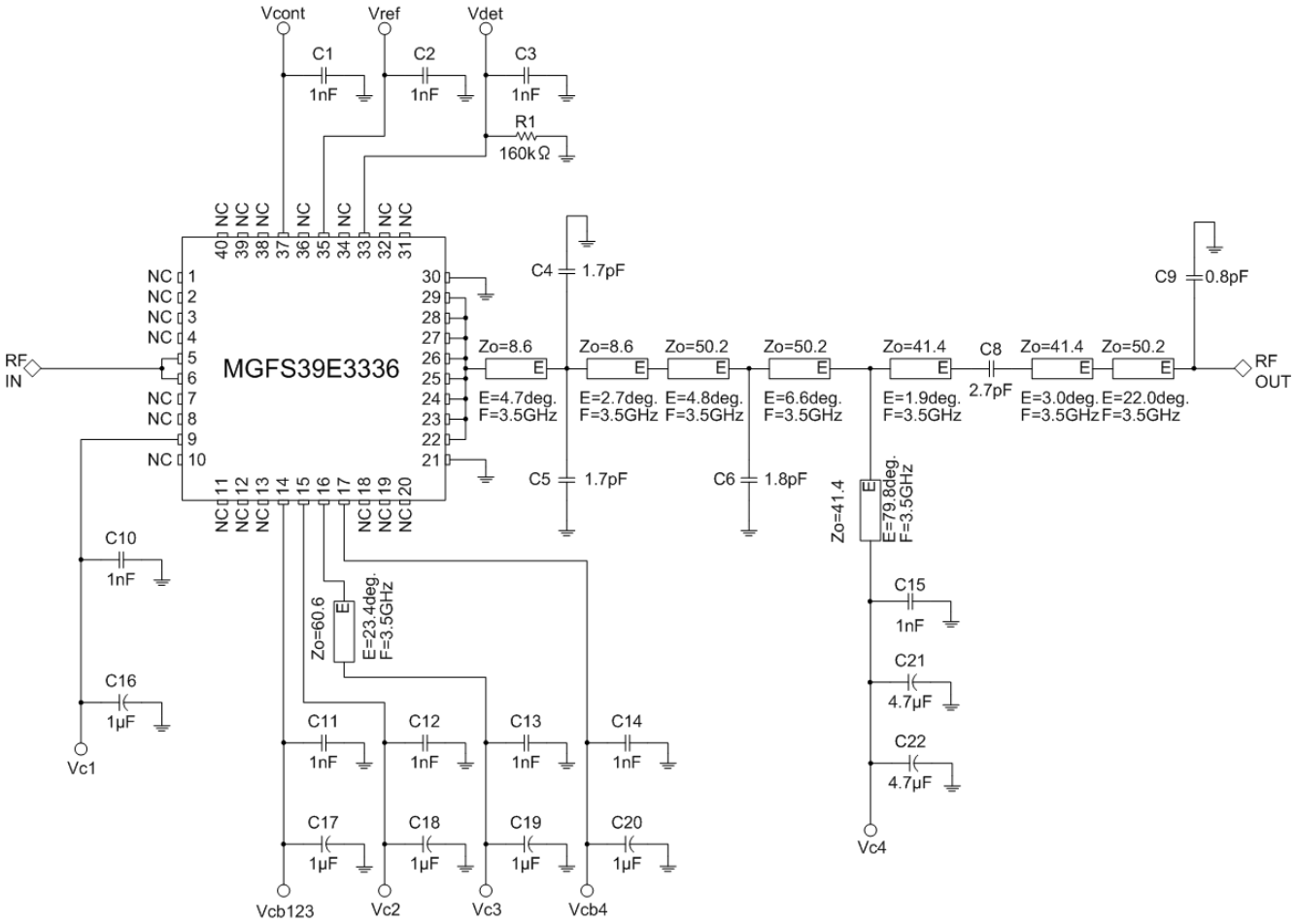
Pin	Function	Description
1, 2, 3, 4, 7, 8, 10, 11, 12, 13, 18, 19, 20, 31, 32, 34, 36, 38, 39, 40	NC	No connect pins, not wired inside the package. It is recommended to connect them to ground.
5,6	RF IN	RF input terminals, internally DC-grounded. Do not apply DC voltage to them
9	Vc1	Collector terminal of the 1st stage.
14	Vcb1-3	DC supply terminal for the 1st, 2nd and 3rd stage bias circuits.
15	Vc2	Collector terminal of the 2nd stage.
16	Vc3	Collector terminal of the 3rd stage.
17	Vcb4	DC supply terminal for the 4th stage base bias circuit.
21,30	GND	Ground pins, internally grounded inside the package. It is recommended to connect them to on-board ground to achieve stable operation.
22,23,24,25, 26,27,28,29	RF OUT	RF output pins and the collector terminals of the 4th stage.
33	Vdet	Output of power detector. A capacitor and a resistor are connected on board between this pin and ground for setting output voltage level appropriately. (See P.10 and 11)
35	Vref	Reference voltage and power up/down control pin for all the stage. The bias circuit operates with a Vref of 2.85V. All bias currents can be shut down by turning off Vref. The Vref pin should be operated under the pulsed condition in order to achieve specified performance. The recommended pulse condition is shown in P. 12.
37	Vcont	Attenuator control pin. The ATT controller offers through mode with a Vcont of 0V, and offers attenuation mode with a Vcont of 3V.
GND	GND	The backside ground paddle should be connected to the external ground plane which provides heat sinking.

EXAMPLE LAYOUT OF EVALUATION BOARD(40mmX 40mm, t=0.2mm(RF), Er=4.2, FR-4)



ITEM	DESCRIPTION	NOTE
Q1	MGFS39E3336	6mmX6mm, QFN
C1, C2, C10, C11, C12 C14	1 nF, 1005 Murata, GRM155B11H102KDA2	Decoupling Capacitors.
C13, C15	1 nF, 1005 Murata, GRM155B11H102KDA2	Decoupling Capacitors. Position is important.
C3	1 nF, 1005 Murata, GRM155B11H102KDA2	Capacitor for detector circuit. Defines response shape.
C4, C5	1.7 pF, 1005 Murata, GJM1554C1H1R7BB01	Capacitors for output matching circuit, Position is important.
C6	1.8 pF, 1005 Murata, GJM1554C1H1R8BB01	Capacitor for output matching circuit. Position is important.
C7	(Unused Number)	-
C8	2.7 pF, 1005 Murata, GJM1553C1H2R7BB01	Capacitor for output matching circuit. Position is important.
C9	0.8 pF, 1005 Murata, GJM1554C1HR80BB01	Capacitor for output matching circuit. Position is important.
C16, C17, C18, C19, C20	1uF, 1608 Murata: GRM188B31E105KA75	Decoupling Capacitors.
C21, C22	4.7uF, 3216 Murata: GCM31CR71E475KA40	Decoupling Capacitors.
R1	160kohms, 1005 Taiyosha, RPCO3T164J	Resistor for detector circuit. Defines output voltage

APPLICATION CIRCUIT IN EVALUATION BOARD



NOTE:

<Layout>

A properly designed PC board is essential to any RF/microwave circuit. Be sure to use controlled impedance lines on all high-frequency inputs and outputs. A ground plane should be present on both the top and bottom of the PC board and plated-through via holes connecting the top and bottom ground planes should be distributed (See page 10). GND pins and ground paddle of the package should be connected to the bottom ground plane with plated-through via holes close to the package. To improve the heat resistance, place as plated-through via holes as possible under the ground paddle (See page. 13).

<Output matching circuit>

The output matching circuit is not included in the device so that users can determine the optimum output performance on their boards at the frequencies of interest. Since the circuit dictates the RF characteristics of PA, especially distortion, it should be designed with great care to obtain its maximum ability.

The schematic of the evaluation board is shown above. Capacitors, C4~C6, C8, C9 and C15, and controlled impedance lines are optimized to realize broad-band output matching at frequencies from 3.3 to 3.6GHz.

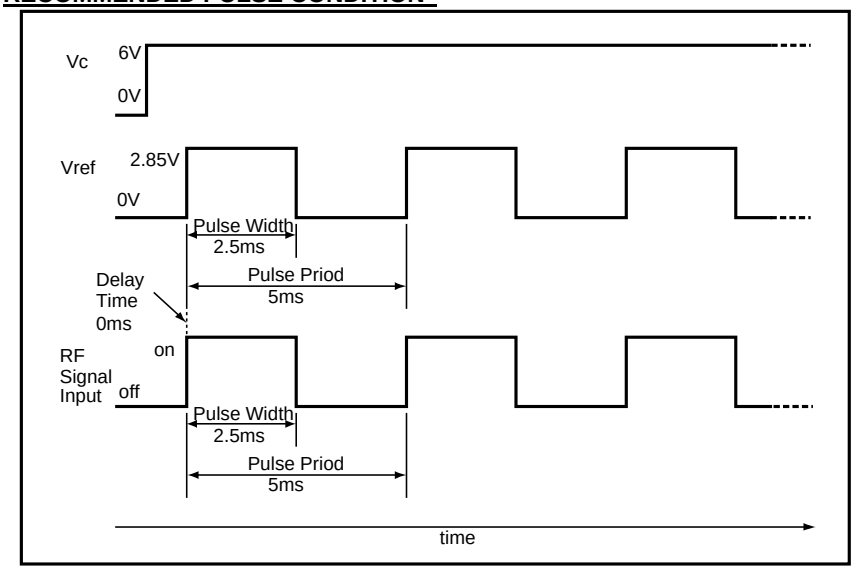
Input and output matching networks are very sensitive to layout-related parasitics. Suggested component values may vary according to layout and PC board material.

<Bias circuit>

Since the high-impedance feed lines for Vc3 and Vc4 are not included in the device, both the lines have to be laid out on the PCB. In layout design, please refer to the reference circuit of the feed lines which affect the distortion.

Each Vc node on the board should have its own decoupling capacitor to minimize supply coupling from one section of the MMIC to another. A bypass capacitor with low ESR at the RF frequency of operation is located close to the package to reject the RF noise. In addition, a large decoupling capacitor is located on each power supply line to reject low frequency noise.

RECOMMENDED PULSE CONDITION

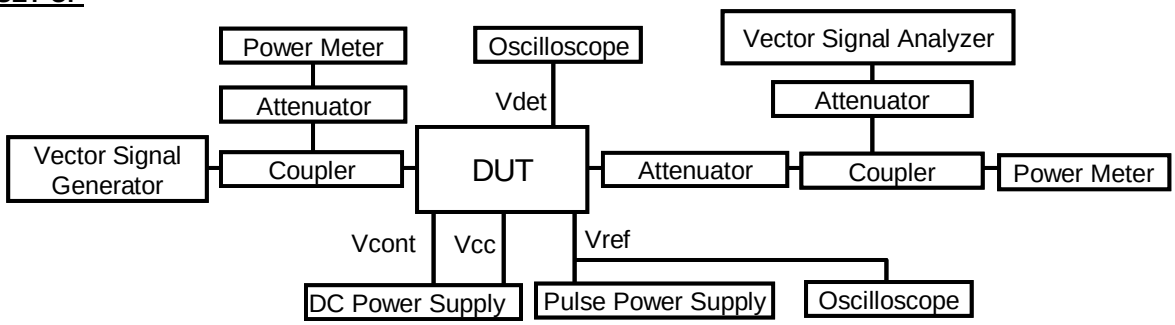


- Pulse Period : 5ms
- Pulse Width : 2.5 ms
- Delay time : 0 ms
- Rise time of Vref pulse : 100ns
- Set up time of quiescent current after Vref turn on : 1 us

- This figure shows the timing chart between Vref and input signal.
- Only while the reference voltage is 2.85V, the device transmits the input signal (*1).
- We usually set the delay time at 0ms in our EVB evaluation because of short set-up time. However set-up time often depends on bypass capacitors of PCB. Therefore, please give appropriate delay time (e.g. about the rise time of Vref) between the rise edge of Vref and that of the input signal .
- We recommended the device operate with less than 50% duty cycle of a 5msec period in order to ensure specified reliability.

*1: In case the device is operated under the Vref conditions of more than 50% duty cycle, self-heating will cause reliability problem, thereby degrading both power gain and EVM performance unexpectedly.

TEST SET-UP



- Calibrate power meters at input/output ports on the EVB.
- Apply DC voltage to Vcc (Vcb1-3, Vcb4, Vc1~Vc4) and Vcont, where pulsed power supply should be applied to Vref for pulsed operation. .
- Monitor DC output voltage from Vdet using an oscilloscope or a multimeter.

<Power up sequence>

GND->Vcc->Vref->Vcont

(1)Apply 6V to Vcc, where stepping up from 0 to 6V is preferable.

(2)Supply pulsed voltage between 0 and 2.85V for Vref.
Please check the voltage level of Vref close to EVB and the timing chart between Vref and input signal using an oscilloscope. Also please do not apply supply voltage exceeding 3V(absolute maximum rating) to the Vref terminal.

(3)Supply Vcont with 3V for the attenuation mode. In the thru-mode, apply 0V to Vcont or keep it open.

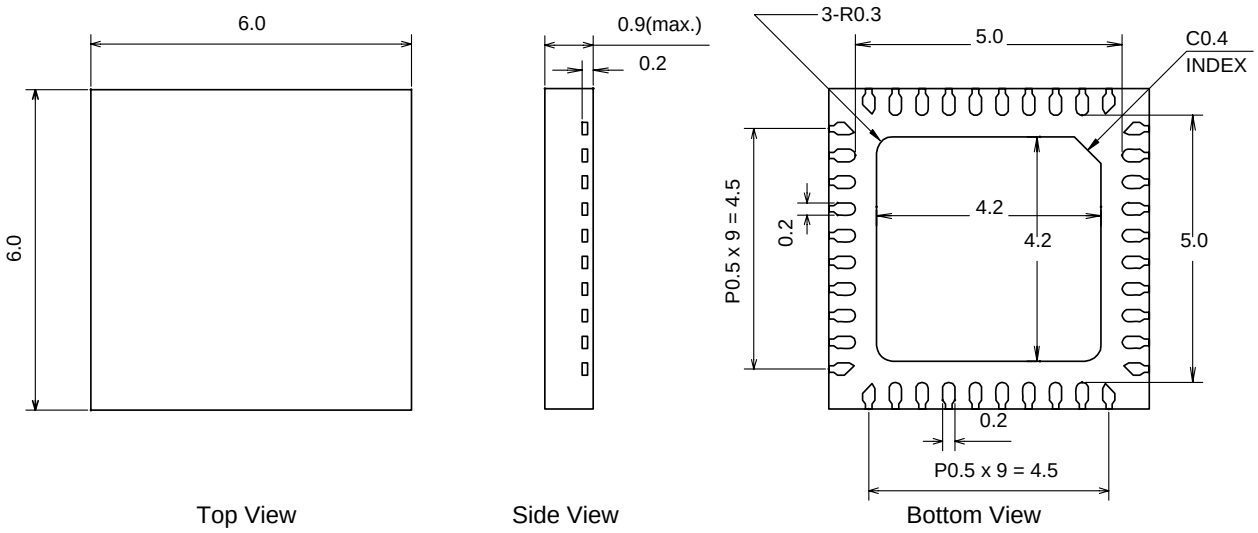
<Power off sequence>

Vcont->Vref->Vcc->GND

The reverse procedure is recommended for bias off.

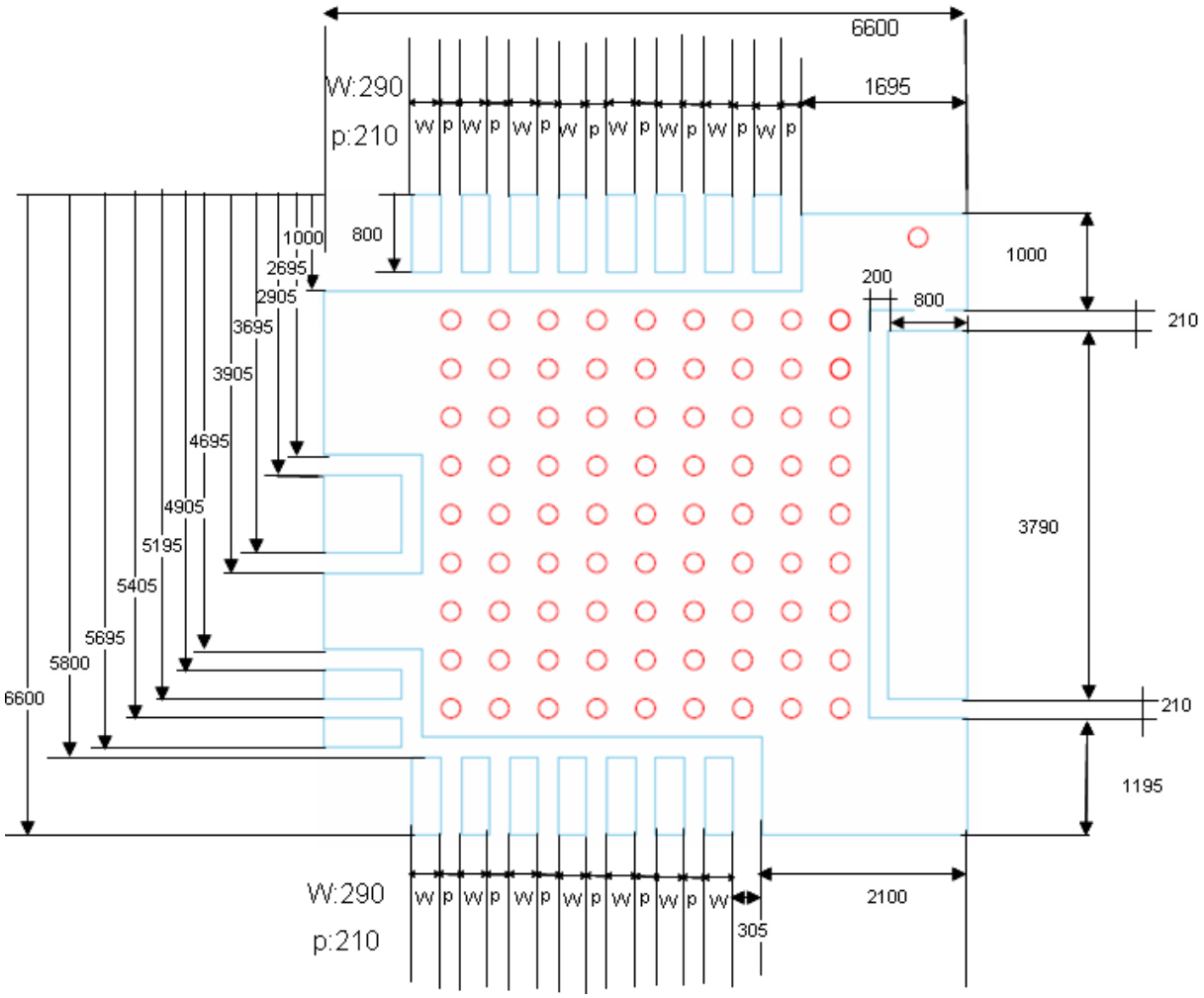
PACKAGE DRAWING DIMENSIONS

All Dimensions are in mm. General tolerance is ±0.1mm.



Top View Side View Bottom View

EXAMPLE METAL LAND PATTERN



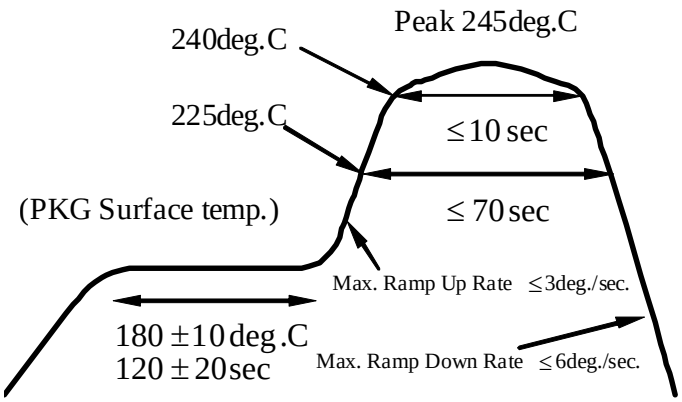
Through holes with 200um diameter should be put with a distance of 500um among them.
It is recommended that they have metallization of 25um thick on the inside wall.

HANDLING PRECAUTION

1) Work desk, test equipment, soldering iron and worker should be grounded before mounting and testing. Please note that electric discharge of GaAs HBT is much more sensitive than that of Si transistor. Handling without ground possibly damages GaAs HBT.

2) The surface of a board on which this product is mounted should be as flat and clean as possible to prevent a substrate from cracking by bending this product.

3) Recommended IR reflow soldering condition is shown as follows. (Max. two times)



4) Handling precaution at high temperature
In case of heating this product, please keep the same heat profile as recommended reflow one.
Please note that crack, flaw or modification may be generated if epoxy resin part is handled with tweezers and etc. at high temperature.

5) Cleaning condition
Please select after confirming administrative guidance, legal restrictions, and the mass of the residual ion contaminant etc., and use it.

6) After soldering, please remove the flux. Please take care that solvent does not penetrate into this product.

7) GaAs HBT contains As(Arsenic). This product should be dumped as particular industrial waste.