# RENESAS

# RNA51958A,B

## Voltage Detecting, System Resetting IC Series

## Description

RNA51958A,B are semiconductor integrated circuits for resetting of all types of logic circuits such as CPUs, and

has the feature of setting the detection voltage by adding external resistance.

They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor.

They fined extensive applications, including battery checking circuit, level detecting circuit and waveform shaping

circuit.

## Features

- Few external parts
- Large delay time with a capacitor of small capacitance (td ≈ 100 ms, at 0.33 μF)
- Wide supply voltage range: 2 V to 17 V
- Wide application range
- Ordering Information

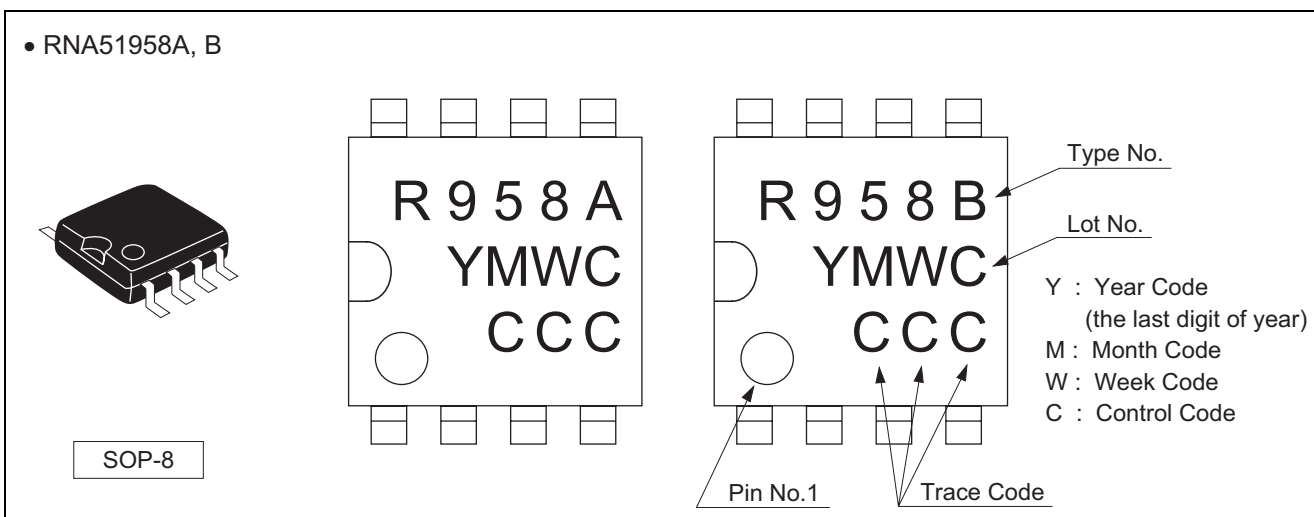| Part Name | Package Type | Package Code | Package Abbreviation | Taping Abbreviation (Quantity) | Surface Treatment |
|---|---|---|---|---|---|
| RNA51958AFPH0 | SOP-8 pin | PRSP0008DE-C | FP | H (2,500 pcs / Reel) | 0 (Ni/Pd/Au) |
| RNA51958BFPH0 | SOP-8 pin | PRSP0008DE-C | FP | H (2,500 pcs / Reel) | 0 (Ni/Pd/Au) |

## Application

- Reset circuit of Pch, Nch, CMOS, microcomputer, CPU and MCU, Reset of logic circuit, Battery check circuit, switching circuit back-up voltage, level detecting circuit, waveform shaping circuit, delay waveform generating circuit, DC/DC converter, over voltage protection circuit
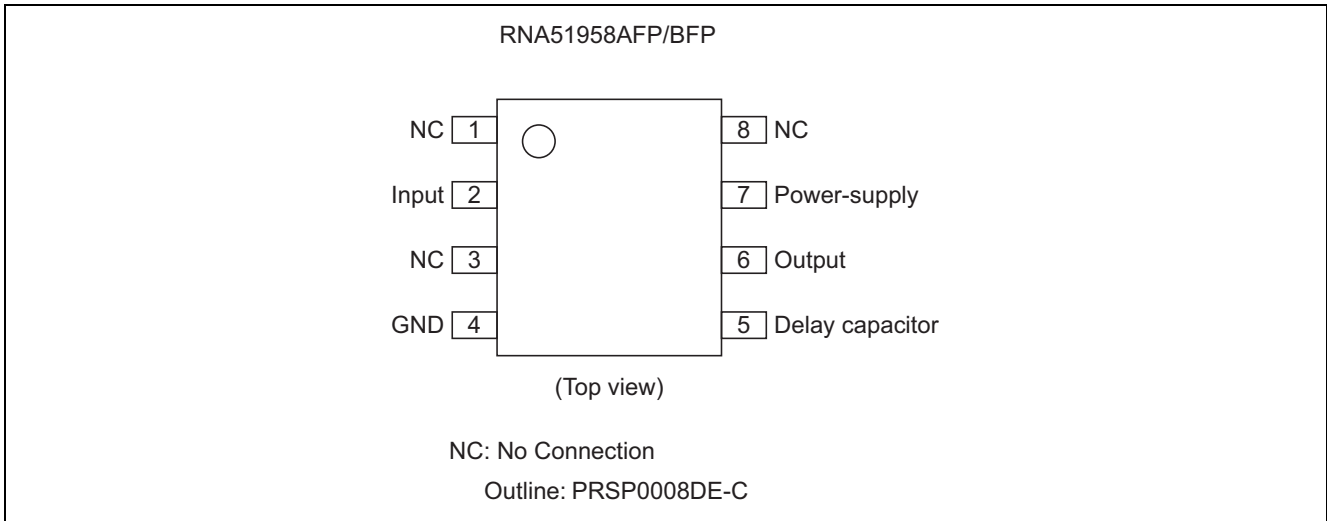
## Recommended Operating Condition
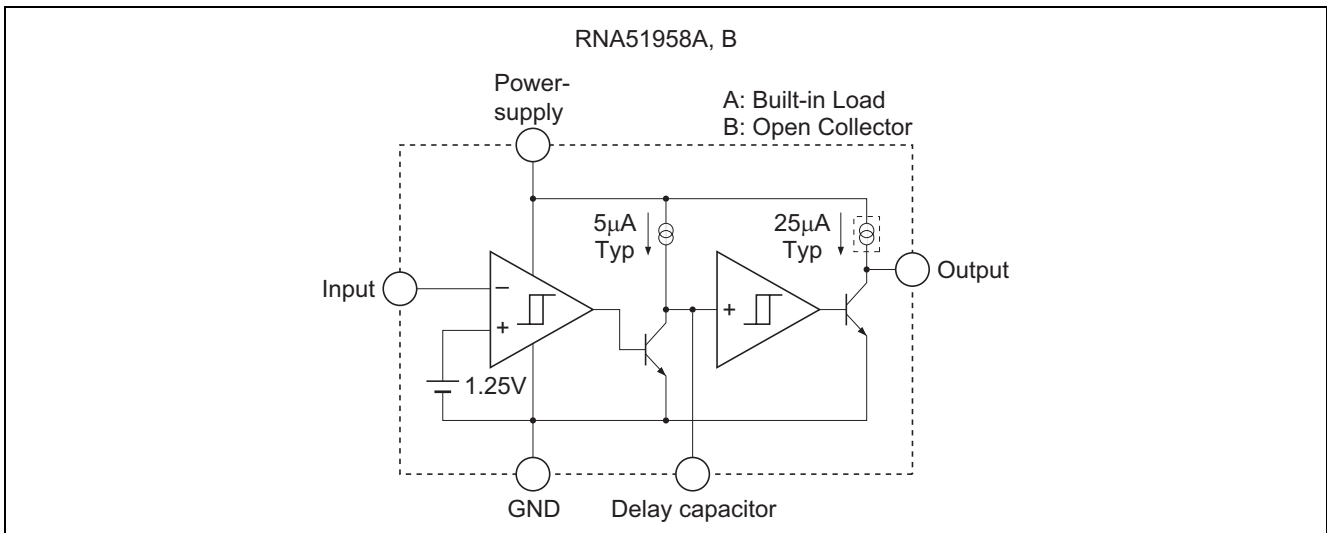
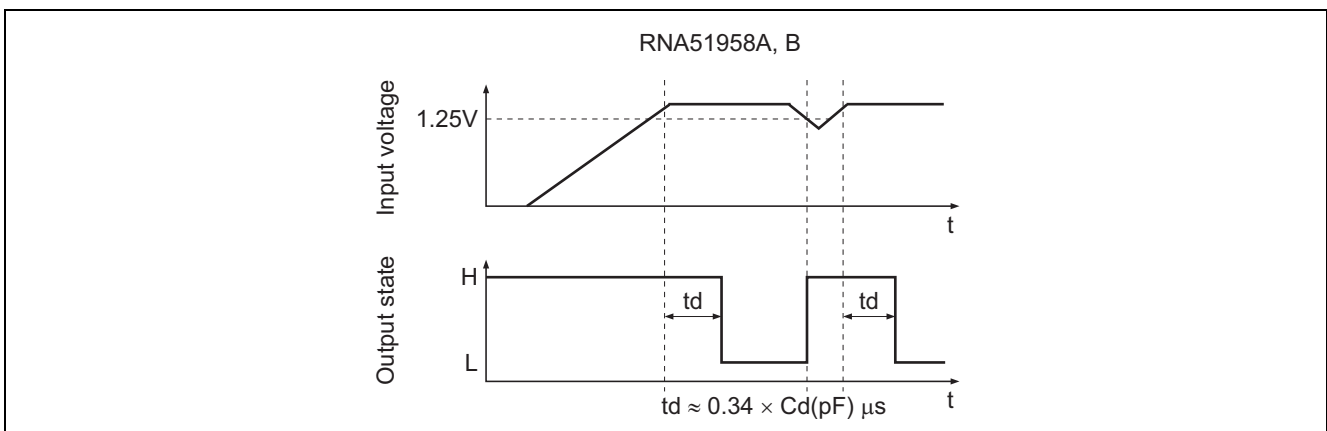- Supply voltage range: 2 V to 17 V

## Outline and Article Indication



- RNA51958A, B

R958A
YMWC
CCC

R958B
YMWC
CCC

SOP-8

Type No.
Lot No.
Y : Year Code
(the last digit of year)
M : Month Code
W : Week Code
C : Control Code

Pin No.1
Trace Code

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## Pin Arrangement

RNA51958AFP/BFP

| | |
|---|---|
| NC $\boxed{1}$ | $\boxed{8}$ NC |
| Input $\boxed{2}$ | $\boxed{7}$ Power-supply |
| NC $\boxed{3}$ | $\boxed{6}$ Output |
| GND $\boxed{4}$ | $\boxed{5}$ Delay capacitor |

(Top view)

NC: No Connection

Outline: PRSP0008DE-C

## Block Diagram

RNA51958A, B

Power-supply

A: Built-in Load
B: Open Collector

5μA Typ

25μA Typ

Input

Output

1.25V

GND    Delay capacitor

## Operating Waveform

RNA51958A, B

Input voltage

1.25V

t

Output state

H

td          td

L

$td \approx 0.34 \times Cd(pF)$ μs

t

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## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

| Item | Symbol | Ratings | Unit | Conditions | |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 18 | V | | |
| Output sink current | Isink | 6 | mA | | |
| Output voltage | $V_O$ | $V_{CC}$ | V | Type A (output with constant current load) | |
| | | 18 | | Type B (open collector output) | |
| Power dissipation | Pd | 400 | mW | 8-pin SOP (PRSP0008DE-C) | |
| Thermal derating | Kθ | 4.4 | mW/°C | Refer to the thermal derating curve. | 8-pin SOP (PRSP0008DE-C) |
| Operating temperature | Topr | −40 to +85 | °C | | |
| Storage temperature | Tstg | −55 to +125 | °C | | |
| Input voltage range | Vin | −0.3 to $V_{CC}$ | V | $V_{CC} \leq 7$ V | |
| | | −0.3 to +7 | | $V_{CC} > 7$ V | |

## Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

- "H" reset type

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detecting voltage | $V_S$ | 1.20 | 1.25 | 1.30 | V | |
| Hysteresis voltage | $\Delta V_S$ | 9 | 15 | 23 | mV | $V_{CC} = 5$V |
| Detecting voltage temperature coefficient | $V_S/\Delta T$ | — | 0.01 | — | %/°C | |
| Supply voltage range | $V_{CC}$ | 2 | — | 17 | V | |
| Input voltage range | Vin | −0.3 | — | $V_{CC}$ | V | $V_{CC} \leq 7$V |
| | | −0.3 | — | 7.0 | | $V_{CC} > 7$V |
| Input current | Iin | — | 100 | 500 | nA | Vin = 1.25V |
| Circuit current | $I_{CC}$ | — | 390 | 590 | μA | Type A, $V_{CC} = 5$V |
| | | — | 360 | 540 | | Type B, $V_{CC} = 5$V |
| Delay time | $t_{pd}$ | 1.6 | 3.4 | 7.0 | ms | Cd = 0.01μF * |
| Output saturation voltage | Vsat | — | 0.2 | 0.4 | V | $V_{CC} = 5$V, Vin < 1.35V, Isink = 4mA |
| Output leakage current | $I_{OH}$ | — | — | 30 | nA | Type B |
| Output load current | $I_{OC}$ | −40 | −25 | −17 | μA | Type A, $V_{CC} = 5$V, $V_O = 1/2 \times V_{CC}$ |
| Output high voltage | $V_{OH}$ | $V_{CC}$−0.2 | $V_{CC}$−0.06 | — | V | Type A |

Note:   Please set the desired delay time by attaching capacitor of the range between 4700 pF and 10 μF.

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## Typical Characteristics


Thermal Derating


Detection Voltage vs. Ambient Temperature


Detection Voltage vs. Supply Voltage


Input Current vs. Supply Voltage


Delay Capacitance vs. Delay Time


Delay Time vs. Ambient Temperature

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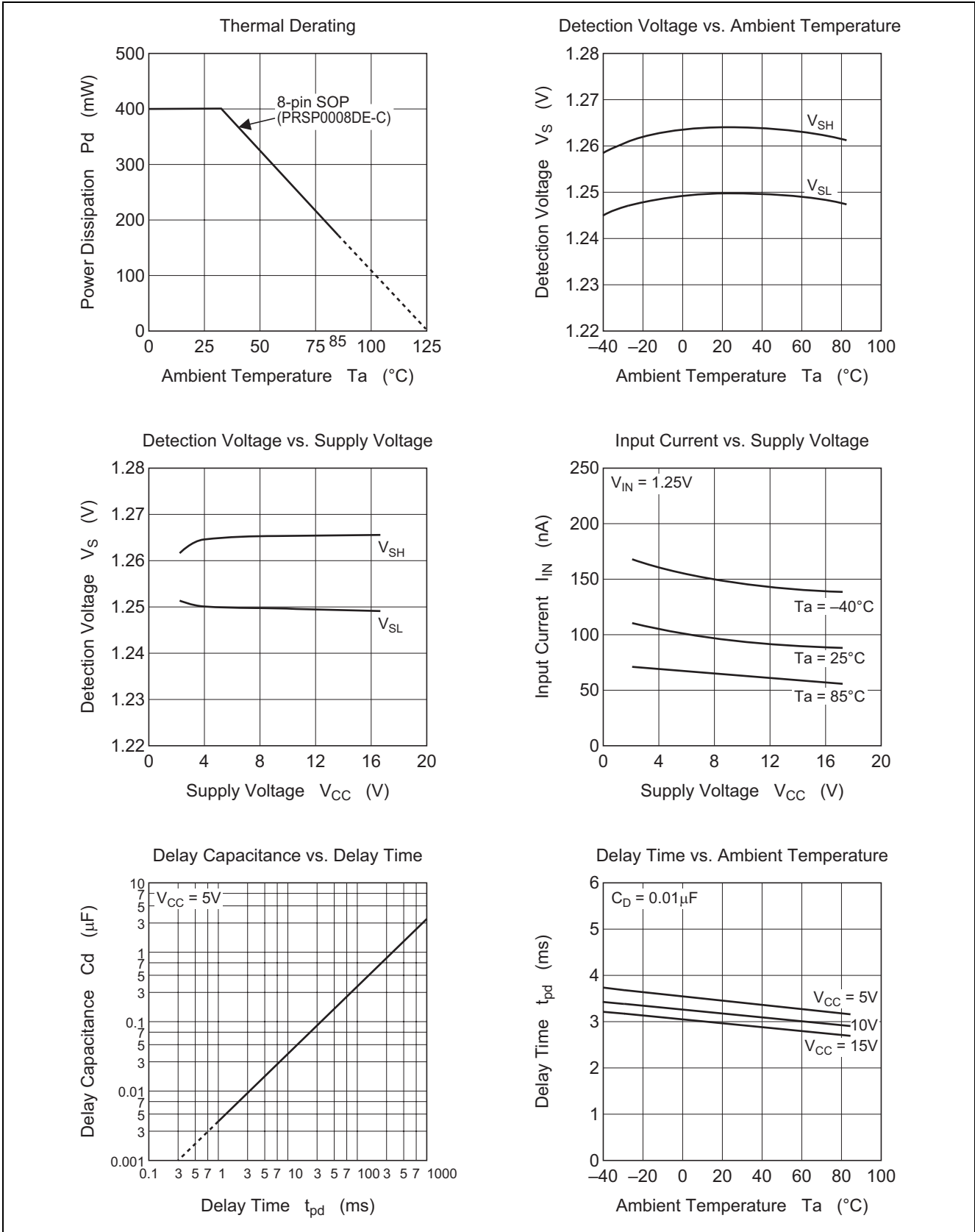
## Canstant Current at Cd pin vs. Ambient Temperature

Canstant Current at Cd pin   Ipd   (µA)

Ambient Temperature   Ta   (°C)

- $V_{CC}$ = 5V
- $V_{CC}$ = 15V
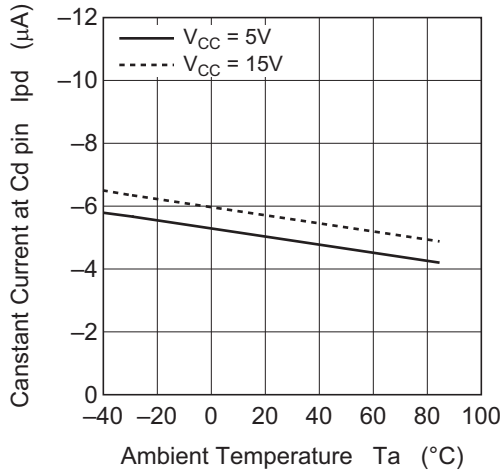
## Output Saturation Voltage vs. Output Sink Current

Output Saturation Voltage   Vsat   (V)

Output Sink Current   Isink   (mA)

Supply voltage detecting
: $V_{CC}$ = 5V
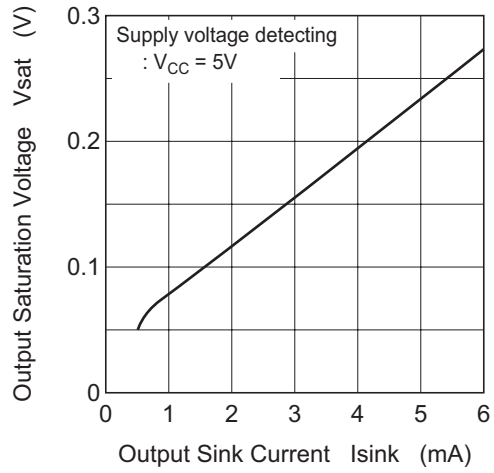
## Output Load Current vs. Output Voltage (RNA51958A)

Output Load Current   $I_{CC}$   (µA)

Output Voltage   $V_O$   (V)

$V_{CC}$ = 5V    $V_{CC}$ = 10V    $V_{CC}$ = 15V
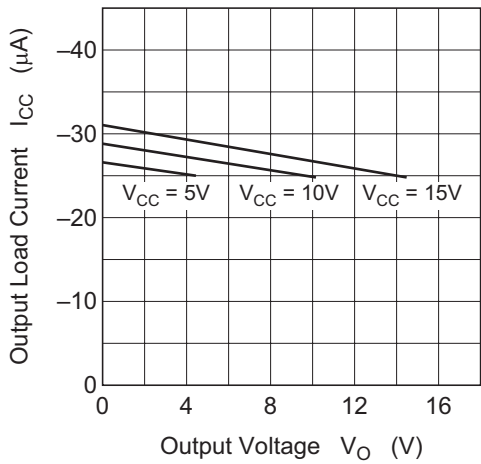
## Circuit Current vs. Supply Voltage (RNA51958B)

Circuit Current   $I_{CC}$   (µA)

Supply Voltage   $V_{CC}$   (V)

Ta = −40°C
Ta = 25°C
Ta = 85°C

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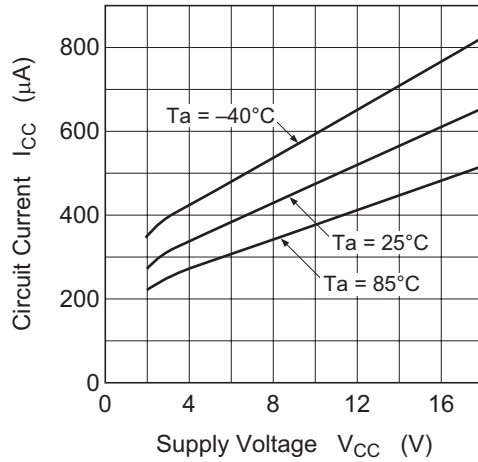
## Example of Application Circuit

### Reset Circuit of RNA51958
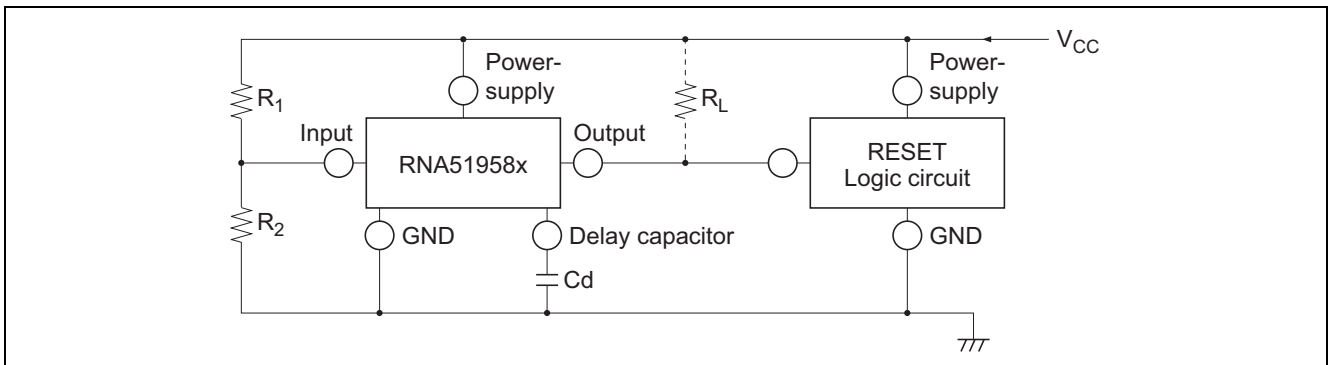


**Figure 1   Reset Circuit of RNA51958**

Notes: 1. When the detecting supply voltage is 4.25 V, RNA51953 are used.  In this case, $R_1$ and $R_2$ are not necessary.  When the voltage is anything except 4.25 V, RNA51957 and RNA51958 are used.  In this case, the detecting supply voltage is $1.25 \times (R_1 + R_2)/R_2$ (V) approximately.

The detecting supply voltage can be set between 2 V and 15 V.

2. If a longer delay time is necessary, RNA51953, RNA51957, RNA51958 are used.  In this case, the delay time is about $0.34 \times Cd$ (pF) μs.

3. If the RNA51958 and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.

4. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor $R_L$ to overcome the pull-down resistor.

5. When the reset terminal in the logic circuit is of the low reset type, RNA51953 and RNA51957 are used and when the terminal is of the high reset type, RNA51958 are used.

6. When a negative supply voltage is used, the supply voltage side of RNA51958 and the GND side are connected to negative supply voltage respectively.

### Case of Using Reset Signal except Supply Voltage in the RNA51958
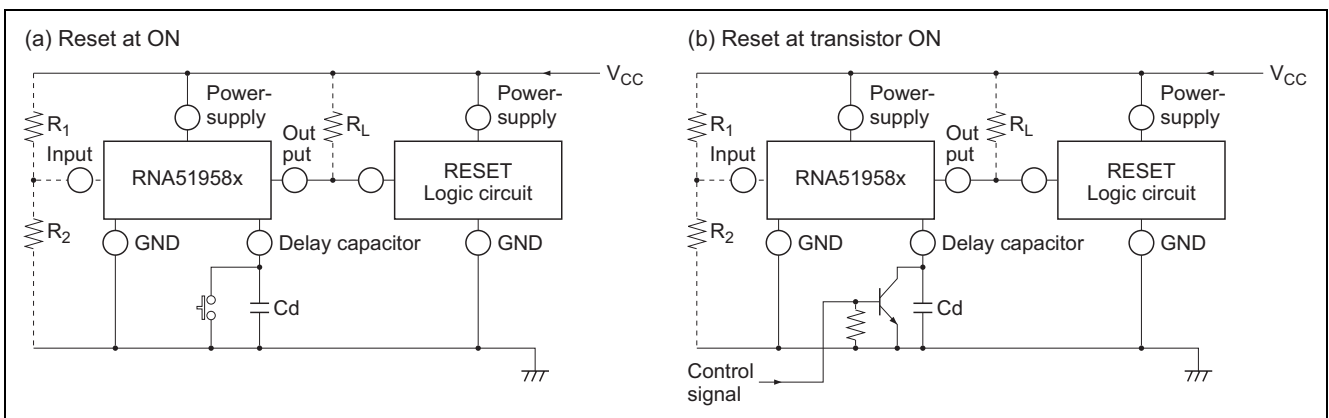


**Figure 2   Case of Using Reset Signal except Supply Voltage in the RNA51958**

## Delay Waveform Generating Circuit

When RNA51958 are used, a waveform with a large delay time can generate only by adding a small capacitor.
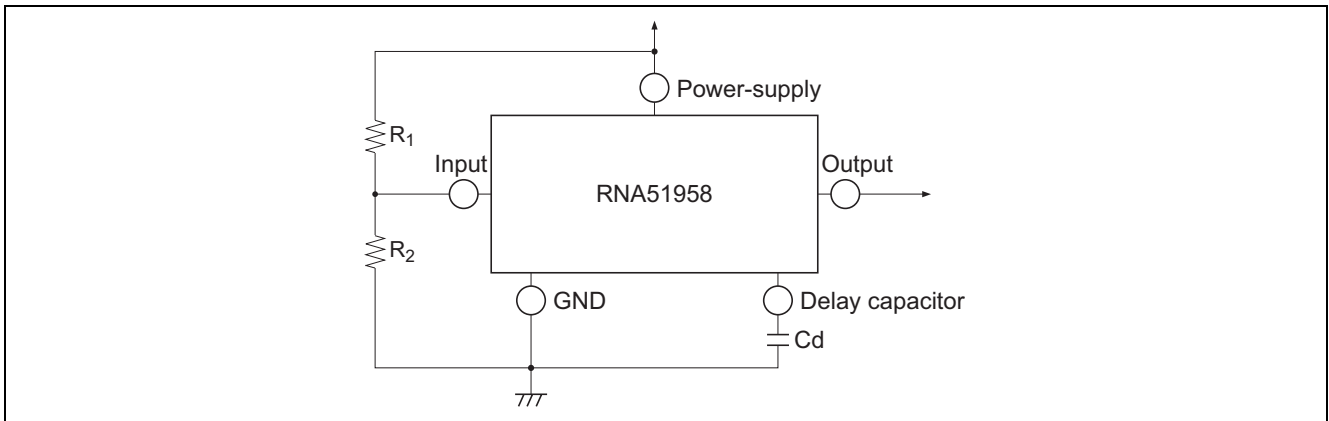


**Figure 3   Delay Waveform Generating Circuit**

## Operating Waveform



$$td \approx 0.34 \times Cd(pF)\ \mu s$$
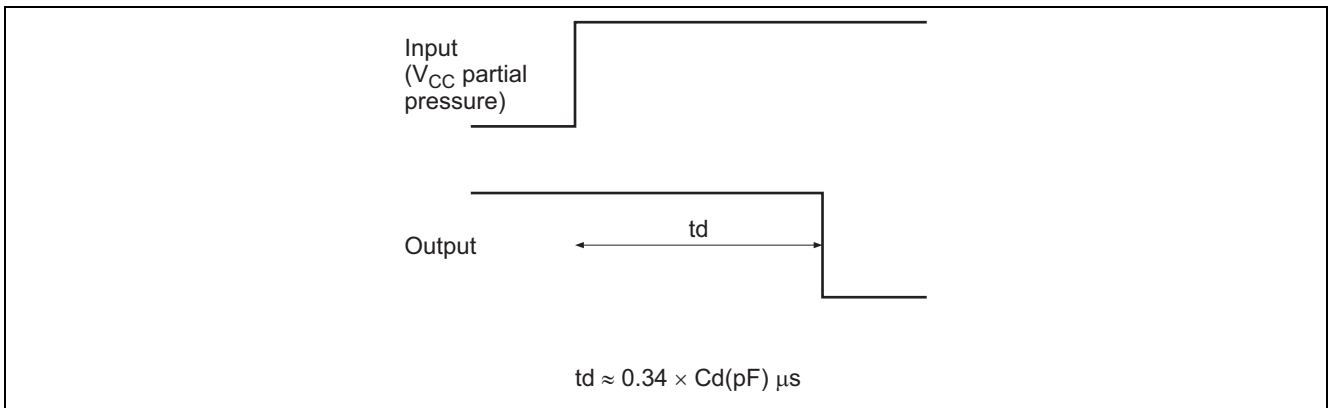
**Figure 4   Operating Waveform**

## Notice for use

### About the Power Supply Line

1. About bypass capacitor
   Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.
   Therefore, please install $C_1$ and $C_2$ for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure 5.
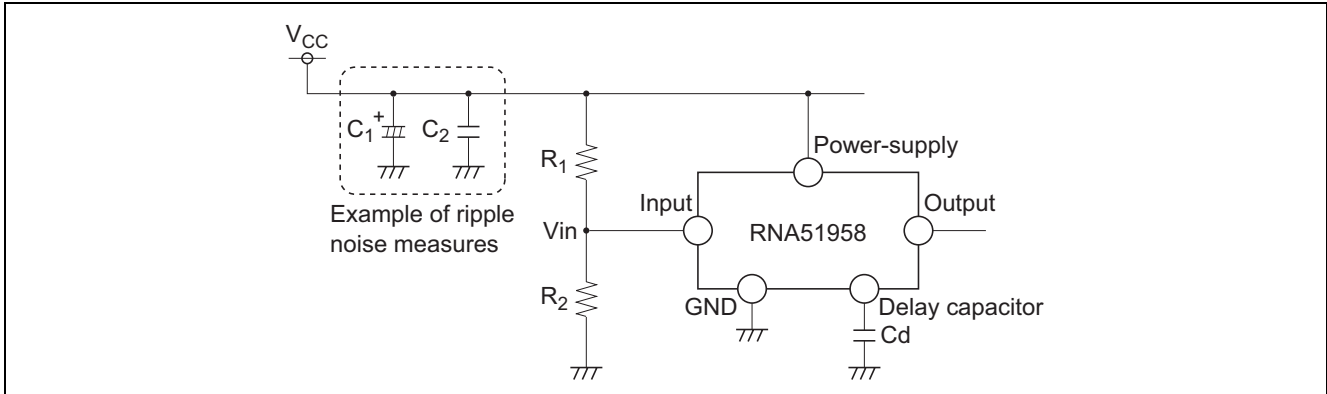


**Figure 5   Example of Ripple Noise Measures**

2. The sequence of voltage impression
   Please do not impress the voltages to the input terminals earlier than the power supply terminal.  Moreover, please do not open the power supply terminal with the voltage impressed to the input terminal.
   (The setting of the bias of an internal circuit collapses, and a parasitic element might operate.)

### About the Input Terminal

1. Setting range of input voltage
   The following voltage is recommended to be input to the input terminal (pin 2).

   about 0.8 (V) < Vin < $V_{CC}$ – 0.3 (V)  ... at $V_{CC} \leq 7$ V

   about 0.8 (V) < Vin < 6.7 (V)  ............. at $V_{CC} > 7$ V

2. About using input terminal
   Please do an enough verification to the transition characteristic etc. of the power supply when using independent power supply to input terminal (pin 2).
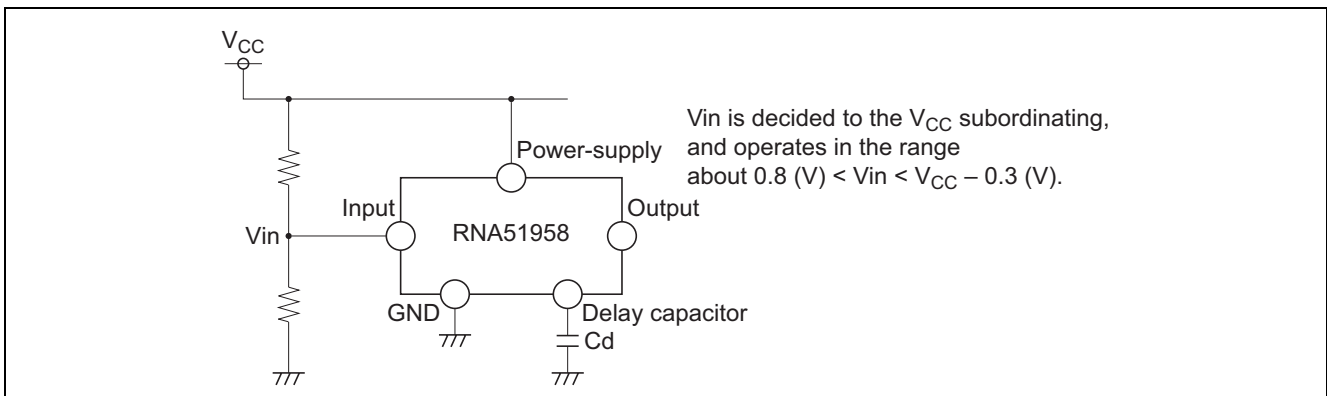


**Figure 6   Recommended Example**

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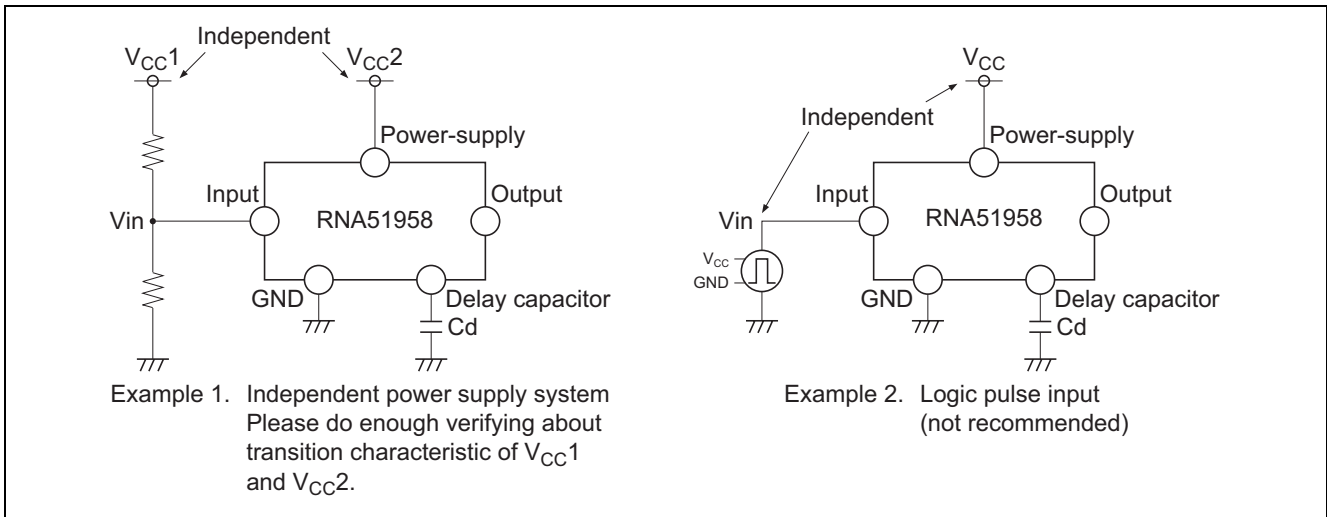
**Figure 7**

3. Calculation of detecting voltage

Detecting voltage Vs can be calculated by the following expression.

However, the error margin is caused in the detecting voltage because input current Iin (standard 100 nA) exists if it sets too big resistance.

Please set the constant to disregard this error margin.

$$V_S = 1.25 \times \left( \frac{R_1 + R_2}{R_2} \right) + \underbrace{I_{in} \times R_1}_{\text{error margin}}$$
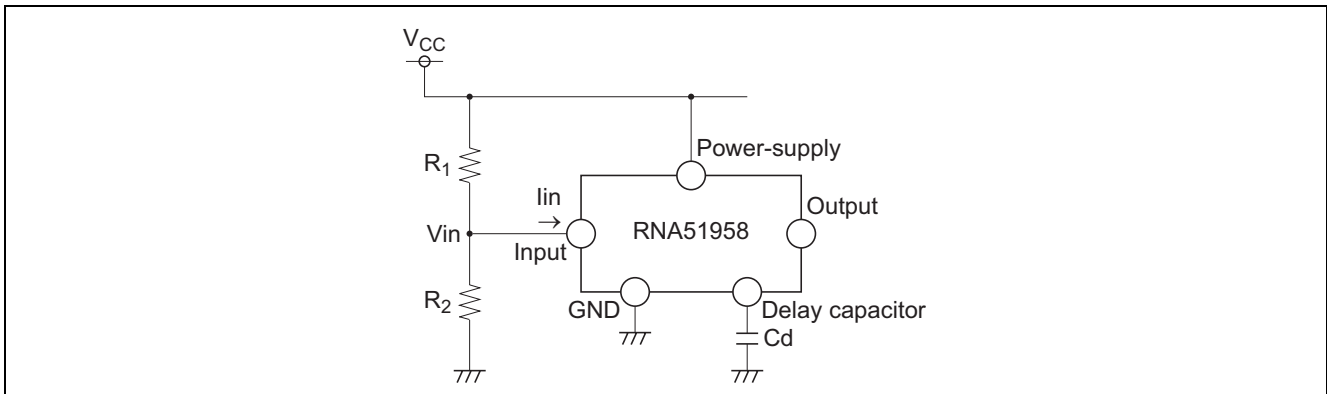


**Figure 8   Influence of Input Current**

4. About the voltage input outside ratings

Please do not input the voltage outside ratings to the input terminal.

An internal protection diode becomes order bias, and a large current flows.

## Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 µF or less.

When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.
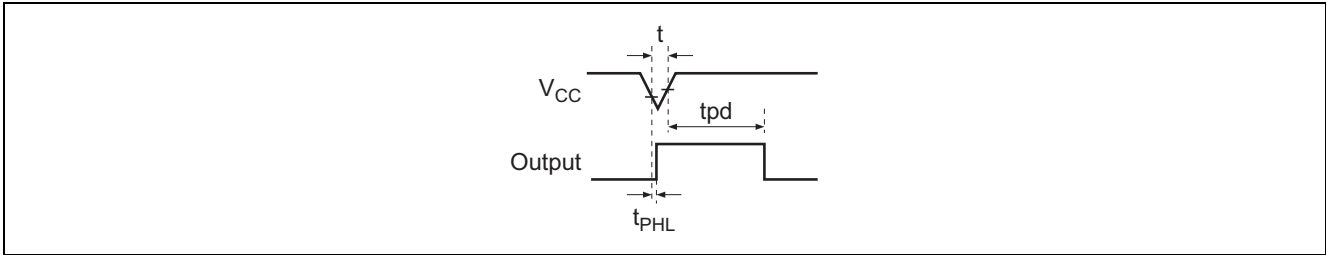


**Figure 9   Time Chart at Momentary Voltage-Decrease**

(1) The difference at delay time becomes remarkable.

A long delay setting of tens of seconds is fundamentally possible.  However, when set delay time is lengthened, the range of the difference relatively grows, too.  When a set value is assumed to be 'tpd', the difference occurs in the range from $0.47 \times$ tpd to $2.05 \times$ tpd.  For instance, 34 seconds can be calculated at 100 µF.  However, it is likely to vary within the ranges of 16-70 seconds.

(2) Difficulty to react to a momentary voltage decrease.

For example, the reaction time $t_{PHL}$ is 10 µs when delay capacitor Cd = 0.1 µF.

The momentary voltage-decrease that is longer than such $t_{PHL}$ are occurs, the detection becomes possible.  When the delay capacitance is enlarged, $t_{PHL}$ also becomes long.  For instance, it becomes about 100 to 200 µs in case of circuit constant C1 = 100 µF.

(Characteristic graph 1 is used and extrapolation in case of Cd = 100 µF.)

Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

(3) Original delay time is not obtained.

When the momentary voltage-decrease time 't' is equivalent to $t_{PHL}$, the discharge becomes insufficient and the charge starts at that state.  This phenomenon occurs at large capacitance.  And, original delay time tpd is not obtained.

Please refer to characteristic graph 2. (Delay time versus input pulse width)
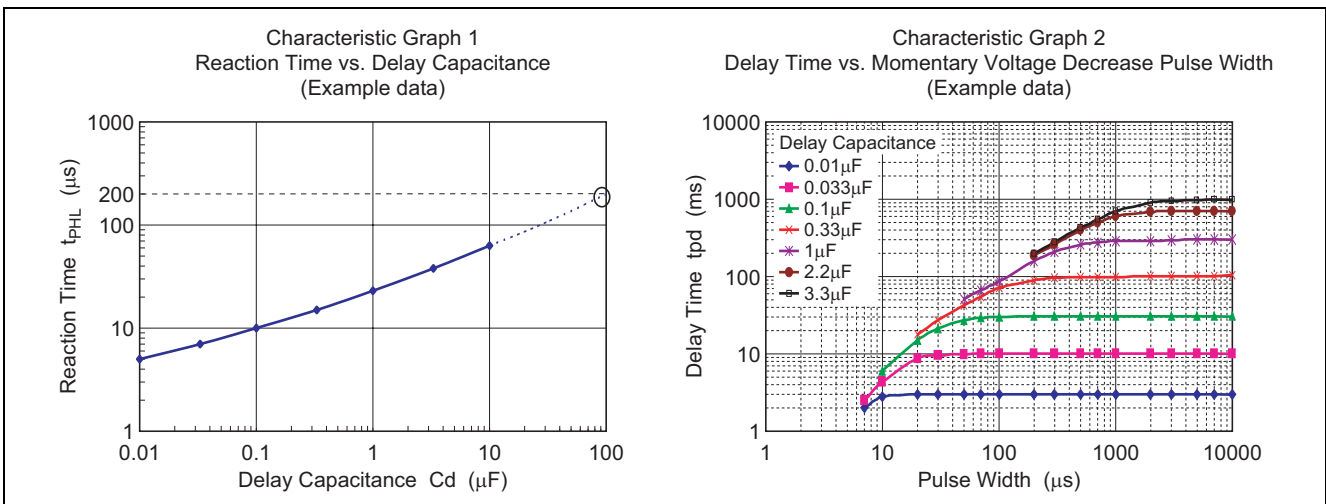


**Figure 10   Characteristic Graph**

## Setting of Output Load Resistance (RNA51958B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation.
   Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance) $R_L$ so that the output current (output inflow current $I_L$) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).
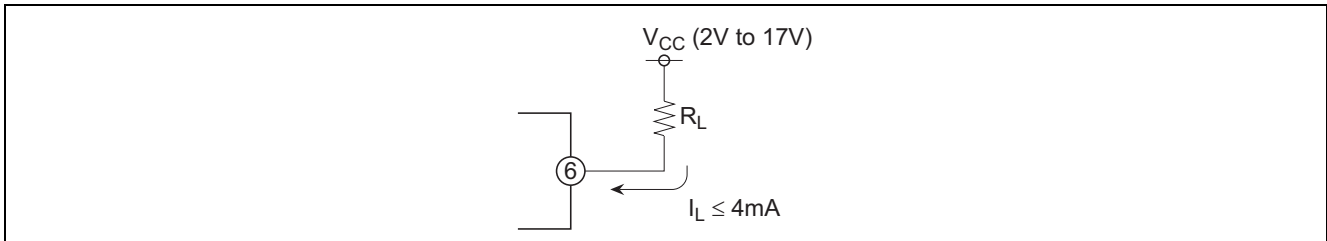


**Figure 11   Output Load Resistance $R_L$**

## Others

1. Notes when IC is handled are published in our reliability handbook, and please refer it.
   The reliability handbook can be downloaded from our homepage (following URL).
   http://www.renesas.com/fmwk.jsp?cnt=reliability_root.jsp&fp=/products/common_info/reliability
2. Additionally, please inquire of our company when there is an uncertain point on use.

# Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP8-4.4x4.85-1.27 | PRSP0008DE-C | — | 0.1g |



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section
( Ni/Pd/Au plating )

Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.65 | 4.85 | 5.05 |
| E | 4.2 | 4.4 | 4.6 |
| $A_2$ | — | 1.85 | — |
| $A_1$ | 0.00 | 0.1 | 0.20 |
| A | — | — | 2.03 |
| $b_p$ | 0.34 | 0.4 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| $\theta$ | 0° | — | 8° |
| $H_E$ | 5.7 | 6.2 | 6.5 |
| e | 1.12 | 1.27 | 1.42 |
| x | — | — | 0.12 |
| y | — | — | 0.10 |
| Z | — | — | 0.75 |
| L | 0.25 | 0.45 | 0.65 |
| $L_1$ | — | 0.90 | — |

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