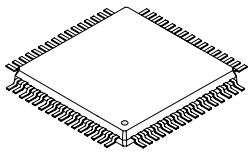
AUDIO SYSTEM CONTROL MCU

DESCRIPTION

SC9351 is an 8051-based MCU with built-in 64KByte FLASH, 8KByte RAM and abundant on-chip periphery modules including I^2C, UART, SPI, ADC and RTC, etc.



LQFP-64-10x10-0.5

FEATURES

* In system programming(ISP)
* 2.7-3.6V supply voltage for chip core, together with internal or external LDO.
* 8051 architecture compatible with MCS51 instructions
  2~4 clock cycles for per instruction
  Dual data pointer to improve the data processing efficiency
* Built-in 64Kx8 FLASH programmed by on-chip program or programmer for program memory or data memory
* Data memory IDATA : 256Byte(compatible with 8051) + 64Byte(save data when power down)
  XDATA: 8Kbyte external data memory, low 4K of which can be program memory for Flash programming
* Integrate RTC providing calendar, clock, auto leap-year adjustment, timing alarm clock and clock adjustment.
  Built-in 8-bit timer for max. 256 seconds long time timing.
* Maximum 40 general IO pins
* Four 8-bit timers T0/T1/T2/T3, where T0/T1 is the same as that of 8051; T2 supports PWM function
* Extended interrupt module with four external interrupts
* Two UART interfaces.
* One SPI interface.
* 3-channel 8-bit AD converter.
* One I^2C interface
* Various operating modes with low power dissipation

APPLICATIONS

* Desktop audio, car audio

ORDERING INFORMATION

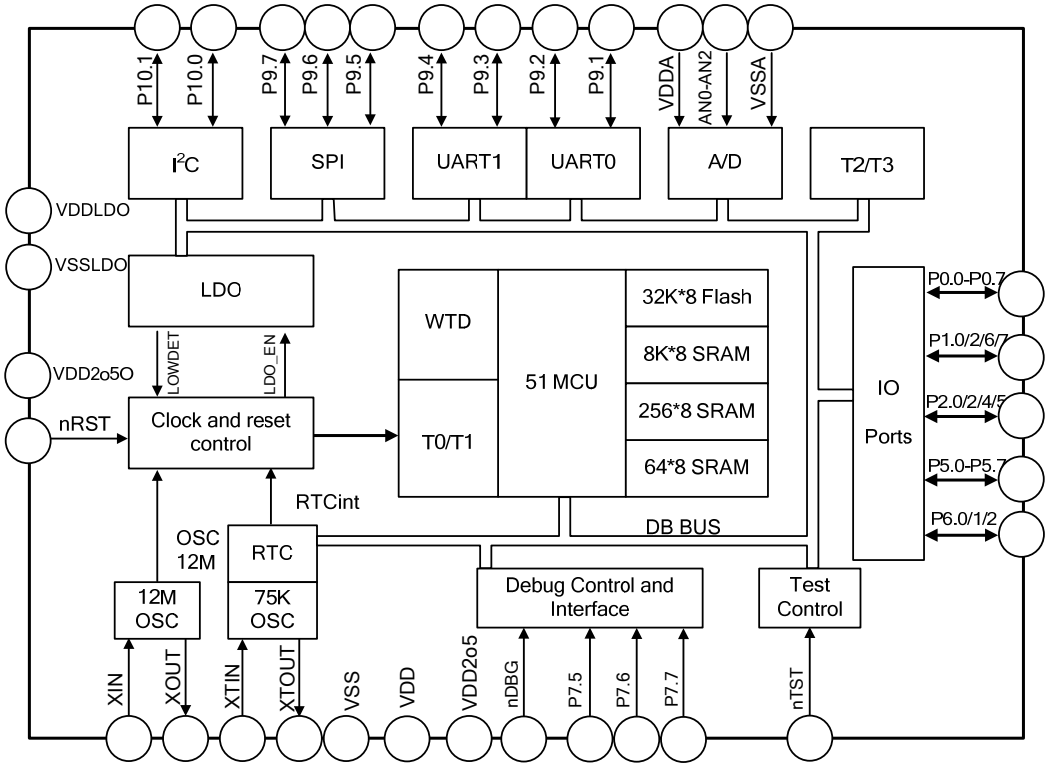
Part No.	Package	Marking
SC9351	LQFP-64-10 x 10-0.5	SC9351

Resource list

Part No.	Timer	ADC channel	SPI	UART	I^2C	IO Qty.Note1	External interrupt
SC9351	4	3	1	2	1	40	4

Note 1: three pins of P7 port are shared with debug ports.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

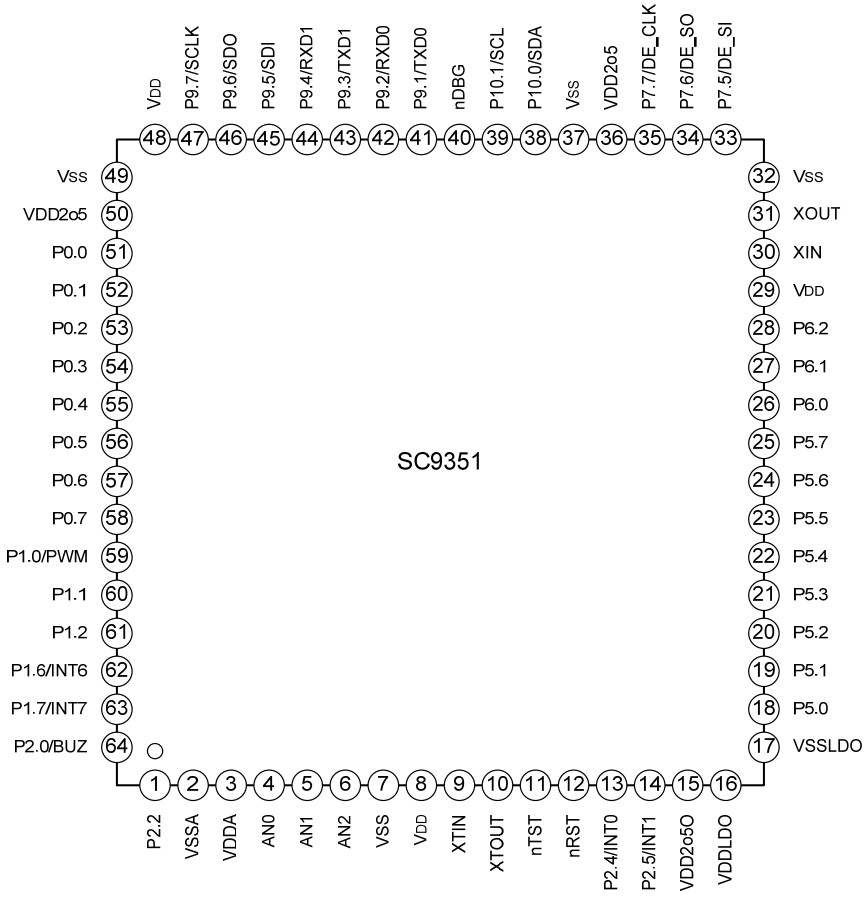
Characteristics	Symbol	Ratings	Unit
Power supply	V_{DD}	-0.3~+5.0	V
Input voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Storage temperature	T_{STG}	-65~+150	°C
Operating temperature	T_{OPR}	-40~+85	°C
ESD	Vesd	2	KV

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=3.3V, T_{amb}=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Power Supply	V_{DD}	-	2.7	3.3	3.6	V
I/O Pull-Up Resistor	R_{pu}	-	--	50		KΩ
Operating Frequency	F_{CPU}	-		12		MHz
RTC Input Frequency	F_{RTC}	-	--	75K		Hz
High-Frequency Operating Current1	I_{OPH1}	F_{CPU} = 12MHz (Other modules are closed except for MCU and SRAM is used as program memory.)	--	7.5	--	mA
High-Frequency Operating Current2	I_{OPH2}	F_{CPU} = 12MHz (Other modules are closed except for MCU and FLASH is used as program memory.)	--	8	--	mA
Low-Frequency Operating Current1	I_{OPL1}	F_{CPU} = 75KHz (Other modules are closed except for MCU and RTC is powered by external LDO, and SRAM is used as program memory (LDO power dissipation is not included))	--	70	--	μA
Low-Frequency Operating Current2	I_{OPL2}	F_{CPU} = 75KHz (Other modules are closed except for MCU and RTC is powered by internal LDO, and SRAM is used as program memory)	--	400	--	μA
Low-Frequency Operating Current3	I_{OPL3}	F_{CPU} = 75KHz (Other modules are closed except for MCU and RTC is powered by internal LDO, and FLASH is used as program memory)	--	1.5	--	mA
Sleep Current 1	I_{s1}	F_{CPU} = 75KHz (MCU is in sleep mode, other modules are closed except for RTC powered by external LDO, and SRAM is used as program memory (LDO power dissipation is not included))	--	40	--	μA
Sleep Current 2	I_{s2}	F_{CPU} = 75KHz (MCU is in sleep mode, other modules are closed except for RTC powered by internal LDO, and SRAM is used as program memory)	--	360	--	μA

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Sleep Current 3	I_{S3}	F_{CPU} = 12MHz (MCU is in sleep mode, other modules are closed except for RTC powered by internal LDO, and SRAM or FLASH can both be program memory)	--	3.5	--	mA
Quiescent Current	I_Q	Close main oscillator, LDO and other modules except for RTC working at 75K clock frequency.	-	14	--	μA
High-Level Output Current (Except For Port P10)	I_{OH}	V_{OH} = 3V	-	-3.0	-	mA
Low-Level Output Current(Except For Port P10)	I_{OL}	V_{OL} = 0.3V	-	4.0	-	mA
Low-Level Output Current (Port P10)	I_{OL}	V_{OL} = 0.3V	-	9.0	-	mA
Input High Voltage	V_{IH}	P0/P1/P2/P9	2.0	-	-	V
Input High Voltage	V_{IH}	P5/P6/P7	1.5	-		V
Input High Voltage	V_{IH}	P10	1.5	-		V
Input Low Voltage	V_{IL}	P0/P1/P2/P9		-	0.7	V
Input Low Voltage	V_{IL}	P5/P6/P7		-	0.8	V
Input Low Voltage	V_{IL}	P10		-	0.8	V

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Function
1	P2.2	I/O	In extended bus mode, output notDMRD; alternate function is external interrupt InT2
2	VSSA	--	Ground of ADC
3	VDDA	--	Power supply of ADC
4~6	AN0~AN2		Input channel 0~2 of ADC
7	VSS	--	Digital ground
8	VDD	--	Power supply of IO, RTC and 64Byte RAM
9	XTIN	I	75KHz oscillator input pin
10	XTOUT	O	75KHz oscillator output pin
11	nTST	I	Test enable pin internally connected with pull-up resistor; High level is connected for normal use.
12	nRST	I	Reset pin internally connected with pull-up resistor; low level reset.
13	P2.4/INT0	I/O	General I/O pin; alternate function is external interrupt input INT0

Pin No.	Pin Name	I/O	Pin Function
14	P2.5/INT1	I/O	General I/O pin; alternate function is external interrupt input INT1
15	VDD2o5O	--	2.5V output pin of LDO with a 1~10uF capacitor to power the core
16	VDDLDO	--	Power supply of LDO, input voltage is 2.7~3.3V
17	VSSLDO	--	Ground of LDO
18~25	P5.0~5.7	I/O	General I/O port P5 with 8 pins
26~28	P6.0~6.2	I/O	General I/O port P6 with 3 pins
29	VDD	--	3.3V power supply
30	XIN	I	12MHz oscillator input pin.
31	XOUT	O	12MHz oscillator output pin.
32	VSS	--	Ground
33	P7.5/DE_SI	I/O	General I/O pin; used as data serial-in in debug mode.
34	P7.6/DE_SO	I/O	General I/O pin; used as data serial-out in debug mode.
35	P7.7/DE_CLK	I/O	General I/O pin; input synchronous communication clock in debug mode
36	VDD2o5	--	2.5V power input
37	VSS	--	Ground
38	P10.0/SDA	I/O	General I/O pin; alternate function is data port of I^2C
39	P10.1/SCK	I/O	General I/O pin; alternate function is clock of I^2C
40	nDBG	I	Debug mode selection with pull-up resistor; enter Debug mode when it is connected to ground.
41	P9.1/TXD0	I/O	General I/O pin; alternate function is TXD of UART0
42	P9.2/RXD0	I/O	General I/O pin; alternate function is RXD of UART0
43	P9.3/TXD1	I/O	General I/O pin; alternate function is TXD of UART1
44	P9.4/RXD1	I/O	General I/O pin; alternate function is RXD of UART1
45	P9.5/SDI	I/O	General I/O pin; alternate function is data-in of SPI
46	P9.6/SDO	I/O	General I/O pin; alternate function is data-out of SPI
47	P9.7/SCLK	I/O	General I/O pin; alternate function is clock of SPI
48	VDD	--	3.3V power supply
49	VSS	--	Ground
50	VDD2o5	--	2.5V power input
51~58	P0.0~0.7	I/O	General I/O port P0 with 8 pins
59	P1.0/PWM	I/O	General I/O pin; alternate function is PWM waveform output
60	P1.1	I/O	General I/O pin
61	P1.2	I/O	General I/O pin
62	P1.6/INT6	I/O	General I/O pin; alternate function is external interrupt input INT6
63	P1.7/INT7	I/O	General I/O pin; multiplexing with external interrupt input INT7
64	P2.0/BUZ	I/O	General I/O pin; multiplexing with BUZ output

FUNCTION DESCRIPTIONS

1. MCU function description

1.1 Introduction to MCU

SC9351 adopts S51 MCU core with embedded 64KByte FLASH, supporting external instruction memory and data memory extension. Standard 805x assembler and compiler can be used for software development and maximum 4 hardware breaks supported in Debug mode are convenient for program development.

1.2 Introduction to address space

Instruction and data addresses are programmed separately and each occupies 64K address space.

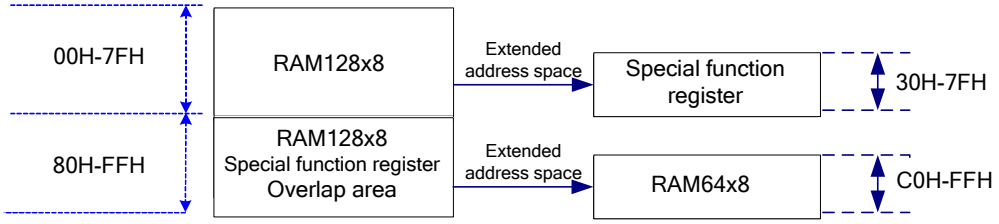
- **Data memory address assignment**

Compatible with 8051, it also includes address of internal data memory (IDATA) and external data memory (XDATA), which are accessed by MOV instruction and MOVX instruction respectively.

✧ **Internal data memory**

The address space of internal data memory is 0000H~00FFH including several memory areas which are different in physical characteristics. The 128 bytes memory from 00H to 7FH is RAM. Different from general 8051, the 80 bytes memory from 30H to 7FH can be extended as special function register whose addressing method is the same as RAM.

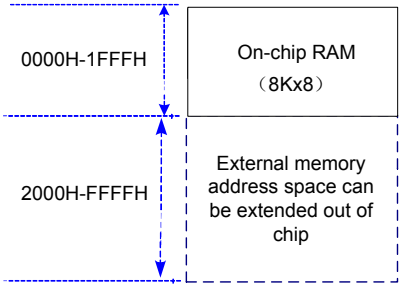
The 128 bytes memory from 80H to FFH is the overlap area of RAM and special function register, which are distinguished by their different addressing method (special function register is accessed by Direct addressing commands, while the RAM is accessed by indirect addressing commands). Different from general 8051, the 64 bytes (from C0H to FFH) can be extended as extra RAM that can be accessed by indirect addressing commands.



Address space of internal data memory

✧ **External data memory**

The address space of external data memory is 0000H~FFFFH which can only be accessed by MOVX instruction. SC9351 integrates 8K bytes RAM with address of 0000H~1FFFH as external data memory which can be extended to 64K according to the requirements.



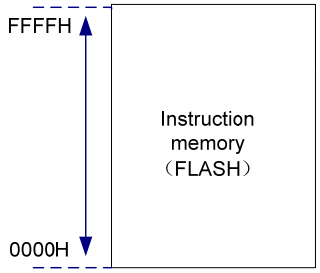
Address space of external data memory

1.3 External data memory extension

When data memory is written/read by CPU through MOVX instruction, internal 8K RAM is written/read if the address is within 0X0000~0X1FFF, while external data memory is written/read if the address is beyond 0X1FFF. External data memory extension is not supported here.

- **Instruction memory address assignment**

Same as general 8051, the address space of instruction memory is 64K. SC9351 integrates 64K bytes FLASH as internal instruction memory.



Address space of instruction memory

1.4 Introduction to DPTR

DPTR is a 16-bit data pointer, which can be used by MOVX instruction as indirect addressing register to access the external data memory from 0000H to FFFFH. 8051 has only one DPTR, which is not enough when accessing the external data memory frequently. So SC9351 adopts two DPTRs to access the external data memory conveniently.

The two DPTRs share the same address (DPH:83H; DPL:82H) and behavior, and different DPTR can be got through DPS control bit.

2. Special function register (SFR)

Address	Name	R/W	Description
8051 special register			
81H	SP	R/W	Stack pointer
82H	DPL	R/W	Data pointer low
83H	DPH	R/W	Data pointer high
87H	PCON	R/W	Power control register

Address	Name	R/W	Description
88H	TCON	R/W	Timer/counter control register
89H	TMOD	R/W	Timer/counter mode control register
98H	SCON	R/W	Serial port control register
99H	SBUF	R/W	Serial data buffer
8AH	TL0	R/W	Timer/counter 0 (low byte)
8BH	TL1	R/W	Timer/counter 1 (low byte)
8CH	TH0	R/W	Timer/counter 0 (high byte)
8DH	TH1	R/W	Timer/counter 1 (high byte)
8EH	TIMPS	R/W	Prescaler control register of TIMER
A2H	AUXR1	R/W	Data pointer select register of DPTR
A8H	IE	R/W	Interrupt enable control register
B8H	IP	R/W	Interrupt priority control register
D0H	PSW	R/W	Program status word
E0H	ACC	R/W	Accumulator of CPU
F0H	B	R/W	Register B of CPU
Operating mode register (register extended)			
31H	PSM_OSCREF	W	Access control address of 75K OSC gain setting
32H	PDN_OSCREF	W	Access control address of 75K OSC enable
33H	MCLKSEL	W	Access control address of CPU clock selection
34H	PDN_OSCIN	W	Access control address of 12M OSC enable
35H	PDN_LDO	W	Access control address of LDO enable
36H	OSCRSTCTRL	R	System clock and power status register
37H	HSCSEL	W	Access control address of high-speed OSC selection
38H	LBDCTRL	R/W	LBD control register
External interrupt register (register extended)			
39H	EINTF	R/W	External interrupt flag
3AH	EXTINTENABLE	W	External interrupt source identification enable register
3BH	EINT_EDGE	W	External interrupt control register
3CH	IPLSR3_E	R/W	Interrupt priority selection register 4
3DH	IPLSR2_E	R/W	Interrupt priority selection register 3
3EH	IPLSR1_E	R/W	Interrupt priority selection register 2
3FH	IPLSR0_E	R/W	Interrupt priority selection register 1
40H	IER_E	R/W	External interrupt (INT0 extension) enable register
41H	IPR_E	R/W	External interrupt source identification register
42H	ISR_E	R/W	Interrupt status register
43H	ICR_E	R/W	Interrupt mask control register
IO register (register extended with address within 30~7FH)			
46H	P10OD	R/W	Open-drain output control of port P10
47H	P10PU	R/W	Pull-up control register of port P10
49H	P10	R/W	Port register of P10
4BH	P9OD	R/W	Open-drain output control of port P9

Address	Name	R/W	Description
4CH	P9PU	R/W	Pull-up control register of port P9
4DH	P9DDR	R/W	Direction control register of port P9
C0H	P9	R/W	Port register of P9
4F~50H registers unused, and read/write is not allowed			
51H	P7OD	R/W	Open-drain output control of port P7
52H	P7PU	R/W	Pull-up control register of port P7
53H	P6OD	R/W	Open-drain output control of port P6
54H	P6PU	R/W	Pull-up control register of port P6
55H	P5OD	R/W	Open-drain output control of port P5
56H	P5PU	R/W	Pull-up control register of port P5
57H	P4OD	R/W	Open-drain output control of port P4
58H	P4PU	R/W	Pull-up control register of port P4
5AH~5DH registers unused, and read/write is not allowed			
5FH	P2OD	R/W	Open-drain output control of port P2
60H	P2PU	R/W	Pull-up control register of port P2
D4H	P2DDR	R/W	Direction control register of port P2
A0H	P2	R/W	Port register of P2
64H	P1OD	R/W	Open-drain output control of port P1
65H	P1PU	R/W	Pull-up control register of port P1
66H	P1DDR	R/W	Direction control register of port P1
90H	P1	R/W	Port register of P1
69H	P0D	R/W	Open-drain output control of port P0
6AH	P0PU	R/W	Pull-up control register of port P0
6BH	P0DDR	R/W	Data direction control register of port P0
80H	P0	R/W	Port register of P0
RTC register(register extended with address within 30~7FH)			
6DH	SECADJL	R/W	Second cycle adjust register
6EH	SECADJH	R/W	Second cycle adjust register
6FH	SECADJCON	R/W	Second adjust control register
70H	RTC_CS	R/W	RTC control and status register
71H	YEARH	R/W	High 8-bit register of year
72H	SEC	R/W	Second register
73H	MIN	R/W	Minute register
74H	HOUR	R/W	Hour register
75H	DAY	R/W	Day register
76H	WEEK	R/W	Week register
77H	MON	R/W	Month register
78H	YEARL	R/W	Low 8-bit register of year
79H	MIN_ALARM	R/W	MIN alarm control register
7AH	HOUR_ALARM	R/W	HOUR alarm control register
7BH	DAY_ALARM	R/W	DAY alarm control register

Address	Name	R/W	Description
7CH	WEEK_ALARM	R/W	WEEK alarm control register
7DH	CLKOUT_CTRL	R/W	CLKOUT control register
7EH	TMCON	R/W	RTC built-in timer control
7FH	TMREF	R/W	Initial value of RTC built-in timer
WDT register			
84H	WDT_CTRL	R/W	WDT control register
85H	WDT_CLR0	W	WDT clear register 0
86H	WDT_CLR1	W	WDT clear register 1
91H	SLEEP_CTRL	R/W	Sleep mode control register
92H	SYS_STATUS	R/W	System status register
Register extension setting register			
93H	CS_SFR	W	Access switch control register of data area 30~7F
RAM extension setting register			
94H	CS_INTDM	W	Access switch control register of data area C0~FFH
Port multiplex control register			
96H	IOMUX	R/W	IOPort multiplex control register
Interrupt register			
97H	ICR_I	R/W	Interrupt mask control register
9AH	ISR_I	R	Interrupt status register
9BH	IPR_I	R	Internal interrupt source identification register
9CH	IER_I	R/W	INT1 extension interrupt (generated by internal modules) enable control
9DH	IPLSR0_I	R/W	Interrupt priority selection register 4
9EH	IPLSR1_I	R/W	Interrupt priority selection register 3
9FH	IPLSR2_I	R/W	Interrupt priority selection register 2
A1H	IPLSR3_I	R/W	Interrupt priority selection register 1
Flash program register			
A5H	FSHWRADRH	R/W	High 8-bit address register of FLASH write
A6H	FSHWRADRL	R/W	Low 8-bit address register of FLASH write
A7H	FSHWRDATA	R/W	FLASH write data register
A9H	FSHWRCON1	R/W	FLASH write control register 1
AAH	FSHWRCON2	R/W	FLASH write control register 2
ABH	FSHERSCON1	R/W	FLASH erase control register 1
ACH	FSHERSCON2	R/W	FLASH erase control register 2
ADH	FSHTIMER	R/W	FLASH write/erase prescaler control register
AEH	FlashCtrl	R/W	FLASH switch control register
SPI register			
B1H	SPICR	R/W	SPI control register
B2H	SPISR	R	SPI status register
B3H	SPIBUF	W/R	SPI transmit/receive buffer
B4H	SPIBR	R/W	SPI baud rate setting register

Address	Name	R/W	Description
B5~BCH registers unused, and read/write is not allowed			
BDH	BUZCR	W/R	BUZZER output control register
I²C register			
BEH	I2CRXB	R	Second stage buffer of data receive
BFH	I2CSR	R	Status register
DFH	I2CCR	W/R	Control register
C1H	I2CSLA	W/R	Slave address/host baud rate setting register
C2H	I²CBUF	W/R	Receive/transmit buffer
UART0 register			
C3H	UART_BUF0	W/R	UART0 receive/transmit buffer
C4H	SCON0	W/R	UART0 control register
C5H	BRCON0	W/R	UART0 baud rate control register
C6H	BRTIMER0	W/R	UART0 baud rate setting register
UART1 register			
C7H	UART_BUF1	W/R	UART1 receive/transmit buffer
C9H	SCON1	W/R	UART1 control register
CEH	BRCON1	W/R	UART1 baud rate control register
CFH	BRTIMER1	W/R	UART1 baud rate setting register
ADC register			
D1H	ADATA	R	AD conversion data register
D2H	ADCON	W	AD control register
D3H	ADCIS	W	AD channel input select register
T2/T3 register			
D5H	T2CON	R/W	T2 control register
D6H	T2REF	R/W	T2 preset register
D7~D9FH registers unused, and read/write is not allowed			
DAH	T3CON	R/W	TIMER3 control register
DBH	T3REF	R/W	TIMER3 preset register
EE~FFH registers unused, and read/write is not allowed			

3. Introduction to operating mode

SC9351 provides various operating modes: high-frequency, low-frequency, Sleep and power-down hold. Please see details below:

3.1 High-frequency operating mode

In this mode, 12MHz or 12MHz divided-by-2 is selected by software to provide high-speed clock for CPU (use MClk for short in the following), I²C, SPI, UART, ADC, TIMER and WDT, etc. While, 75KHz oscillator provides clock for RTC. Operating mode can be switched from high-frequency to low-frequency, Sleep or power-down hold through program setting.

3.2 Low-frequency operating mode

In this mode, 75KHz is selected to provide clock for CPU, RTC and all the other function modules and operating mode can be switched from low-frequency to high-frequency or other modes through program setting.

Note: 1. 12MHz oscillator needs to be closed by software after MCU being switched to low-frequency operating mode.

2. High-frequency oscillator needs to be open first by software for at least 1ms until it is stable when operating mode is switched from low-frequency to high-frequency.

3.3 Sleep mode

In this mode, the clock for CPU, WDT, I^2C, SPI, UART and ADC is closed, while oscillator still works and TIMER, RTC, IO port and interrupt system still work under clock.

CPU can be waken up by allowed interrupt events caused by external interrupt, RTC, or TIMER and back to former operating mode to execute the corresponding interrupt service routine.

3.4 Power-down hold mode

This mode is provided only when the chip adopts internal LDO(this operating mode is not available when adopting external LDO). After LDO is closed, CPU, 64Kx8FLASH, 8Kx8RAM, 256x8RAM, I^2C, SPI, UART, ADC, TIMER and WDT are powered down because of no 2.5V supply voltage, while 12MHz/75KHz oscillator, RTC, 64x8RAM, IO port and external interrupt extension modules fed by external power supply still work.

In this mode, 75KHz oscillator provides clock for RTC; 75KHz or 12MHz oscillator provides clock for IO, interrupt extension module intc_e. RTC and external interrupt can wake up LDO and reset CPU to back to former operating mode.

Data can be saved in 64x8RAM in this mode.

4. Introduction to function module

4.1 Clock system

There are two oscillators and 75KHz oscillator provides clock for low-frequency operating, 12MHz oscillator provides clock (12MHz/6MHz) for high-frequency operating.

- 75KHz and 12MHz oscillators are programmable control.
- In power-down hold mode, 12MHz oscillator can be closed and 75KHz oscillator provides clock for RTC and external extension module.

Note: unless otherwise specified, the clock source mentioned below is 12MHz or 75KHz.

4.2 Reset control

There are power-on reset/external keypress reset, low voltage detect reset functions. What's more, RTC interrupt and external interrupt will also generate reset signal in power-down hold mode to reset CPU to come back to operating mode.

- In power-down hold mode, external interrupt and RTC interrupt will generate reset signal to wake up LDO and reset CPU, which has no effect on register value of RTC, oscillator control, clock control and interrupt extension control, etc. About 15ms time delay is needed for LDO stable.
- In other operating modes (high-frequency, low-frequency, Sleep), LDO is working normally and

external interrupt, RTC interrupt will generate interrupt request instead of reset signal.

- Power-on reset by connecting resistor, capacitor or external keypress reset by connecting reset key to pin nRST are both available.
- LDO low-voltage detect signal can reset MCU and has no effect on RTC.
- WDT overflow reset can reset CPU and has no effect on LDO, RTC, clock system, operating mode control module and interrupt extension module, etc.

4.3 Interrupt

There are 18 interrupt sources in SC9351 except for reset signals. These interrupt sources enter interrupt processing module through five channels same as 8051.

Five interrupts of S51 are supported: INT0, INT1, TF0, TF1, TI/RI, where, INT0 is extended to 4 external interrupts, INT1 (internal interrupt extended) is shared by various internal modules (such as I2C and SPI), and TI/RI interrupt channel is corresponding to transmitting/receiving interrupt of two UARTs. High-level trigged interrupts TF0 and TF1 separately belong to timer/counter0 and timer/counter1 of 8051.

Priority and mask function setting for external/internal interrupts extended is independent and software inquiry should be used by interrupt routine due to external/internal interrupts extended share one interrupt entry. (For example, interrupt source register should be checked to make sure which pin triggers the interrupt after INT0 responds to interrupt.)

External 4 interrupts are from pin P1.6/P1.7/P2.4/P2.5, which can be programmable as rising-edge or falling-edge trigger, and share the entry address 0003H corresponding to INT0 of 8051. Each interrupt source can be set to a corresponding priority (0~7), which is different according to different sources. And CPU only responses to the interrupt request with PRI (bigger number for higher PRI) higher than the setting value of interrupt control register (ICR). The execution of interrupt service routine with low PRI will not be broken by the interrupt with high PRI which will be responded after the low PRI interrupt is completed due to these interrupts share the same degree of CPU. The interrupts can be responded as long as the interrupt flag is active, so external interrupts will not be lost.

Internal interrupts of SC9351 are mainly from its embedded digital and analog modules including I^2C, SPI, ADC, T2, T3 and RTC, etc., and share the entry address 0013H corresponding to INT1 of 8051.

When serial interrupt is processed, RI and TI requests of UART0 share TI of 8051, while RI and TI requests of UART1 share RI of 8051 due to there are two UARTs in SC9351. The interrupt source is decided by inquiring corresponding flag and the flag RI/TI is cleared automatically by hardware after interrupt response.

The interrupt processing of S51 is the same as that of 8051, mainly controlled by interrupt enable control register IE and interrupt PRI register IP.

The following 3 steps must be executed to use interrupts of S51:

1. Set EA of IE register to 1
2. Set corresponding interrupt enable bit to 1
3. After interrupt is triggered, program pointer jumps to corresponding vector address and interrupt service routine starts to be executed.

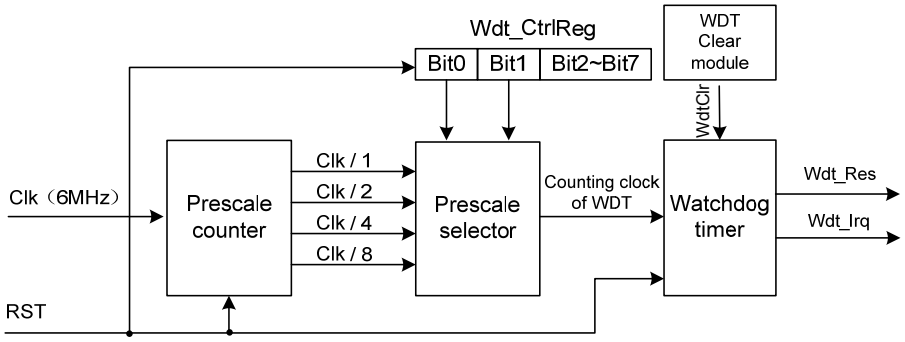
Table 1: SC9351 interrupt list

Interrupt module	Interrupt source		Entry of 8051	Corresponding vector address
External interrupt (4)	EINT0	P2.4	INT0	0003H
	EINT1	P2.5		
	EINT6	P1.6		
	EINT7	P1.7		
Timer 0	T0 overflow interrupt		TF0	000BH
Internal interrupt	PINT0	Reserved	INT1	0013H
	PINT1	I^2C interrupt		
	PINT2	SPI interrupt		
	PINT3	ADC interrupt		
	PINT4	Reserved		
	PINT5	T2 overflow interrupt		
	PINT6	T3 overflow interrupt		
	PINT7	RTC interrupt		
Timer1	T1 overflow interrupt		TF1	001BH
Serial port interrupt	UART0(RI0,TI0)		TI	0023H
	UART1(RI1,TI1)		RI	

4.4 WDT

Watchdog (WDT) is mainly used for program monitor, and generates reset signal after the counting overflows to avoid the error execution state. The clock source of WDT counter is 6MHz. In Sleep mode, the clock of WDT is closed and doesn't work.

Default latency time of WDT is 175ms after reset and the maximum timing time set by program is 1398ms.



IP_WDT structure diagram

Note: In debug mode (nDBG is connected to GND), WDT doesn't work when MCU is single-step running, and normal work when MCU is full-speed running.

4.5 Timer T0/T1

The operating mode is the same as 8051 with additional programmable prescaler to control the clock frequency

of TIMER, which is different from frequency divided-by-12 of 8051.

MCLK/2, MCLK/4, MCLK/8, MCLK/16, MCLK/32, MCLK/64, MCLK/128 and MCLK/256 can be selected for timer/counter, and MCLK can be 12MHz, 6MHz and 75KHz according to different MCU operating modes.

Note: For SC9351, T0 is connected to 0 and T1 is connected to 1, so there is no counter mode.

4.6 Timer T2/T3

Operating mode of T2: internal timing/counting and PWM mode

Operating mode of T3: internal timing mode

Six clocks below can be selected according to different operating mode:

- MCLK/16
- MCLK/64
- OSC75K
- MCLK /256
- MCLK /512,
- MCLK /1024

4.7 I²C

The I^2C interface of SC9351 has configurable host and slave modes with 7-bit device addressing function supporting 400Kbps baud rate; however, multiple hosts and the relevant arbitration processing, etc. are not supported. It has mainly three operating modes: Host transmitting and slave receiving; host receiving and slave transmitting continuous mode; host receiving and slave transmitting random mode;

4.8 UART

Two independent UARTs can implement serial communication with the following operating modes:

1. 8-bit asynchronous communication mode, baud rate adjustable;
2. 9-bit asynchronous communication mode, baud rate fixed(MCLK/16, MCLK/32);
3. 9-bit asynchronous communication mode, baud rate adjustable.

4.9 SPI

SPI adopts three-line transmission method including SCK (bi-direction clock line), SDI (data output) and SDO (data input), which supports simplex, half duplex, full duplex transmission modes below:

1. Internal (clock)transmitting——external (clock)receiving
2. Internal receiving——external transmitting
3. Internal receiving/transmitting——external receiving/transmitting

4.10 ADC

8-bit AD converter is mainly used for keyboard scan, electronic volume or low-speed data sampling with three input channels (AN0~2) which can be chosen for input conversion voltage and the result is stored in an 8-bit register. There are four clock sources (75KHz, MCLK/8, MCLK/16, MCLK/32) for conversion clock and internal reference voltage or external power supply (VDD) can be reference voltage.

11 clock cycles are needed for one AD conversion, and conversion time is7.3μs when the clock source of ADC is MCLK/8 under 12MHz system clock.

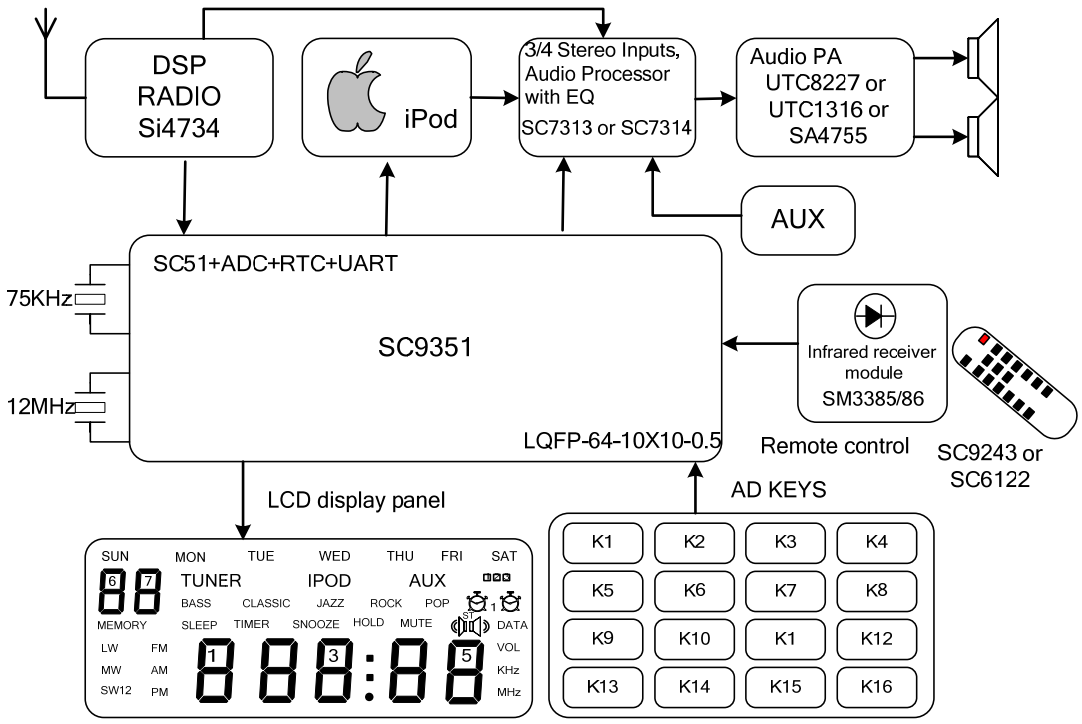
4.11 RTC

The real time clock (RTC) driven by frequency divided-by-2 of 75KHz clock provides clock and calendar function of year, month, week, hour, minute and second and the leap year auto switch function. When setting week, day, hour and minute, the alarm clock generates alarm interrupt which can close or start some function of alarm clock through corresponding alarm control bit.

In standby state, RTC needs to be powered by battery to remain the working state.

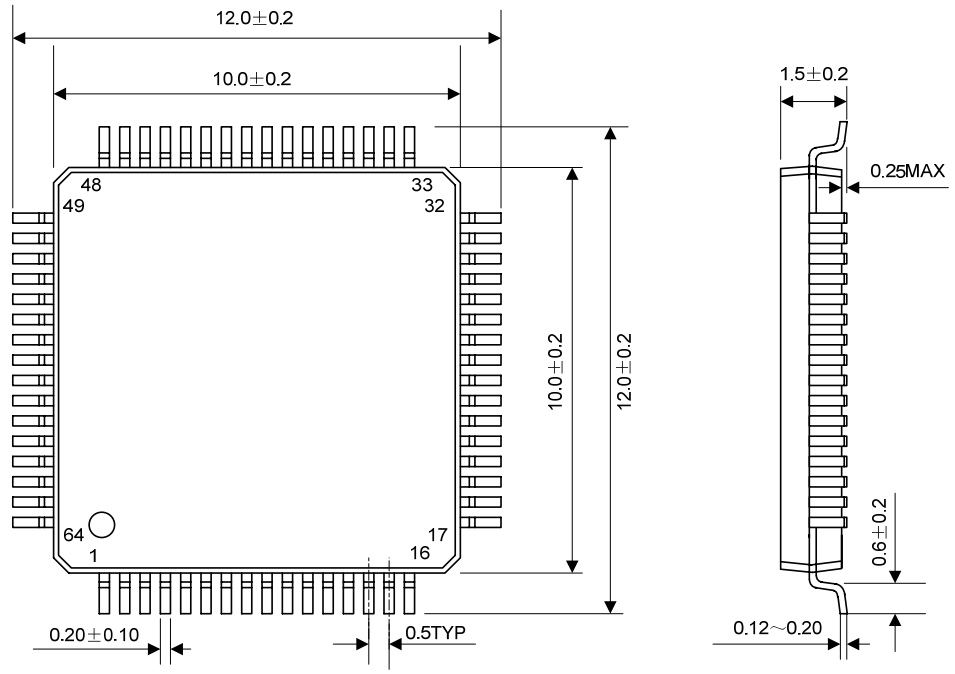
RTC provides an 8-bit timer with four clock sources: 4687Hz, 73Hz, 1Hz and 37.5KHz. The operation of this timer is similar to others and long time timing is easy to realize due to the low-frequency of clock source.

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

LQFP-64-10x10-0.5 Unit: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.