STi7108

Advanced HD AVC decoder with 3D graphics acceleration

Features

- Open GL ES 2.0/Open VG 1.1 compatible 3D graphics GPU for enhanced EPGs/UIs

- Dual HD (1080i/720p) video decode for PIP or mosaic support

- 1080p50, 1080p60 video decoding

- High-performance ST40-300 500 MHz applications CPU with Level 2 cache

- High-performance ST40-300 500 MHz real-time CPU

- Dual eSATA ports

- Triple USB 2.0 host ports

- Dual 16-bit/32-bit LMI supporting DDR2/DDR3

- Dual Ethernet GMAC

- Low power process and design with dynamic power management architecture

Description

STi7108 is the next generation of HD, AVC set-top box decoder for satellite, cable, terrestrial and IP-STB markets.

The STi7108 provides a solution for operators to specify a range of high-performance, MPEG2 / H.264 / VC-1 STBs.

The STi7108 can be used with Zappers, IP clients, DVR standalone, and DVR server/home network STBs, especially where true 3D graphics is required.

Content delivery is possible using broadcast or broadband networks, or both (hybrid STBs).

The STi7108 is also targeted at next generation DLNA compatible Blu-ray (BD) and HD Media players.

For further information contact your local STMicroelectronics sales office.

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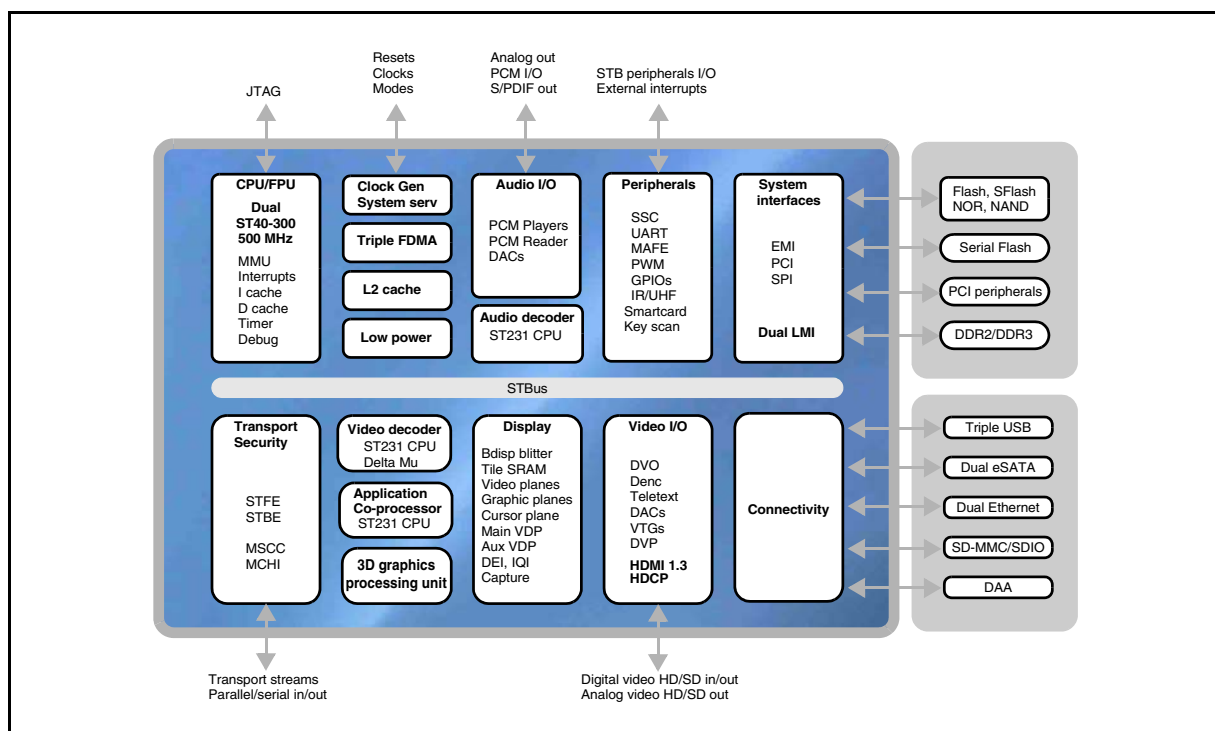
1 Introduction

The STi7108 integrates in a single IC, multi-stream transport demultiplexing, an applications CPU, a real-time CPU, A/V decode, video processing, true 3D graphics and display, advanced security, STB peripherals, audio/video DACs, digital A/V outputs, HDMI, dual eSATA ports, triple USB ports, dual Ethernet controllers (GbE capable) and an SDIO/SD-MMC card controller.

Features	Benefits
ST40 applications CPU, ST40 real-time CPU, ST231 applications co-processor. Each CPU has 32KI and 32K L1 caches with 256K L2 cache for the ST40 applications CPU.	The high performance ST40 CPU for applications and middleware, is enhanced by a real-time companion ST40. The real-time ST40 off loads a/v management and network protocols. The applications CPU is complemented by a co-processor, for multimedia processing and security/DRM in home networks. Each ST40 delivers over 900DMIPs, which together with the ST231, offers an unparalleled 2500DMIPs of CPU performance from a single STB SoC.
Integrated graphics processing unit (GPU). Programmable Vertex (geometry) processor and fragment (pixel) processor, accelerated four times full scene anti-aliasing (4 × FSAA).	True 3D graphics and 2D vector graphics acceleration, optimized for HD consumer digital video applications. Compatible with the latest Open GL ES 1.1/2.0 and OpenVG 1.1 libraries, for best-in-class 3D graphics effects/games, font rendering and Adobe Flash support. Open GL ES 2.x ready. Decoded HD video can be used as textures for visually enhanced, video rich navigation guides and user interfaces.
Latest generation of ST's Delta video decoder with an ST231-based multi-codec capable controller coupled with a High Quality Video Display Pipeline. (HQVDP).	Decoding of advanced high definition standards for broadcast (MPEG2, H264, VC-1, AVS) plus the performance and flexibility for web-based content decoding such as Flash, DivX, MJPEG and Real. New capabilities such as, Dual H264 HP@L4.1 decoding for HD PIP, and video-video transition effects, decoding of H264 HP@L4.2 (1080p50, 1080p60 decoding) and premium rescaling techniques open the way for high quality viewing of enhanced HD services on the latest generation of TVs.
Latest generation transport/security subsystem, with enhanced performance for DVR client/server-based home networks.	Multi-stream transport demultiplexing, descrambling and section/data filtering. Up to 6 live TS inputs supported by an aggregate input rate > 480 Mbits/sec. Decryption/encryption/transcription supported for all the major conditional access systems, local content protection, and DRM security schemes.
Triple USB 2.0 hosts, dual e-SATA , Dual Ethernet MAC with MII/RMII/TMII/GMII interfaces, PCI, SD-MMC/SDIO interface.	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, Gigabit Ethernet, home network controllers (eg MoCA, Wifi), DOCSIS modem and memory cards.

1.1 STi7108 features summary

CPUs

● Applications CPU, ST40-300, dual-issue, MMU, 32KI, 32KD caches, 500 MHz delivering >900DMIPs:
    – Includes an L2 cache, 256KB, 2-way set associative
    – Includes a tightly coupled vector FPU to accelerate 3D graphics transformations
● Real-time CPU for a/v real-time control and network processing offload - ST40-300, dual-issue, MMU, 32KI, 32KD caches, 500 MHz delivering >900DMIPs
● Additional ST231 CPU available for further offloading of the applications CPU with multimedia, security and networking tasks

2D Graphics acceleration

● Link list based, multi-operator 2D graphics blitter
● Supports rendering, formatting and pre-composition of 2D graphics and 3D-like user interface effects
● Up to 266 Mpixels/sec with destination alpha blending
● Tile RAM memory bandwidth saver accelerates blitter based pre-composition of virtual graphics planes before display
● Support for concurrent blitter use by applications and composition threads

3D Graphics acceleration

● True 3D graphics and 2D vector graphics acceleration engine (GPU), optimized for consumer applications
● Programmable Vertex (Geometry) processor and Fragment (Pixel) processor:
    – Accelerated four times full scene anti-aliasing (4×FSAA)
    – Tile based for memory bandwidth efficiency
    – Supports decoded video as textures
● Compatible with industry standard APIs, OpenGL ES 1.1/2.0 and Open VG 1.0/1.1
● Rendering performance up to either 720p60 with 4×FSAA or 1080i60 with 4×FSAA (without lighting) with simple pixel shaders, and up to 720p30 with 4×FSAA with complex pixel shaders (with lighting)

Video decoding, transcoding and post processing

● Latest generation "Delta" Video Decoder with ST231 programmable CPU core:
  – MPEG2, H264, VC-1/WMV9, HD or SD Advanced Video Decoding
  – Provides flexibility to support other codecs for example MPEG4 Pt2, DivX SD/720p, XviD, H263 encode/decode, Real, Flash (Sorenson, ON2/VP6), AVS-SD/HD, MJPEG, Theora
  – Single HD decoding up to H264 HP@L4.2 (1080p50, 1080p60), Dual HD decoding (MPEG2 MP@HL or H264 HP@L4.1), HD + SD decoding or Dual SD Decoding, PIP and Mosaic capable

● Real-time transcoding of MPEG2 SD to H264 SD/CIF/QCIF

● Advanced de-blocking, de-ringing/mosquito noise reduction of decoded MPEG2 sources, based on ST's Digital Source Enhancer (DSE) Technology with 2D Analysis window and Texture Adaptive Filter

High quality video reformatting

● Main display pipeline (HQVDP) comprising DEI, HQR, IQI:
  – DEI - motion and detail adaptive spatial and temporal de-interlacing including 1080i60 >1080p60 deinterlacing. Film mode detection (FMD) supported
  – HQR - high quality reformatting/resizing engine using 8-tap spline-based interpolation filters. Advanced features include built-in global sharpness, overshoot and edge adaptive controls
  – IQI - image quality improvement capabilities including contrast enhancement, luma transient improvement, chroma transient improvement and peaking

● Aux video display pipeline (VDP):
  – High quality H and V reformatting/resizing with sample rate conversion/filtering
  – Motion and detail adaptive spatial and temporal de-interlacing. Film mode detection (FMD) supported

Display and output

- Independent Main and Aux display compositors (Video/Graphics mixing):
  – Four independent graphics planes (GDPs) with H and V resize, CLUT and anti-flicker filtering
  – Flexibility to have three graphics planes on the Main compositor and one on the Auxiliary compositor or two graphics planes on each compositor
  – Two video planes: Main Video plane and a 2nd video plane assignable for PIP or the Auxiliary display
  – PIP is also possible using a graphics plane on Main compositor when the 2nd video plane is used for Auxiliary display
- Two options provided for concurrent HD and SD output of the main composition:
  – HD display capture, down-conversion and auxiliary display with single graphics plane
  – Symmetric assignment of two graphics planes and one video plane set on each compositor
- HDMI 1.3a* interface with HDCP copy protection. (HD/ED/SD formats up to 1080p60, high bit rate audio, deep color modes (30/36bits) and xv-YCC colorimetry pass through):
  – Integrated HDMI CEC line controller
- PAL/NTSC/SECAM digital encoder
- Macrovision and Dwight Cavendish analog copy protection
- Six 10-bit DACs for component/composite analog video output (HD/ED/SD formats up to 1080i):
  – DACs available for HD + SD output, or all DACs can be used for SD output with concurrent HD over HDMI
- Digital video input port (DVP), 8-bit SD, 16-bit HD formats supported
- 24-bit digital video output (DVO) for main display composition (HD/ED/SD formats)

Audio

- ST231 CPU based Audio processor:
  – MPEG1 I/II, MP3, Dolby Digital/DD+, MPEG4 AAC/AAC+, WMA/WMA-pro, Dolby True-HD, DTS HD Master Audio
  – Multi-channel audio decoding with down-mixing
  – PCM mixing with sample rate conversion
  – Volume levelling
  – Concurrent audio description decoding
  – DD+ to DD and AAC+ to DD/DTS up-transcoding
  – Audio encoding to AAC stereo or MP3 stereo for down-transcoding support
- Integrated stereo audio DAC
- 7.1-channel audio PCM output interface
- Stereo audio PCM input interface
- Independent S/PDIF output

Memory interfaces

- Parallel external memory and peripheral interface (EMI):
  - 16-bit data bus, five banks, addressing up to 64 MB per bank. 256 Mbytes total EMI address range
  - Interface to Parallel NOR Flash, SLC NAND Flash, SRAM, and 8-,16-bit Peripherals
  - Secure boot from NOR or NAND Flash
  - Supports ATAPI, DVB-CI and CI-Plus host interface protocols
- High speed SPI interface:
  - Secure boot from Serial Flash
  - Post boot read/write of Serial Flash
  - Supports standard SPI, dual and quad I/O protocols
- Dual -16, 32-bit DDR2/DDR3 local memory interfaces (LMIs), each up to 533 MHz (DDR2/3-1066)

Connectivity

- Triple USB 2.0 Host interfaces including PHYs
- Two e-SATA HDD interfaces
- 32-bit, 33 MHz, PCI interface, shared on EMI with access interleaving possible
- Two integrated Ethernet GMACs. Each supports: wake-on-LAN, multiple hardware address filters, 10/100 MII/RMII, Turbo-MII up to 300 Mbits/sec and GMII up to 1000 Mbits/sec.
- 8-bit, 52 MHz, SD-MMC/SDIO interface for memory cards and eMMC:
  - V4.3 for eMMC flash support
  - SD HC V2.0 PART A2
- Soft modem support: integrated MAFE: integrated system side DAA. (Si-Labs)

Transport and security

- Front end transport stream pre-processor (STFE):
  - PID filtering and transport stream merging
  - Six external TS inputs
  - Four internal TS paths from memory
  - TS I/O routing for DVB-CI/CI-Plus, TS I/O routing for MultiStream CableCard with stream merging/demerging
  - Aggregate TS processing > 480 Mbits/sec live input rate
- Transport stream processor with security co-processor (STBE)
  - Multi-stream transport stream de-multiplexing from any source (Broadcast, IP Network, DVR)
  - Section filtering and clock recovery
  - Supports CA vendors' latest advanced security specifications
  - DVB/DES/TDES/AES/Multi-2/ICAM2.2 descrambling
  - ATIS-IIF and CI-Plus descrambling
  - Multi-stream AES/TDES encryption/decryption for local copy protection or network DRM schemes including SVP, DTCP-IP, WMDRM, DVB-CPCM, DivX, Marlin

DVR support

- DVR supported with HDD attachment through e-SATA or USB

- Server application supported: Multi-Stream DVR recording and playback for viewing locally (with time-shift), concurrently with playback to multiple clients

- Time-shift supported without HDD attached using stream buffering in NAND Flash attached directly through EMI or USB, SATA, SD-MMC card or e-MMC

STB peripherals, system services, package

- Two smartcards, four UARTs, seven SSC/I²C, 27 × 8 GPIO banks with alternate functions, IR Tx/Rx, UHF Rx/SCD, PWM, ILC, 4×4 key matrix scanner

- All required clocks generated on chip from PLLs and frequency synthesizers

- Reset controller, watchdog timers, real-time clock (RTC) and protected JTAG/DCU port

- Passive standby mode for lowest power consumption, and dynamic power management architecture to optimize power efficiency of active standby modes

- Package - PBGA 35×35 864 balls, 1.0 mm ball pitch, 0.5 mm ball diameter

2 Target applications

2.1 Satellite applications
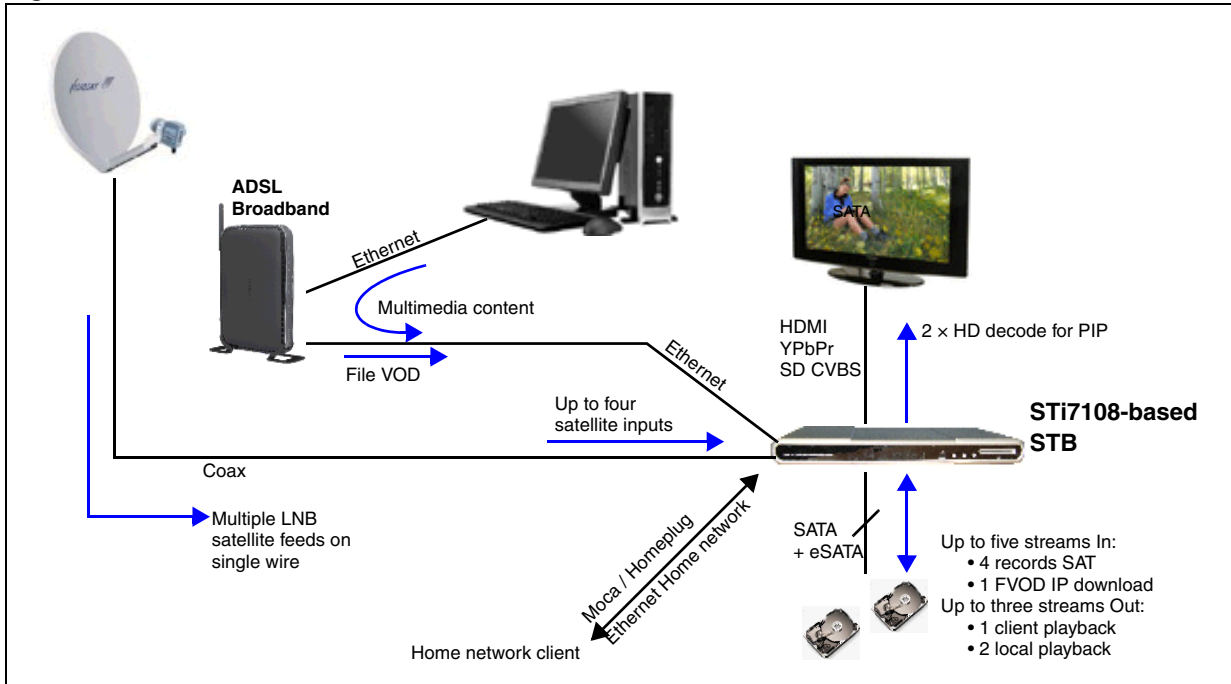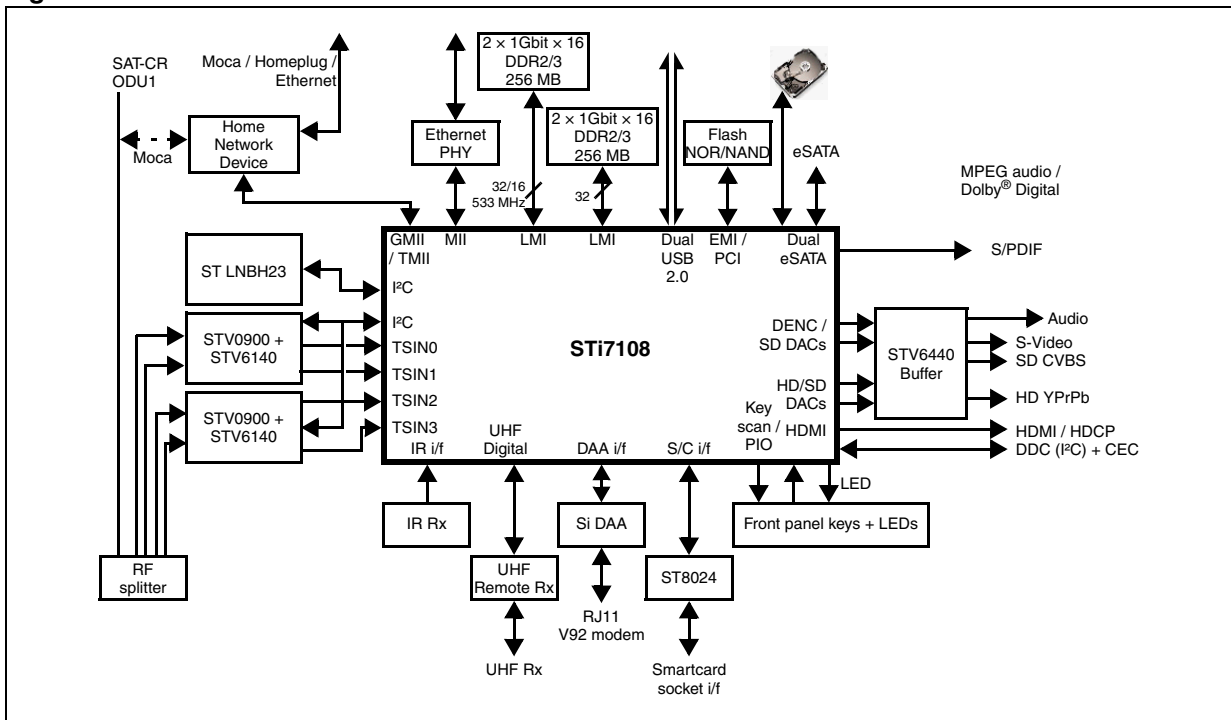
Figure 1. Satellite HD DVR

Figure 2. Satellite HD four tuner DVR

2.2 Cable applications

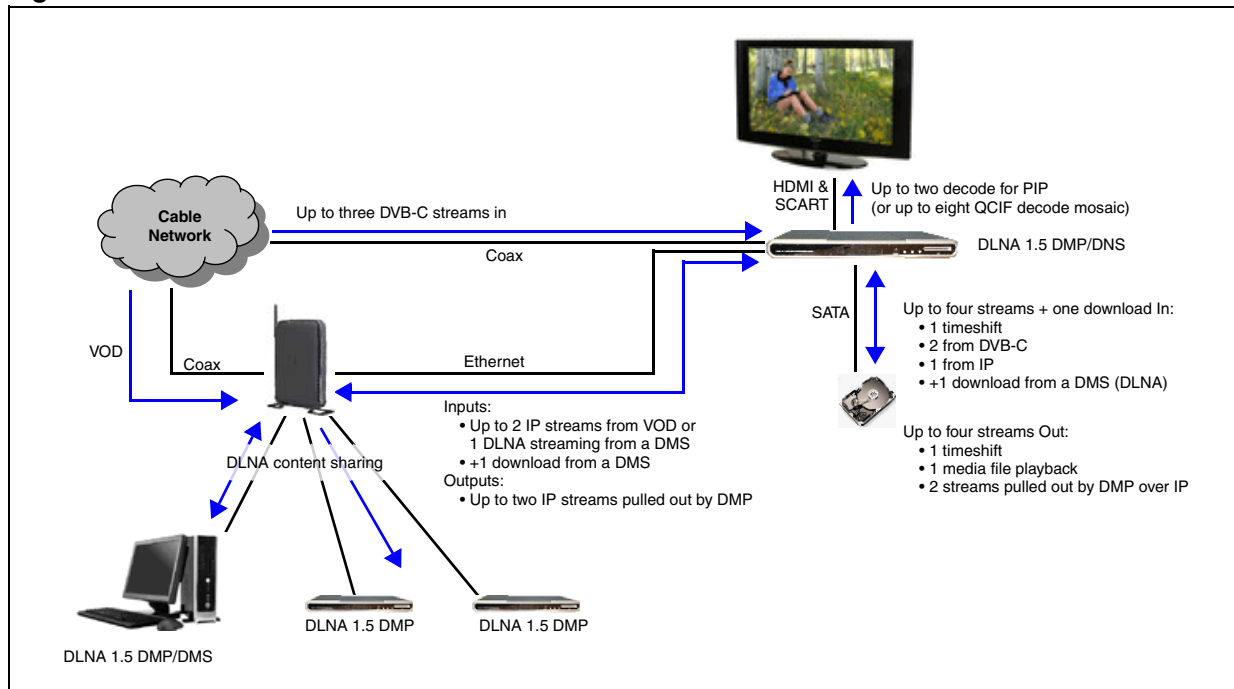**Figure 3. Cable DVR with DLNA server**
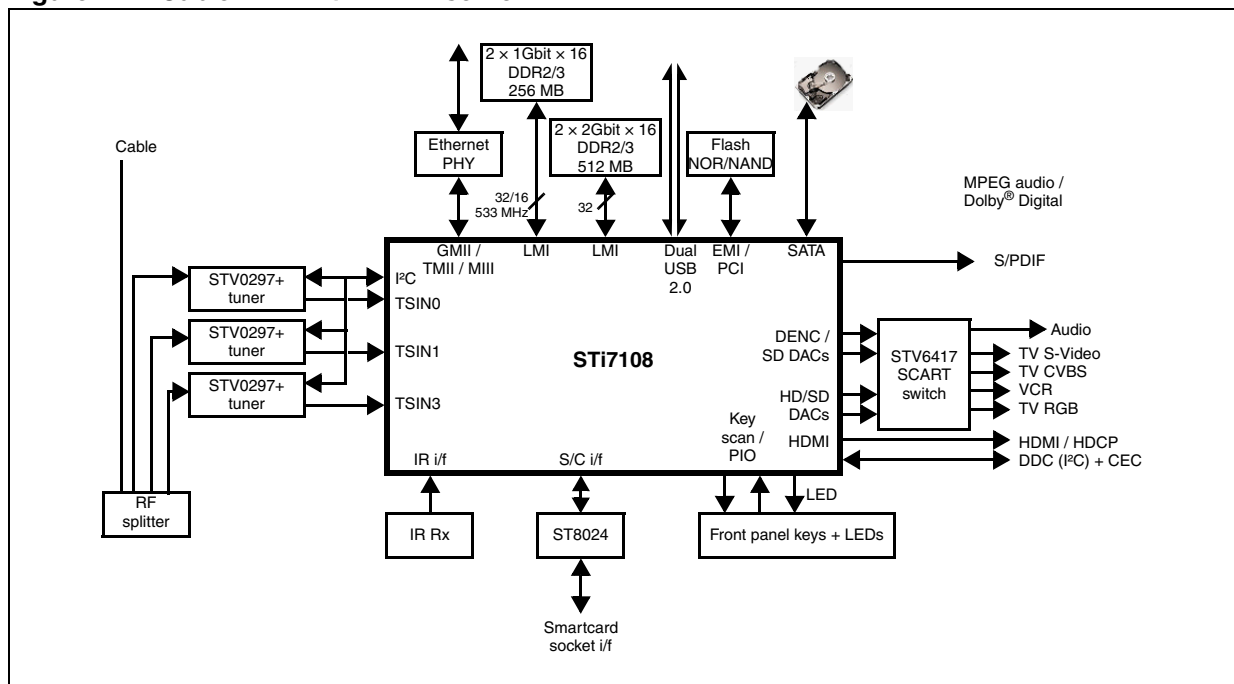

Figure 4. Cable DVR with DLNA server
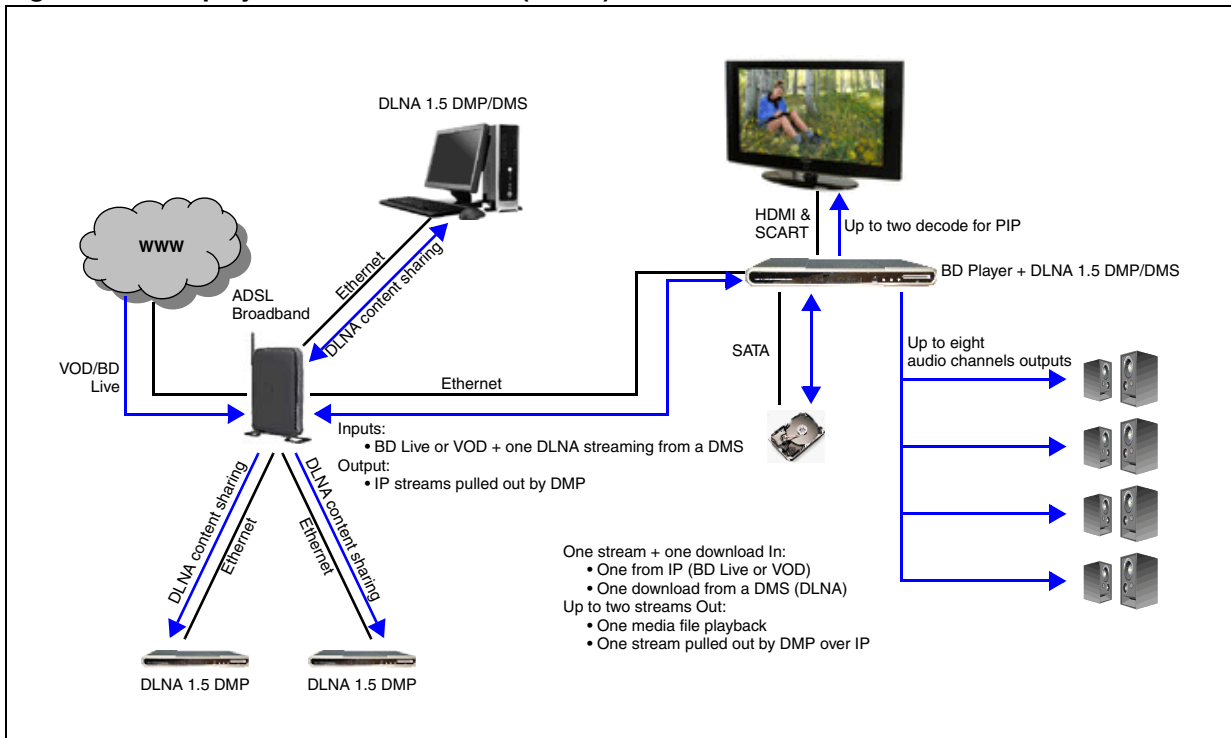
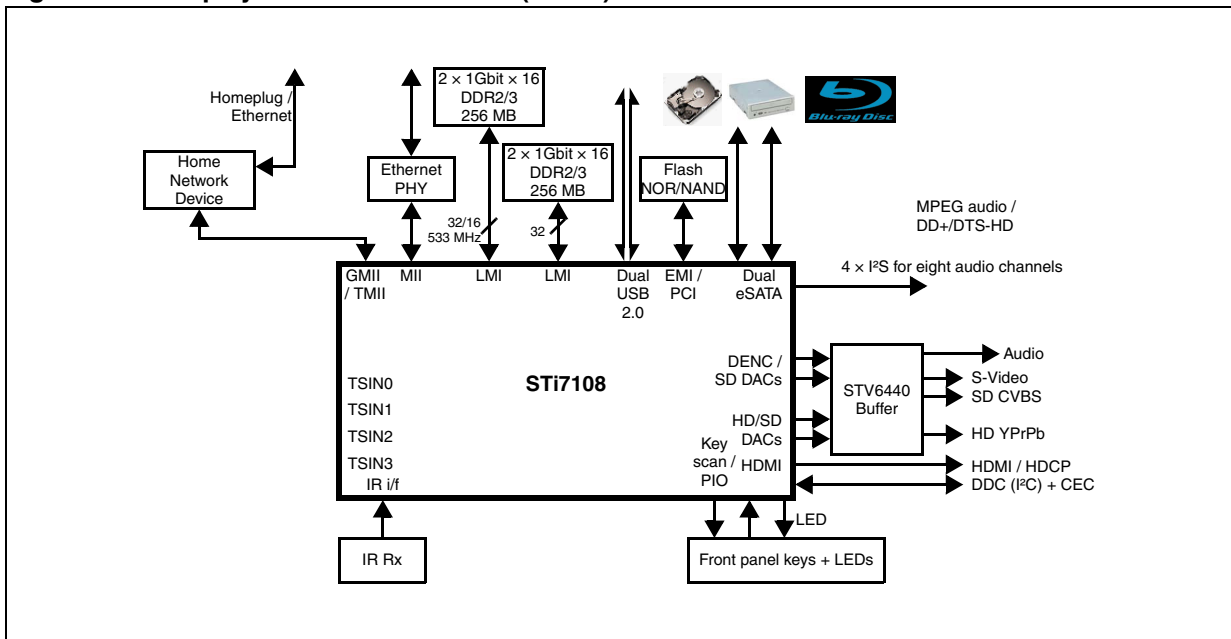**Figure 5. BD player with media center (DLNA)**

Figure 6. BD player with media center (DLNA)

3 Ordering information

Table 1.   Ordering information

Order code	Packaging	Description
STi7108ZWA	FPBGA 35 mm × 35 mm	Development version, all options

4 Revision history

Table 2.   Document revision history

Date	Revision	Changes
16-Nov-2009	1	Initial release.

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